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Ti/Pt/Ti/Cu-Metallized Interconnects for GaN High-Electron-Mobility Transistors on Si Substrate

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Cu-metallized interconnects for GaN high-electron-mobility transistors (HEMTs) on Si substrate using a Pt/Cu diffusion barrier layer are investigated. Auger electron spectroscopy (AES) depth profiles indicate that the GaN/Au/Ti/Pt/Ti/Cu thin metal structure is thermally stable up to 350 °C. The Cu-metallized devices using the proposed metal scheme exhibited DC characteristics comparable to those of conventional Au-metallized GaN devices even after annealing at 350 °C for 30 min. No degradation in current with time was observed when the device was tested under 28 V high-voltage stress for 24 h at room temperature. These results indicate that the Cu-metallized airbridges with the Ti/Pt/Ti/Cu diffusion barrier layer can be used for GaN HEMT fabrication.

GaN high-electron-mobility transistors (HEMTs) have been widely studied due to their high breakdown voltage (3.3 mV/cm), high electron saturation velocity ($\sim 3 \times 10^7$ cm^2/s), large band gap, and high operating temperature, which are suitable for power device applications.[1–3] In the conventional HEMT process, gold (Au) is usually used as the major metallization metal for interconnects. However, the price of gold is increasing. Copper (Cu) has a lower resistivity (1.67 μΩ cm for Cu; 2.2 μΩ cm for Au),[4,5] a higher thermal conductivity (4.01 W cm^{-1} K^{-1} for Cu; 3.18 W cm^{-1} K^{-1} for Au), and a lower cost (the price of Cu is 400 times cheaper than Au), and is widely considered as a good candidate to replace gold as the metallization metal for GaN devices.

However, Cu can easily diffuse into GaN and cause deterioration in device characteristics when in direct contact with the GaN material without any diffusion barrier.[6–8] Therefore, an effective diffusion barrier is necessary for GaN devices to prevent Cu diffusion into the GaN material when Cu is to be used as the interconnect metal.[9] Reports have shown that the high-melting-point metal Pt is an effective diffusion barrier to prevent Cu diffusion into III–V devices, and the Ti/Pt/Cu material system is very stable after annealing at 350 °C for 30 min.[10–12]

On the other hand, reports have shown that the peeling off between Au and WN$_x$ layers was observed when using WN$_x$ as the diffusion barrier for Cu on GaAs devices, which indicates an adhesion problem between these films, a Ti addition layer was applied to the Au/WN$_x$ and WN$_x$/Cu interfaces to solve this adhesion problem.[13] Also, Ti is widely used as the adhesion layer for Schottky contact metal in the GaAs-based electronic device. In this study, Ti/Pt/Ti thin metal layers are used as the diffusion barrier for Cu airbridges for GaN HEMTs on Si substrate. The DC characteristics of the Au-metallized and Cu-metallized GaN HEMTs are compared, and the thermal stability and reliability of GaN/Au/Ti/Pt/Ti/Cu multilayer structures for Cu-metallized GaN HEMTs are evaluated in this work.

The AlGaN/GaN HEMT device structures were grown by metal organic chemical vapor deposition (MOCVD) on Si substrate. The epi layers of the device, from the Si substrate to the top, were AlN, AlGaN buffer layers, GaN channel layer, undoped AlN spacer, AlGaN Schottky layer, and GaN cap layer. The AlGaN/GaN HEMT fabrication process consisted of Ohmic contact formation, device active region definition, gate formation, device passivation, and the airbridge process for AlGaN/GaN HEMT interconnects.

The GaN HEMT fabrication process started with Ohmic contact formation. An Ohmic metal of Ti/Al/Ni/Au was deposited on the wafer using an e-gun evaporator,[14–16] the wafer was then annealed by rapid thermal annealing (RTA) at 800 °C for 60 s in N$_2$ ambient. The Ohmic contact resistance of 3.2×10^{-6} (Ω cm^2) was obtained by the transmission line method (TLM). Then, mesa regions were formed by etching in the inductive couple plasma (ICP) reactor using Cl$_2$ in Ar ambient. After device isolation, the wafer was coated with photoresist AZ 2020 and exposed using an I-line aligner to define the gate region. Then, the wafer was dipped in 10% HCl solution to remove the native oxide on the GaN surface, and then gate metal Ni/Au was deposited by e-gun evaporation on GaN with the gate length of 1.5 μm. After gate formation, a 100-nm-thick Si$_3$N$_4$ film was deposited on GaN by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C for device passivation.[17] The contact vias of the SiN film were etched by reactive ion etching (RIE) with CF$_4$/O$_2$ plasmas. Finally, Pt and Ti were used as the diffusion barrier layer and adhesion layer, respectively, for the device interconnects. The thin metal structure of Ti/Pt/Ti/Cu was used as a seed layer for Cu airbridges and was deposited from the bottom to the top by sputtering.[18,19] Then, the CuSO$_4$•5H$_2$O electrolyte was used for Cu electroplating at room temperature. The Cu airbridges fabricated on GaN HEMT devices are shown in Fig. 1.

The Au/Ti/Pt/Ti/Cu multilayer deposited on the GaN blanket wafer was analyzed by Auger electron spectroscopy (AES) to evaluate the thermal stability of the material system. Au was used because it was the top layer of the Ohmic metal. The AES depth profiles are shown in Fig. 2. Figure 2(a) is the data for the as-deposited sample. Figures 2(b) and 2(c) are the data of the samples after annealing at 350 and 400 °C for 30 min, respectively. The data from Fig. 2 indicate that there was no obvious interatomic diffusion between Cu and Au after 350 °C annealing for 30 min. However, Cu and Au began to diffuse into each other through the Pt diffusion barrier layer after the

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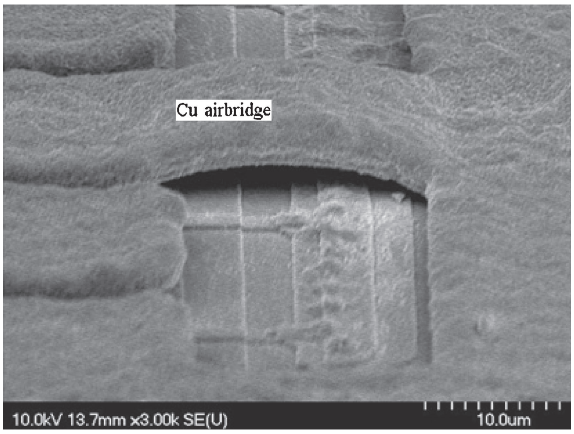
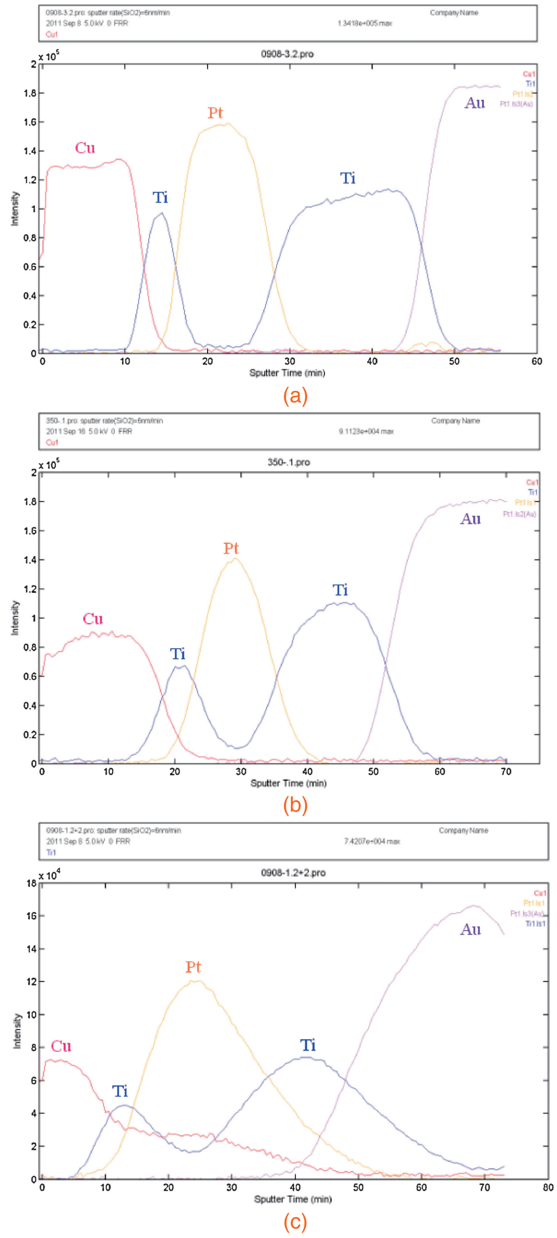


Fig. 1. SEM image of the GaN HEMT with Cu airbridges by using Ti/Pt/Ti/Cu multilayer diffusion barrier.

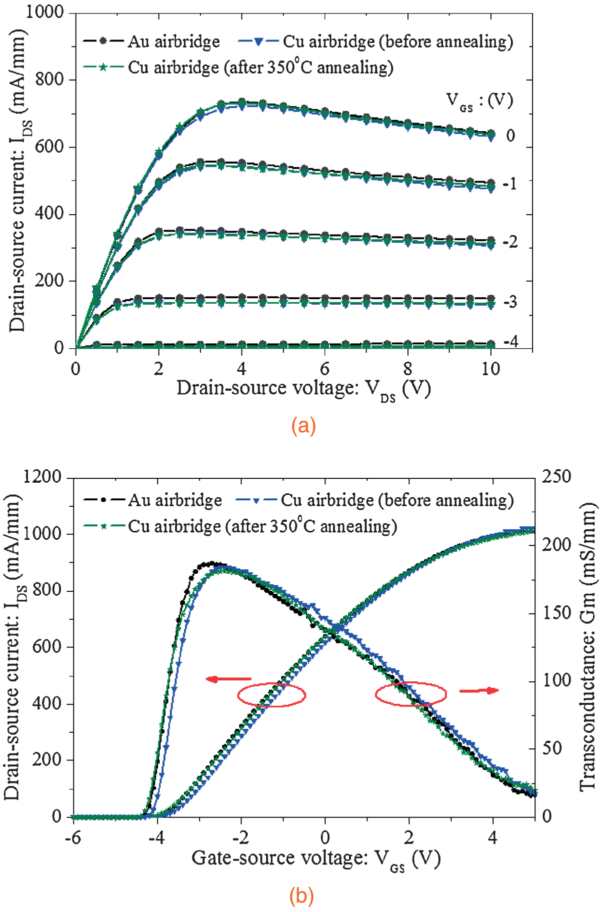


(a)

(b)

(c)

Fig. 2. AES depth profiles of the Au/Ti/Pt/Ti/Cu multilayer structure: (a) as-deposited, (b) after 350 and (c) 400 °C annealing for 30 min.



(a)

(b)

Fig. 3. DC characteristics of the 50 × 4-µm-gate-width Cu-metallized GaN HEMT before and after annealing at 350 °C for 30 min: (a) I_{DS} versus V_{DS} curves, and (b) G_m and I_{DS} versus V_{GS} curves.

sample was annealed at 400 °C for 30 min. A Cu_4Ti phase formed after the annealing process and resulted in the device deterioration. The phenomenon is the same as that reported in ref. 20.

To evaluate the device performances of GaN HEMT with Cu airbridge interconnects, 50 × 4-µm-gate-width GaN HEMTs with Cu airbridges using a Ti/Pt/Ti/Cu diffusion barrier structure were fabricated. The performances of the HEMT devices with Cu airbridges were compared with those GaN HEMTs with Au airbridges. The DC characteristics of GaN HEMT with Au airbridges and GaN HEMT with Cu airbridges before and after 350 °C annealing are shown in Fig. 3. The performances of the Cu-metallized devices are listed below: the drain–source current (I_{DS}) was 631 mA/mm (Au: 642 mA/mm), the maximum drain–source current (I_{DSmax}) was 1020 mA/mm (Au: 1010 mA/mm), the threshold voltage (V_t) was −4.1 V (Au: −4.2 V), and the maximum extrinsic transconductance ($G_{m,max}$) was 184 mS/mm (Au: 187 mS/mm) at $V_{DS} = 10$ V. The Cu airbridge devices were also tested after annealing at 350 °C for 30 min to determine their stability at high temperature. I_{DS} of 638 mA/mm, I_{DSmax} of 1012 mA/mm, V_t of −4.3 V, and $G_{m,max}$ of 181 mS/mm were obtained for the Cu-metallized HEMTs after annealing at 350 °C for 30 min, as shown in Fig. 3. Comparison of the Cu airbridge devices with and without annealing shows no obvious device degradation and no obvious decay of the I_{DS} and G_m

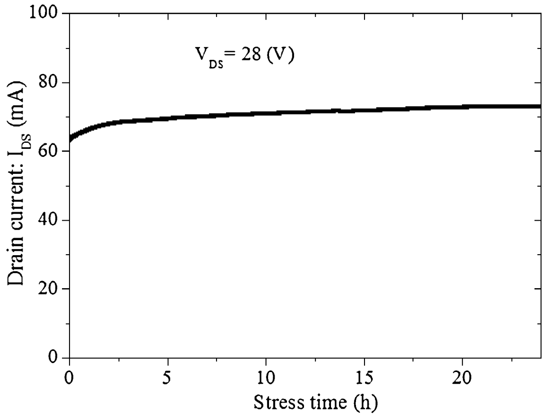


Fig. 4. Drain–source current of the Cu-metallized GaN HEMT after being stressed at 28 V for 24 h at room temperature.

for Cu-metallized GaN HEMT was observed even after annealing. Figure 4 shows the Cu-metallized GaN HEMT with a Ti/Pt/Ti/Cu seed layer after being stressed at the high voltage of 28 V for 24 h at room temperature. Little change was observed after the stress, indicating that the material system was quite stable.

Cu-metallized GaN HEMT using a Ti/Pt/Ti/Cu metal scheme was successfully fabricated and showed electrical characteristics comparable to those of the Au-airbridged GaN HEMT. The AES depth profiles of the Au/Ti/Pt/Ti/Cu multilayer after thermal annealing at 350 °C for 30 min indicate that the material system is quite stable. Also, the Cu-metallized and Au-metallized devices exhibited comparable DC characteristics even after 350 °C annealing for 30 min. In conclusion, we have demonstrated that Pt is an effective diffusion barrier for Cu-metallized interconnects on GaN HEMT. The Cu-metallized GaN HEMT device shows good thermal stability and the performances are comparable to those of Au-metallized GaN HEMT devices.

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1) S. N. Mohammad, A. Salvador, and H. Morkoc: Proc. IEEE **83** (1995) 1306.
2) H. Morkoc, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns: J. Appl. Phys. **76** (1994) 1363.
3) U. K. Mishra, P. Parikh, and Y. F. Wu: Proc. IEEE **90** (2002) 1022.
4) J. D. Plummer, M. D. Deal, and P. B. Griffin: *Silicon VLSI Technology* (Prentice Hall, Upper Saddle River, NJ, 2000) 695.
5) J. R. Lloyd, J. Clemens, and R. Snede: Microelectron. Reliab. **39** (1999) 1595.
6) V. Rajagopal Reddy and P. Koteswara Rao: Microelectron. Eng. **85** (2008) 470.
7) E. R. Weber: Appl. Phys. A **30** (1983) 1.
8) A. Cros, M. O. Aboelfofotoh, and K. N. Tu: J. Appl. Phys. **67** (1990) 3328.
9) S. W. Chang, E. Y. Chang, C. S. Lee, K. S. Chen, C. W. Tseng, and T. L. Hsieh: IEEE Trans. Electron Devices **51** (2004) 1053.
10) S. W. Chang, E. Y. Chang, D. Biswas, C. S. Lee, K. S. Chen, C. W. Tseng, T. L. Hsieh, and W. C. Wu: Jpn. J. Appl. Phys. **44** (2005) 8.
11) Y. C. Wu, E. Y. Chang, Y. C. Lin, S. H. Chen, W. C. Wu, L. H. Chu, and C. Y. Chang: IEEE Microwave Wireless Components Lett. **17** (2007) 133.
12) S. W. Chang, E. Y. Chang, C. S. Lee, K. S. Chen, C. W. Tseng, Y. Y. Tu, and C. T. Lee: Jpn. J. Appl. Phys. **44** (2005) 899.
13) C. S. Lee, Y. C. Lien, E. Y. Chang, H. C. Chang, S. H. Chen, C. T. Lee, L. H. Chu, S. W. Chang, and Y. C. Hsieh: IEEE Trans. Electron Devices **53** (2006) 1753.
14) R. Gong, J. Wang, S. Liu, Z. Dong, M. Yu, C. P. Wen, Y. Cai, and B. Zhang: Appl. Phys. Lett. **97** (2010) 062115.
15) M. Piazza, C. Dua, M. Oualli, E. Morvan, D. Carisetti, and F. Wyczisk: Microelectron. Reliab. **49** (2009) 1222.
16) B. Jacobs, M. C. J. C. M. Kramer, E. J. Geluk, and F. Karouta: J. Cryst. Growth **241** (2002) 15.
17) B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman: IEEE Electron Device Lett. **21** (2006) 268.
18) B. Johnson, R. Amster, and L. Vanasupa: J. Electron. Mater. **27** (1998) 923.
19) S. Shibuki, H. Kanao, and T. Akahori: J. Vac. Sci. Technol. B **15** (1997) 60.
20) Y. C. Lien, E. Y. Chang, S. H. Chen, L. H. Chu, P. C. Chen, and Y. C. Hsieh: Appl. Phys. Lett. **89** (2006) 083517.