A Bias-Varied Low-Power K-band VCO in 90 nm CMOS Technology

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***Abstract*—This letter presents a novel bias-varied low-power K-band voltage controlled oscillator (VCO) in a standard 90 nm CMOS technology. This circuit exhibits low power consumption of $\leqq$ 3mW and a 12.2% tuning range with low phase noise characteristic. These performances are realized by combination of the transformer-feedback and the switchable active circuit block, which can control the dc power at different frequencies and improve the phase noise.**

***Index Terms*—Bias-varied, k-band, phase noise, switchable active circuit, voltage controlled oscillator (VCO).**

I. Introduction

In microwave CMOS voltage controlled oscillator (VCO) designs, the phase noise performance is substantially limited by two device-related issues: the relatively high $1/f$ noise of sub-micron MOSFETs [1], [2], and the poor Q-factors of on-chip passive components due to lossy silicon substrate. These effects; therefore, hamper the low-power and low-voltage targets in CMOS VCOs because of lacking acceptable signal-to-noise ratio (SNR) in circuits.

To achieve the low-power goal, several transformer-based feedback CMOS VCOs (TF-VCOs) were proposed [3]–[9]. The major advantage of TF-VCOs is that the dynamic gate-to-source voltage can be enhanced to improve the circuit SNR under a low supply voltage. In addition, a properly designed transformer has a higher Q-factor than an on-chip inductor of the similar size. However, the severe challenge to design high frequency TF-VCOs is that the parasitic capacitance within transformer significantly restricts the operation frequency and the tuning range. To address this issue, the edge-coupled transformers were usually used in K-band TF-VCOs to minimize the parasitic capacitance [7]–[9]. Nevertheless, this approach inevitably decreases the coupling coefficient of the transformer and the strength of magnetic feedback. Different circuit techniques were also adopted in these K-band TF-VCOs to achieve the low power target, as forward body-bias [7], [8] and the current-reused topology [9]. However, the tuning ranges of these circuits are still relatively limited and seldom exceed 10%.

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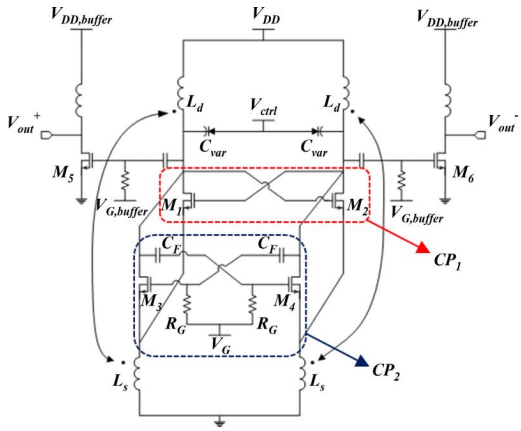

Fig. 1. Schematic diagram of the proposed VCO.

In this letter, we proposed a low power K-band TF-VCO based on another power-reduction perspective. In addition to using transformer-feedback for low power operation, the bias-varied method is adopted in this circuit to control the dissipated power at different frequency ranges. Besides, the active circuit design has an extra merit of improving phase noise with lesser power consumption.

II. Circuit Design

Fig. 1 shows the schematic of the proposed circuit. The drain-to-source transformer-feedback technique in [3] is used in low power operation, where L_d and L_s are the self-inductances of the primary and the secondary coils in the transformer, respectively. To design a VCO operating around 20 GHz with a tuning range larger than 10%, the single-turn, edge-coupled structure was adopted in the transformer design to reduce unwanted parasitic capacitance. This transformer has $L_d = 0.14$ nH, $L_s = 0.086$ nH and a moderate coupling factor of 0.72, which is designed for a balance between the feedback strength and the operation frequency.

The frequency tuning is realized by the accumulation mode varactor, C_{var}, with the device size of $W/L = 28.8\ \mu\text{m}/0.4\ \mu\text{m}$. In a low-power K-band VCO, another major difficulty to achieve a wide frequency tuning is the significant degradation in Q-factor of $C_{var}(Q_{Cvar})$ while C_{var} changes from the depletion region to the inversion region, as shown in Fig. 2. This result implies that the minimum dc power for maintaining oscillation at different frequencies is restricted by the lower Q_{Cvar}. From this point of view, we designed a bias-varied TF-VCO by dividing the active circuit into

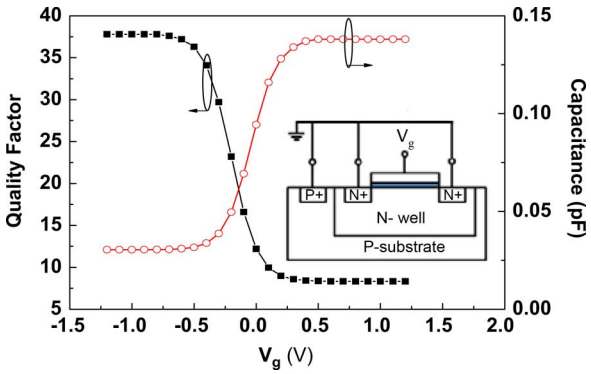

Fig. 2. Simulated capacitance and Q-factor of C_{var} at 20 GHz.

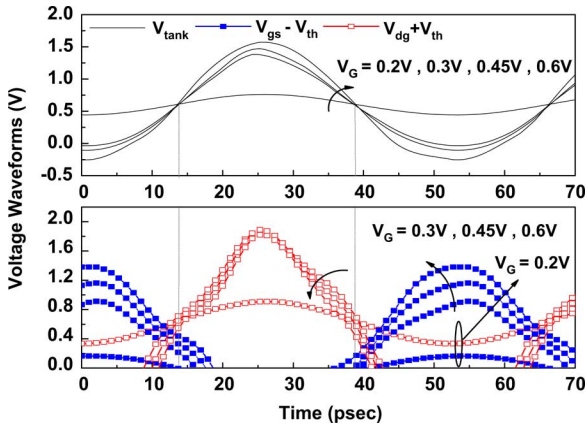

Fig. 3. Simulated voltage waveforms in the LC-tank (top) and in CP_2 (bottom).

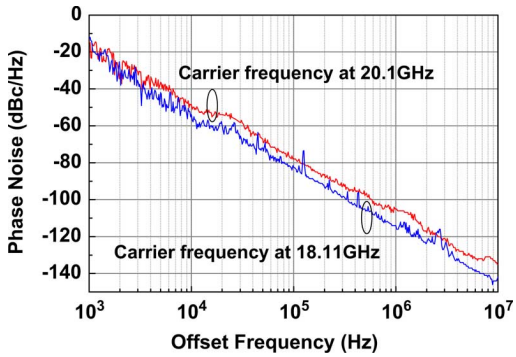

Fig. 4. Measured phase noise of the fabricated VCO at 18.11 and 20.1 GHz with respect to 1 MHz frequency offset.

two cross-coupled pairs, CP_1 and CP_2, where CP_1 utilizes the traditional cross-coupled topology, and CP_2 uses the capacitive feedback as in [10]. The MIM capacitor C_F of 0.62 pF is used to provide the feedback paths in CP_2 and to separate the dc levels of the gate and the drain terminals of transistors. The operation state of CP_2 is controlled by V_G through the large resistor R_G of 3.2 kΩ. In the high frequency range with lower C_{var}, the oscillation is maintained by operating CP_1 solely, where the negative V_G is used to switch off CP_2 for the power-saving goal. When the operation frequency decreases and C_{var} enters into the inversion mode, the gate-bias V_G is increased to turn on the CP_2, providing additional negative resistance to compensate the loss due to the decreased Q_{Cvar}. Since CP_2 is used to compensate the significant varactor loss at the inversion mode, the total transistor width in CP_2 should be larger than in CP_1 to acquire enough trans-conductance; however, the size of CP_2 should be compromised with the design targets of power consumption, operation frequency and tuning range for a low-power K-band VCO. In this design, a small unit-gate-width of 2 μm is applied for the active device to reduce gate resistance, while each transistor in CP_1 and in CP_2 has gate-fingers of 8 and 16, respectively. For the interest K-band frequency, the selected C_F and R_G satisfy $\omega C_F R_G \gg 1$, therefore ensuring that the input voltages in both cross-coupled pairs can keep almost the same phase.

When the proposed VCO operates in the lower Q_{Cvar} region, it is worth to investigate the relationship between the phase noise performance and power consumption. It seems raising V_G level can directly improve the circuit SNR because of the transistor trans-conductance (g_m) is positively related to the overdrive voltage (V_{ov}). However, because of the small threshold voltage (V_{th}) of 90 nm NMOSFETs, the large-signal voltage swing can easily push the transistor biased at a high V_G into the nonlinear triode region. This issue can further decrease the tank Q-factor due to the lower transistor output impedance in the triode region. Fig. 3 exhibits the simulated voltage waveforms under different V_G biases, where the transistor turns on during $V_{gs} - V_{th} > 0$ but only works in the saturation region while $V_{ds} > V_{gs} - V_{th}$ or $V_{dg} + V_{th} > 0$. Although V_{ov} amplitude can be monotonically increased with increasing V_G, the transistor also enters in the triode region deeply and further deviates from the linear voltage-to $-g_m$ relation. On the other hand, while V_G decreases, the conduction periods of the transistor are further away from the zero-crossing of the tank voltage. According to the LTV model, the noise current has the maximum effect on the excess phase if the charge injection is applied at the zero-crossing of the tank voltage [11]. Therefore, the proposed circuit can improve the cyclo-stationary noise property by adopting the semi-Class-B biasing of $V_G = 0.2 \sim 0.3$ V, with lesser power dissipation than using the traditional cross-coupled pair of the same total transistor size. For high-frequency and low-power designs, the combination of CP_1 and CP_2 is also a more feasible topology to realize such semi-Class-B operation than only using a single capacitive feedback cross-coupled pair, which is because of the two advantages: First, the proposed topology has the smaller parasitic capacitance, which is due to that part of active devices are biased at higher overdrive voltage (CP_1); therefore the overall transistor size can be shirked while providing the same trans-conductance as a larger cross-coupled pair biased at Class-AB or Class-B mode; besides, in this approach, the difference between the two V_G states can be relatively large to prevent incorrect switching due to external noise but do not increase the power consumption; this is difficult to realize in a single capacitive feedback cross-coupled pair, since its dc power is sensitive to the gate bias.

III. Measurement Results

The proposed VCO was implemented in a standard 1P9M 90 nm CMOS technology. The performance measurements were carried out by an Agilent E5052 system through on-wafer probing, while the core circuit is biased at a supply voltage

TABLE I
PERFORMANCE COMPARISON OF THE RECENT REPORTED LOW-POWER, K-BAND CMOS TF-VCOS

Refs.	CMOS Tech.	Freq. (GHz)	$V_{DD,core}$ (V)	$P_{DC,core}$ (mW)	Tuning Range (%)	Phase Noise @1MHz Offset (dBc/Hz)	FOM_T (dBc/Hz)
[6]	0.18μm	18.95	1.35	3.3	3.58	-110.82	-182.3
[7]	0.18μm	21.37	0.6	3.5	5.1	-109.8	-184.9
[8]	0.13μm	24	0.6	3	9.4	-113	-195.3
			0.38	0.75	2.6	-96	-173.1
[9]	90nm	20.8	1.3	3	4.8	-116.4	-191.6
This Work	**90nm**	**19.19**	**0.6**	**1.4**	**4 (19.59GHz-20.36GHz)**	**-105.4**	**-182**
				3	**8.2 (18.02GHz-19.59GHz)**	**-114.1**	**-192.8**

$$\mathrm{FOM_T} = L\{\Delta f\} - 20\log_{10}[\frac{Tuning\ Range(\%)}{10}\frac{f_0}{\Delta f}] + 10\log_{10}(\frac{P_{DC,core}}{1mW})$$

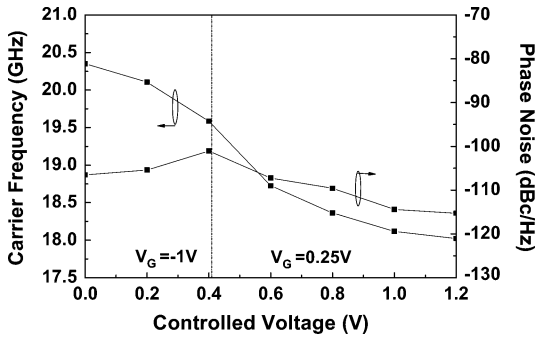

Fig. 5. Measured tuning range and phase noise of the proposed VCO.

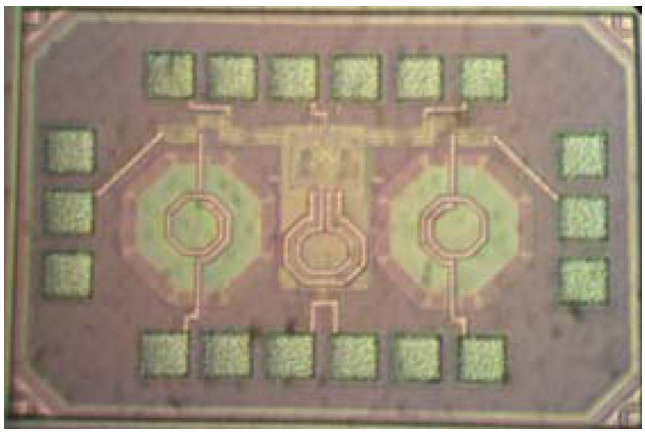

Fig. 6. Microphotograph of the fabricated VCO.

of 0.6 V. Fig. 4 shows the measured phase noises as -114.1 and -105.4 dBc/Hz at 1-MHz offset from the 18.11- and 20.1-GHz carriers.

The frequency tuning and the phase noise characteristics of this circuit are shown in Fig. 5. When the controlled voltage (V_{ctrl}) ranges from 0 to 0.4 V, a negative V_G of -1 V is applied to turn off CP_2. The corresponding oscillation frequency in this condition is from 20.36 to 19.59 GHz. As V_{ctrl} increases from 0.4 to 1.2 V, a small V_G of 0.25 V is used to bias the CP_2 at a semi-Class-B mode, and the corresponding carrier frequency is from 19.59 to 18.02 GHz. The average phase noises of $V_G = -1$ V and $V_G = 0.25$ V regions are -104.3 and -111 dBc/Hz, respectively. The whole tuning range of this VCO is as large as 12.2% at K-band. The VCO core consumes 1.4 and 3 mW power at $V_G = -1$ V and $V_G = 0.25$ V, respectively. Table I compares the performance of the recent K-Band CMOS TF-VCOs with low power consumption of < 5 mW. The proposed oscillator achieves a 12.2% tuning range, low phase noise and the excellent Figure-of-merit-with-tuning-ranges ($\mathrm{FOM_{TS}}$). Fig. 6 displays the microphotograph of the fabricated VCO. The total chip size is $0.66 \times 1\ \mathrm{mm}^2$, and the core circuit area is about $0.4 \times 0.24\ \mathrm{mm}^2$ excluding the buffer stage and the pad frames.

IV. CONCLUSION

The proposed low power K-band VCO is demonstrated in a standard 90 nm CMOS process. By combining the switchable active circuit design with the transformer-feedback, this circuit exhibits low power, large tuning range and excellent $\mathrm{FOM_{TS}}$ at two adjacent operation frequency ranges.

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