A Wafer-Level Three-Dimensional Integration Scheme With Cu TSVs Based on Microbump/Adhesive Hybrid Bonding for Three-Dimensional Memory Application

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***Abstract*—Thin wafer/chip stacking with vertical interconnect by a Cu through-silicon via (TSV) and a Cu/Sn microjoint is one of the candidates for 3-D integration. The insertion loss of the two-chip stack was evaluated with different TSV pitches, microbump diameters, and chip thicknesses to realize the signal transmission effects in high-speed digital signaling via TSV and microjoint interconnection. In addition, a wafer-level 3-D integration scheme with Cu TSVs based on Cu/Sn microbump and BCB adhesive hybrid bonding was demonstrated. Key technologies, including TSV interconnection, microbumping, hybrid bonding, wafer thinning, and backside RDL formation, were well developed and integrated to realize 3-D integration. This paper presents a complete study of the structure design, the process condition, and the electrical and reliability assessment of the wafer-level 3-D integration scheme. This 3-D integration scheme with excellent electrical performance and reliability provides a promising solution for 3-D memory application.**

***Index Terms*—Hybrid bonding, wafer level, 3-D IC, 3-D integration.**

I. Introduction

THREE-DIMENSIONAL IC provides a promising solution to extend and get beyond the Moore's law (more than Moore) as the next generation semiconductor technology. It possesses lots of advantages including small form factor, high performance, low power consumption, potentially low cost, easy for high density heterogeneous integration, and could be widely used for product applications such as CIS, LED, MEMS, memory stacking, logic and memory stacking, and high performance chips stacking, etc. For realization, various 3-D integration platforms have been addressed and developed in the worldwide companies and research institutes [1]–[4]. The key technologies, including through-silicon via (TSV), thin wafer handling, wafer bonding and interconnection are necessary to carry out these 3-D platforms. Vertical interconnection by Cu TSV combination with Cu/Sn microjoint is an attractive option for 3-D integration [5]–[10]. However, this approach is usually limited by chip-to-chip (C2C) or chip-to-wafer (C2W) bonding scheme followed by underfill filling for reliability enhancement. Considering the mass production in future, a wafer-level 3-D integration platform with simplified process flow is essential to be developed to increase the through-put and lower the cost.

In this paper, a wafer-level 3-D integration scheme with Cu TSVs based on Cu/Sn microbump and BCB adhesive hybrid bonding is demonstrated. The microbumps are adopted for inter-wafer connection to achieve vertical interconnection with TSVs. The strength and reliability of stacked structures are effectively increased with the adhesive sealing around and serving reinforcement of mechanical stability to endure the severe wafer thinning and follow-up processes. With this 3-D integration scheme and bonding approach, there are no demands for thin wafer handling technique with carrier temporary bonding and de-bonding. It does not need to meet the challenge of ultra-fine gap underfill filling and flux cleaning. Therefore, the process flow could be simplified with cost reduction effectively. In addition, different from the high bonding temperature requirement on Cu–Cu thermo-compression bond, Cu/Sn and BCB hybrid bonding can be performed under 250°C with lower force, which decreases the induced thermo-stress and possible damage, and satisfies low thermal budget requirement on most devices. The structure design, complete process flow and conditions, assessment results of electrical performance and reliability of the 3-D integration scheme are disclosed in the paper.

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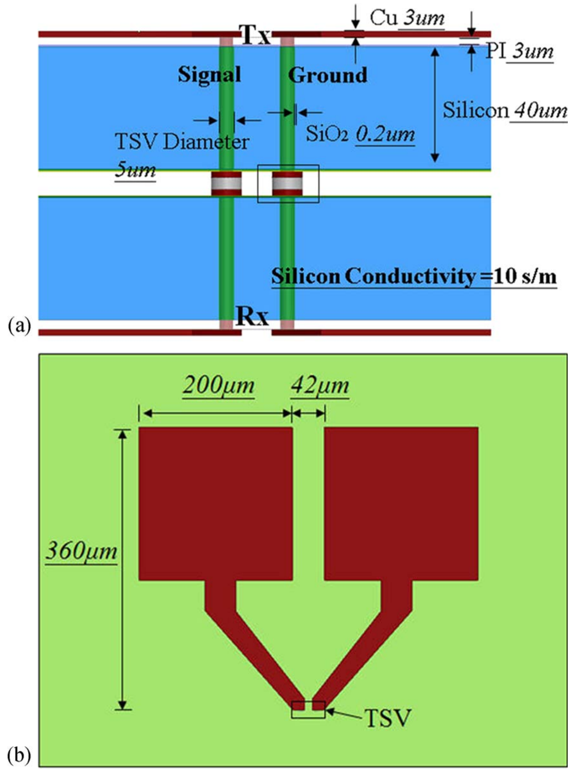


Fig. 1. Two-chip stack structure with vertical interconnect by Cu TSV and Cu/Sn microjoint for insertion loss simulation analysis: (a) side view, (b) top view.

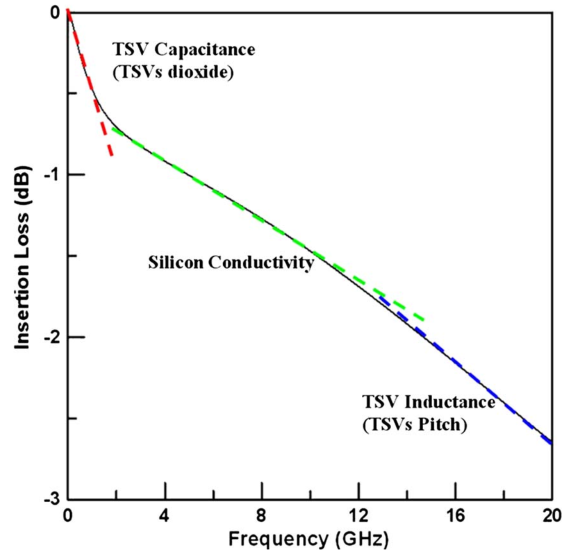


Fig. 2. TSV insertion loss behavior on different zone. (Pitch: 20 μm).

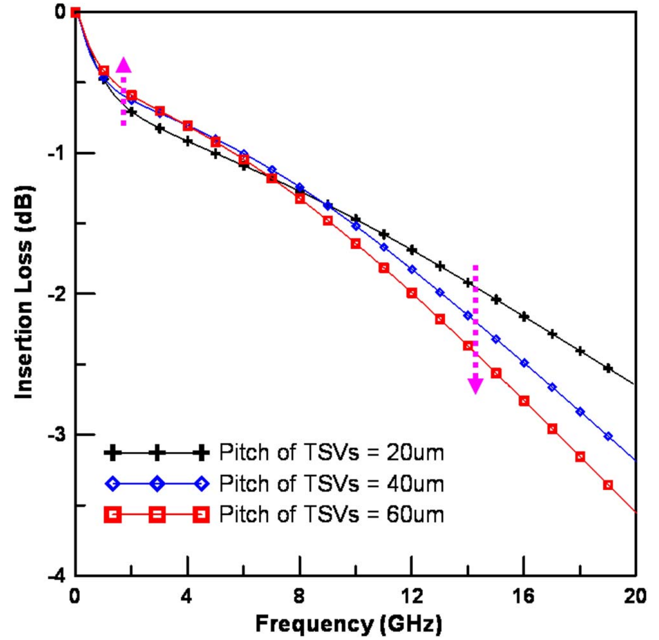


Fig. 3. Simulation result of TSV pitch effect on insertion loss (TSV pitch = 20 μm $\sim$ 60 μm).

II. Evaluation of Cu TSV and Microjoint Interconnect

Thin chip stacking with vertical interconnection by Cu TSV and Cu/Sn microjoint is one of the candidates for 3-D integration. To realize the signal transmission effects in high-speed digital signaling via TSV and microjoint interconnect in 3-D IC, the insertion loss of two-chip stack, as shown in Fig. 1, was evaluated with different TSV pitches, microbump diameters, and chip thicknesses. In this paper, 3-D field solver HFSS was used to simulate the stacked structure. The lump port was set between signal and ground, and the setting silicon size is 1 mm $\times$ 1 mm. The microbump Cu/Sn ratio is 2:3, with the setting resistivity $1.7 \times 10^{-8}\Omega$. m and $7 \times 10^{-7}\Omega$. m respectively for Cu and Sn.

A. TSV Insertion Loss Behavior on Different Zone

TSV has to be electrically isolated from the silicon substrate with a thin silicon dioxide film which causes a capacitive effect. Therefore, high-speed digital I/O signals suffer from the capacitive loading as well as the frequency-dependent loss from the lossy silicon substrate, which results in degradation of the eye opening and timing jitter in the high-speed digital system [11]. Fig. 2 presents TSV insertion loss behavior dominated by TSV capacitance, silicon conductivity, and TSV inductance, respectively in low, middle, and high frequency region. The silicon dioxide, silicon conductivity, and TSV pitch effect frequency range for insertion loss were studied previously [11], [12]. As the TSV thin silicon dioxide film thickness decreases, the insertion loss increases in low frequency region due to the capacitive effect between signal via and ground via increasing. As the silicon substrate conductivity increases, the insertion loss increases in middle frequency region because the resistance between signal via and ground via decreases. As the TSV pitch increases, the insertion loss increases in high frequency region.

B. Insertion Loss versus Pitch

Fig. 3 presents the insertion loss of the stacked structure shown in Fig. 1 with different TSV pitches. As the pitch decreases, the silicon substrate capacitance and conductance between the signal and ground TSVs increase, which results in the increased insertion loss [12]. Therefore, as the TSV pitch increases from 20 μm to 60 μm, the insertion loss improves in middle frequency region ranging from 1 GHz to 8 GHz

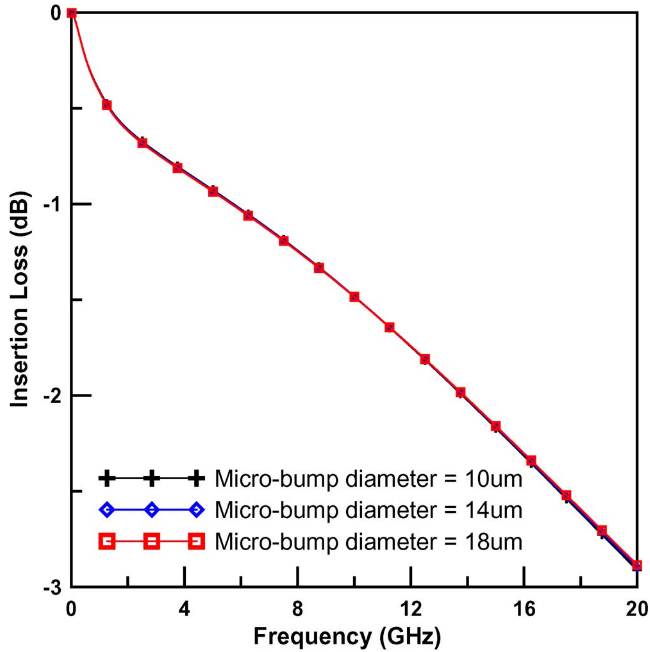


Fig. 4. Simulation result of microbump diameter effect on insertion loss (microbump diameter = 10 μm ~ 18 μm).

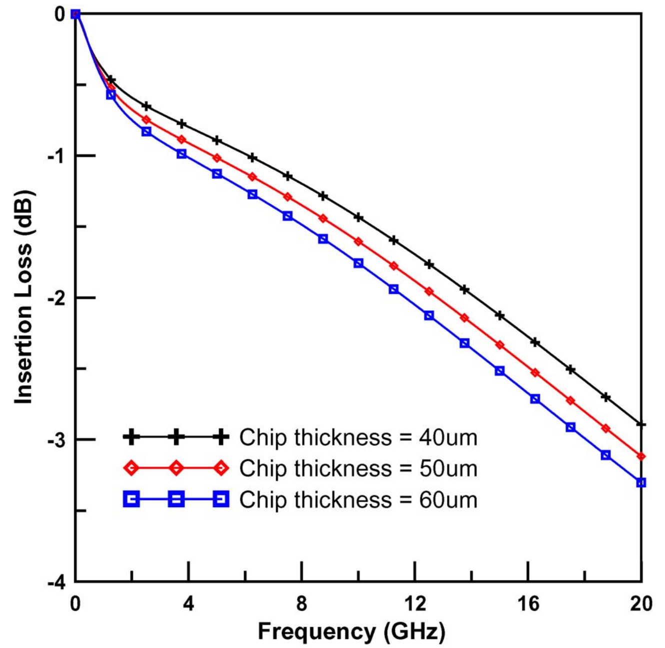


Fig. 5. Simulation result of chip thickness effect on insertion loss (chip thickness = 40μm ~ 60μm).

as shown in Fig. 3. However, as the pitch increases in high frequency region ranging from 8 GHz to 20 GHz, the insertion loss drops quickly due to the increase of TSV loop inductance. Therefore, the pitch of TSV is an important design parameter when system works on higher frequency.

C. Insertion Loss versus Microbump Dia. (Fixed TSV Pitch)

Microbump electrical characteristic affects the electrical performance of 3-D integration system. Fig. 4 shows the simulation result of microbump diameter effect on insertion loss. As the TSV pitch fixed (20 μm), although the microbump diameter increases, the insertion loss does not significantly improve because the microbump is surrounded by the lossless BCB other than the lossy silicon substrate. In addition, the fat and short structure of microbump would be the secondary reason as it is still very conductive.

D. Insertion Loss versus Chip Thickness

In 3-D integration scheme, chip/wafer thickness directly determines the TSV height which affects the TSV electrical performance in high-speed digital transmission. Fig. 5 shows the simulation result of chip thickness effect on insertion loss (microbump diameter: 10 μm, pitch: 20 μm). As the chip thickness increases, the height and impedance both increase. Therefore, the insertion loss increases. However, the insertion loss does not change significantly in low frequency region due to the silicon dioxide film thickness in TSV unchanged.

III. Structure Design and 3-D Integration Demonstration

In this paper, Cu TSVs based on Cu/Sn microbump and BCB adhesive hybrid bonding scheme was designed to demonstrate a wafer-level 3-D integration platform. Several kinds of TSV diameters with different microbump sizes and pitches were designed in the test vehicle. Fig. 6 shows the structure design and schematic process flow. Cu/Sn microbumps were fabricated on bottom wafer and Cu TSVs of top wafer, respectively, as shown in Fig. 6(a). In Fig. 6(b), BCB was subsequently spin-coated and lithographed to expose the microbumps and form the hybrid scheme. Fig. 6(c) shows that two wafers were then aligned and hybrid bonded at 250°C. After bonding, top wafer was thinned to expose TSVs and backside RDL formation with bottom wafer support, as shown in Fig. 6(d). If required, a third wafer (or more) can be further added to achieve multi-layer 3-D structures.

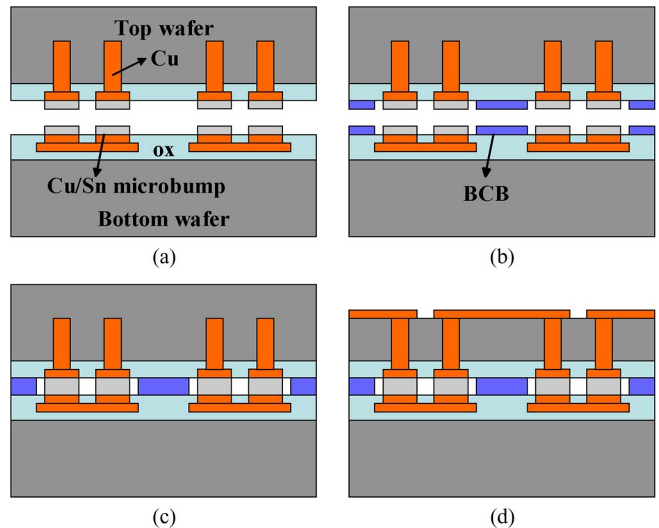
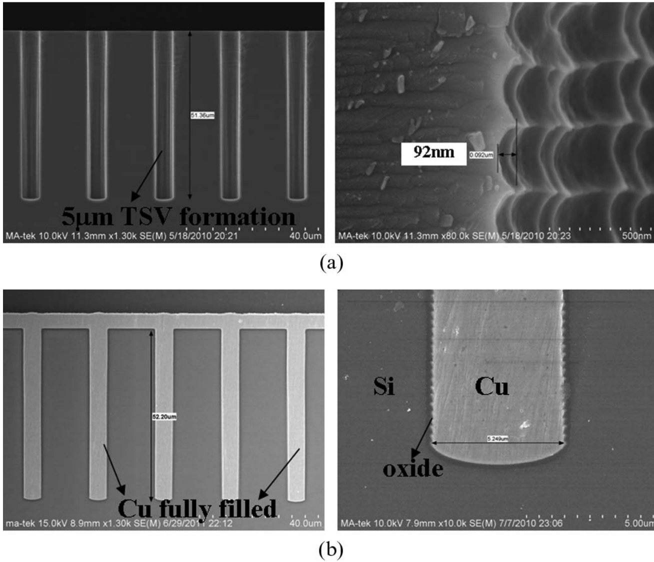


Fig. 6. Structure design and schematic process flow of wafer-level 3-D integration scheme. a) Cu/Sn microbump formation on top (with TSV) and bottom wafer; (b) BCB covering and patterning; (c) Hybrid bonding; (d) Thinning and backsides RDL.



(a)

(b)

Fig. 7. Fabrication of 5 μm size/50 μm depth TSV in 20 μm pitch performed by (a) DRIE formation with scallop less than 100 nm, and (b) followed by ECP-Cu filling without any void and seam inside.

Several key techniques have to be well developed and integrated to perform the 3-D integration scheme, including TSV interconnection, microbumping, hybrid bonding, wafer thinning and backside RDL formation. The section below discloses the process conditions and results in detail.

A. TSV Interconnection

By the definition of photoresist as etching mask, TSVs were formed by deep reactive ion etch (DRIE). The well-known Bosch process [13] was applied where SF_6 was used in etching cycle whereas C_4F_8 in passivation cycle to achieve anisotropic etch of silicon. With optimization of the alternative cycle time, the etch rate could be optimized with minimum sidewall scallop. Fig. 7(a) presents 5 μm size/50 μm depth TSV formation with scallop about 92 nm only. After DRIE, the SPS-200 and EKC chemicals were used to remove the etching mask and polymer generated during DRIE process. The silicon dioxide and TiN/Cu were subsequently deposited on the via surface as dielectric and barrier/seed layers, respectively. With the smaller sidewall scallop, it facilitates the continuity of the deposition layers and then smoothes the ECP-Cu filling process. TSV filling was performed by using Raider-M CFD3 plating tool from AMAT. Fig. 7(b) presents 5 μm size/50 μm depth TSV in 20 μm pitch fully filled with ECP-Cu without any void and seam inside. After TSV filling, the surface Cu overburden and TiN barrier were removed by chemical mechanical polishing (CMP) to complete the TSV exposure for front side interconnection.

B. Microbumping

In this research, Cu/Sn microjoints were employed for vertical interconnect between stacked wafers. Via in pad design was adopted and fine pitch microbumping technique was developed to integrate with TSV to achieve high density interconnection. After Cu pad/trace and oxide passivation formation, the Cu/Sn microbumps were fabricated on the pads by electroplating technique. An adequate barrier and seed layer thickness was applied to minimize the undercut after etching but keep good wafer-level plating uniformity. Fig. 8 demonstrates the Cu/Sn microbumps formation with 10 μm size in 20 μm pitch. With the precise control, the undercut less than 1 μm and bump height uniformity less than 10% could be achieved. In addition, good bumping uniformity ensures the follow-up wafer bonding uniformity.

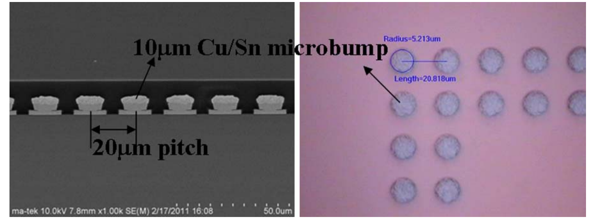
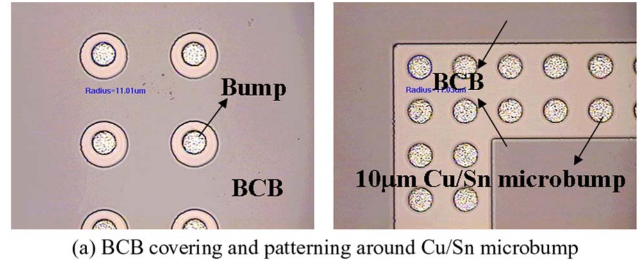
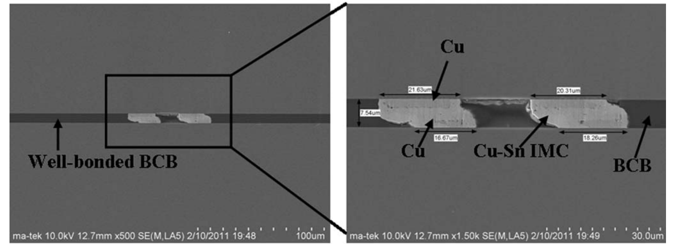


Fig. 8. Formation of 10 μm Cu/Sn microbump in 20 μm pitch.



(a) BCB covering and patterning around Cu/Sn microbump

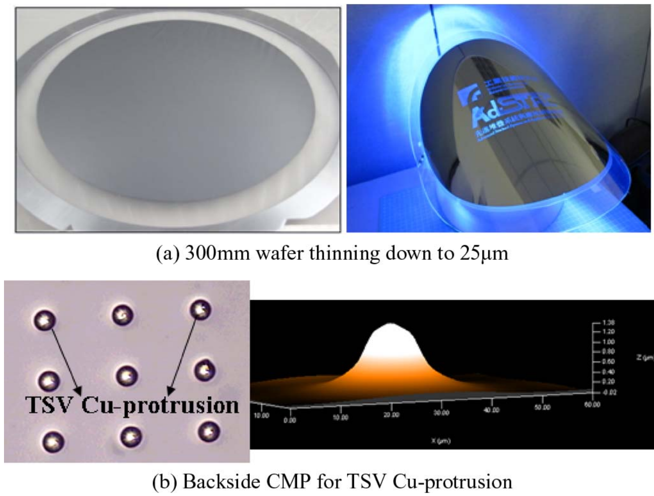


(b) Cu/Sn microbump and BCB hybrid bonding

Fig. 9. (a) BCB covering and patterning around Cu/Sn microbumps without residue on bumps; (b) Cu/Sn microbump and BCB hybrid bonding conditions were optimized to perform the bonding integrity.

C. Hybrid Bonding

As aforementioned, Cu/Sn microbump and BCB adhesive hybrid scheme was applied for wafer-to-wafer (W2W) bonding to achieve the intrinsic interconnection and adhesive sealing simultaneously. The photosensitive BCB with excellent mechanical resistance and bonding properties had been qualified to be compatible with solder bump (and even Cu–Cu) for hybrid integration, and could be performed by 250°C low temperature bonding [14]. After Cu/Sn microbump formation, BCB was spin-coated and UV-lithographed to expose the microbumps to form the hybrid scheme as Fig. 9(a) shows. Because both bump and adhesive are bonding media, the total thickness difference between them needs to be optimized to ensure the bonding integrity on both parts. In addition, due to BCB covering and patterning after bump formation, BCB residue on bump surface was observed and it induced the microjoint bonding failure. In



(a) 300mm wafer thinning down to 25μm

(b) Backside CMP for TSV Cu-protrusion

Fig. 10. (a) The demonstration of 300 mm wafer thinning down to 25 μm thickness; (b) Backside TSV Cu-protrusion image and profile.

the study, a post lithographic treatment was adopted to clean the bump surface to ensure metal intimate contact. Microbump with 5 μm thickness (3 μm Cu and 2 μm Sn) combination with 4 μm thick BCB was applied on one wafer side. Two wafers were aligned and hybrid bonded at 250°C using SUSS manual bonder. The misalignment may be up to several μm in manual mode. As the results shown in Fig. 9(b), 2 μm total thickness difference and an adequate surface treatment application realize the complete bonding performance. Both BCB and microjoint parts are well bonded. Sn metal is almost consumed and Cu_6Sn_5 IMC is observed. The interconnect joints are well protected with BCB perfect sealing around.

D. *Wafer Thinning and Backside RDL Formation*

Wafer thinning, TSV Cu-protrusion and backside RDL formation are the key technologies to perform the wafer-level 3-D interconnection after bonding/stacking. With coarse and fine grinding followed by CMP stress release treatment, 300 mm wafer thinning down to 25 μm thickness had been realized without any crack and chipping as Fig. 10(a) demonstrates. In this 3-D integration platform, the permanent bonded TSV wafer was thinned down to 40 μm with 2 μm TSV Cu-protrusion implemented by CMP. Fig. 10(b) shows the Cu-protrusion image and profile. The thinned TSV wafer was sequentially spin-coated by PI passivation, and lithographed to expose TSV again for backside RDL interconnection. With the bottom wafer support, the backside processes could be implemented smoothly and completed.

Based on the successful development and integration of key technologies, a complete 3-D integration scheme has been achieved as shown in Fig. 11. Herein the TSV wafer was fabricated first, stacked on the bottom wafer using Cu/Sn microbump and BCB hybrid bonding with excellent bonding integrity and uniformity, thinned down to 40 μm without any crack and chipping, and completed with backside RDL formation. Four test vehicles were designed to investigate the electrical performances of 3-D integration. Fig. 12 presents the cross-section image of one design in the 3-D integration wafer. 5 μm TSV,

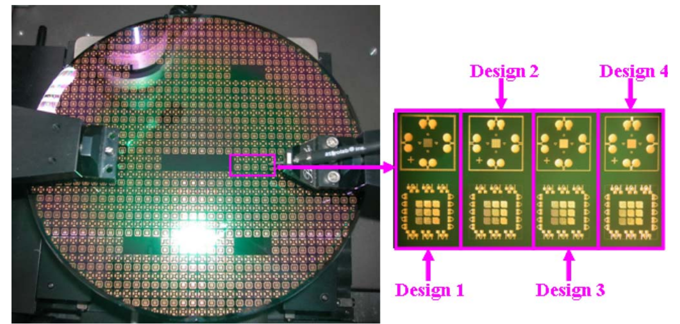


Fig. 11. Image of a complete 3-D integration wafer with four kinds of designs.

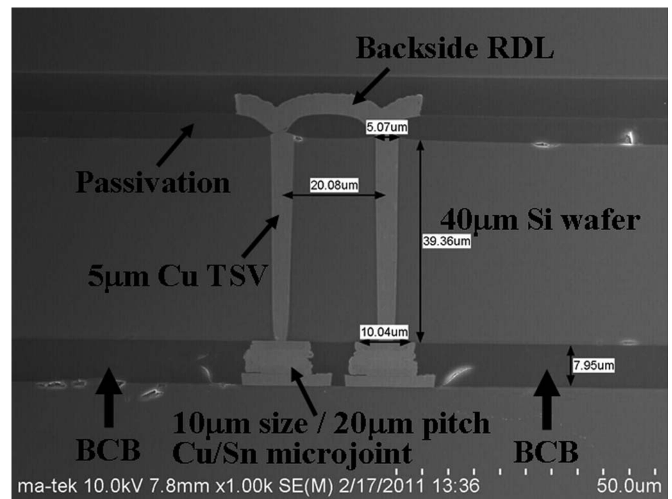


Fig. 12. Cross-sectional SEM image of one design in the 3-D integration wafer.

10 μm microbump, 20 μm pitch, 40 μm thin wafer, and 250 °C low temperature W2W hybrid bonding have been successfully integrated in this 3-D integration scheme.

IV. Electrical Performance and Reliability

Electrical characteristics of the 3-D integration scheme were evaluated through the bond chain structures. The linear characteristic of total resistances and number of via chains with a series of Cu TSVs and Cu/Sn microjoints interconnection indicates excellent bonding integrity and electrical performance. Fig. 13 shows characteristics of total resistances of via chains and locations on wafer. The deviation below 20% indicates good integration performance and uniformity across whole wafer. The “total daisy chain resistance” equals “number of via chain” multiply “single TSV and microjoint resistance” plus “trace resistance” plus “probe contact resistance”. Herein the average of “total daisy chain resistance” in Fig. 13 is about 5.3 Ω with 100 via chains connected in series. The Kelvin structure was designed to investigate the characteristic of single TSV and microjoint interconnect, and the measurement results show the average of “single TSV and microjoint resistance” is about 45 mΩ. Fig. 14 shows characteristics of voltage and current on one 5 μm Cu TSV and 10 μm Cu/Sn microjoint under multiple current stressing. The characteristic curves are almost the same, which implies excellent electrical performance and stability

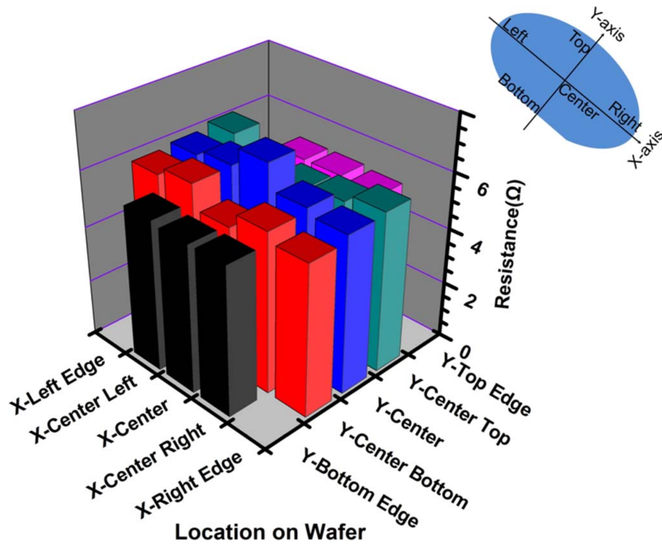


Fig. 13. Characteristics of total resistances of via chains and locations on wafer.

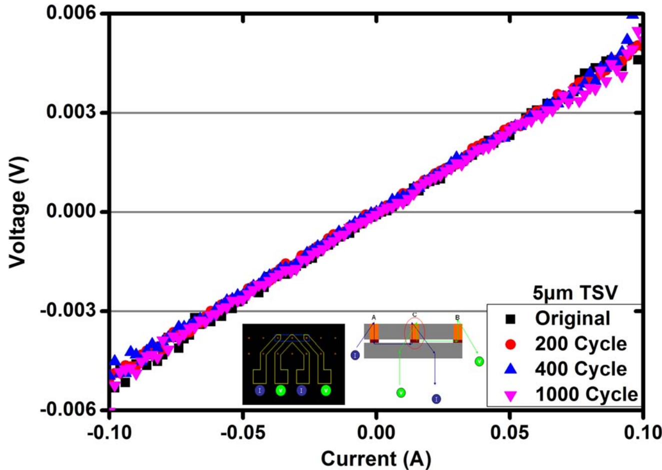


Fig. 14. Characteristics of voltage and current on one 5 μm Cu TSV and 10 μm Cu/Sn microjoint under multiple current stressing.

even after 1000 cycles of current stressing. In addition, via chains were evaluated by multiple current stressing, showing excellent stability as Fig. 14 presents. It also indicates the developed 3-D integration scheme possesses excellent stability and reliability.

V. Three-Dimensional Memory Demonstration

With the excellent electrical performance and reliability, the developed 3-D integration scheme could be applied for many applications. One of the potential applications is memory stacking as Fig. 15 demonstrates. Fig. 15(a) presents the proposed Semi-Master–Slave (SMS) with design of self-timed differential-TSV (STDT) signal transfer [15]. Fig. 15(b) shows the characteristics of TSV wire delay. The delay significantly decreases with STDT design. Fig. 15(c) presents the cross-sectional SEM image and the schematic diagram of two-layer 3-D SRAM stacking. New 3-D SRAM circuit design with TSV and microbump interconnect realizes low power, high capacity and high-speed wide I/O applications.

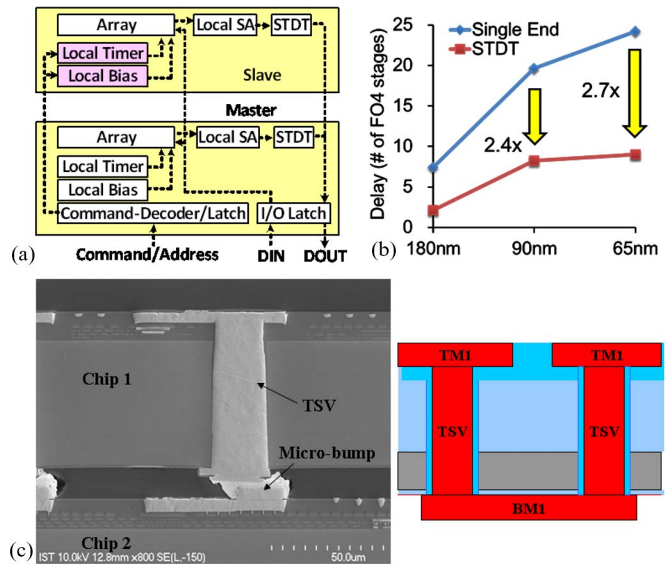


Fig. 15. Three-Dimensional SRAM demonstration: (a) The proposed Semi-Master–Slave (SMS); (b) TSV wire delay characterization; (c) The cross-sectional SEM image and schematic diagram of 3-D SRAM stacking.

VI. Conclusion

The insertion loss of two-chip stack with vertical interconnect by Cu TSV and Cu/Sn microjoint was evaluated with TSV pitch, microbump diameter and chip thickness effect. As the TSV pitch increases, the insertion loss improves in middle frequency region but turns to become worse and drops quickly in high frequency region due to the loop inductance increasing. The insertion loss does not improve significantly as the microbump diameter increasing because the microbump is surrounded by the lossless BCB other than the lossy silicon substrate, and the fat and short structure of microbump is still very conductive. As chip thickness increases, the insertion loss increases as well due to the TSV impedance increases. The TSV pitch, microbump resistance and chip thickness are the important parameters when system working on higher bandwidth.

A wafer-level 3-D integration scheme with Cu TSVs based on Cu/Sn microbump and BCB adhesive hybrid bonding was demonstrated. Key techniques including TSV interconnection, microbumping, hybrid bonding, wafer thinning and backside RDL formation were well developed and integrated to realize it. 5 μm TSV, 10 μm microbump, 20 μm pitch, 40 μm thin wafer, and 250°C low temperature W2W hybrid bonding have been successfully integrated in the 3-D integration scheme. The 3-D integration scheme, with excellent electrical performance and reliability, is potentially to be applied for 3-D memory application.

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