Experimental Verification of RF Stress Effect on Cascode Class-E PA Performance and Reliability

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***Abstract*—A cascode class-E power amplifier (PA) operating at 5.2 GHz has been designed using Advanced Design System simulation. RF circuit performances such as output power and power-added efficiency before and after RF stress have been experimentally investigated. The measured output power, power-added efficiency, and linearity after high-input-power RF stress at elevated supply voltage show significant circuit degradations. The impact of hot-carrier injection and gate oxide soft breakdown on cascode class-E PA reliability is discussed.**

***Index Terms*—Cascode class E, gate oxide breakdown, output power, power amplifier (PA), power efficiency, reliability.**

I. Introduction

THE advancement in CMOS technology for high-frequency applications has made it a natural choice for integrated low-cost RF power amplifiers (PAs) for wireless communications ICs. Class-E PA topology has become popular due to its high power efficiency [1] and, therefore, a good candidate for low-cost high-integration portable communication systems such as cell phones, wireless local area networks, wireless sensor networks, global positioning systems, and Bluetooth applications.

A class-E amplifier with a shunt capacitor was introduced by Sokal and Sokal [2] and was examined by Raab in an analysis of idealized operation [3]. The active transistor in the class-E PA is used as a switch. The voltage and current waveforms are shaped by the LC tuning network such that they do not overlap, producing an ideal power efficiency value of 100%.

Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the deep submicrometer-to-nanometer regime have resulted in major reliability issues, including gate oxide breakdown [4] and channel hot-electron degradation [5], [6]. Class-E PA is very vulnerable to oxide stress because its drain voltage can approach more than three times of supply voltage V_{DD} ideally. To ensure the reliability of class-E PA operation, V_{DD} is conservatively selected to a lower value. However, low V_{DD} reduces a PA's output power and power efficiency.

A cascode topology is adopted in a class-E PA to divide the output voltage and decrease gate oxide stress effect [7]–[9]. The cascode topology is better than the noncascode structure due to reduced drain–gate voltage stress on the output transistor. In addition, a thick oxide of the cascode transistor may be used to alleviate oxide stress at the expense of reduced output voltage swing [10]. Note that prior publications [7]–[10] on class-E PA reliability issues focused on gate oxide stress, not on channel hot-electron injection. This motivates us to evaluate hot-electron effect on class-E PA degradations using experimental data and a mixed-mode device and circuit simulation.

In this paper, a cascode class-E PA is designed using an Advanced Design System simulation (ADS) simulation [11]. Measured PA performances after RF stress are analyzed. Section II illustrates the design of a cascode class-E PA operating at 5.2 GHz. The circuit performances, after the postlayout simulation, are demonstrated.

Section III presents RF stress experiments and class-E PA performance degradations after high input power and increased V_{DD} stress. Section IV discusses the reliability of cascode class-E PA subjected to hot-electron effect through the examination of impact ionization and lattice heating using the mixed-mode device and circuit simulation. Finally, conclusion is given in Section V.

II. Design of a Cascode Class-E PA

To evaluate the class-E PA reliability by experiments, a cascode class-E PA is designed for fabrication Fig. 1 shows the circuit schematics of a cascode class-E PA.

Using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm mixed-signal CMOS technology, the class-E PA designed at 5.2 GHz is evaluated in the ADS simulation. Multifinger transistors with n-channel length of 0.18 μm are

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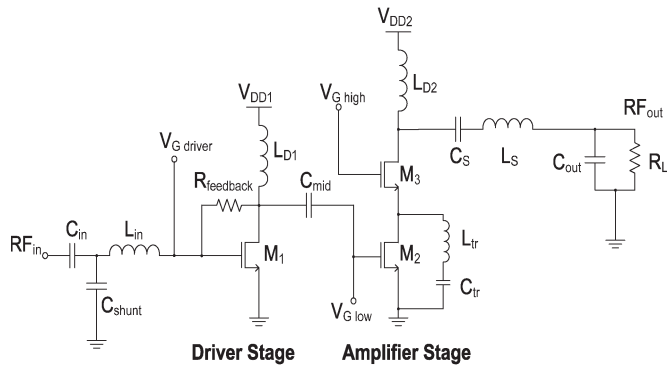

Fig. 1. Schematic of a cascode class-E PA.

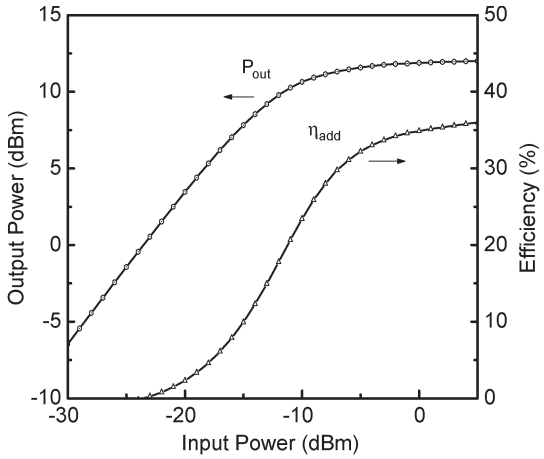

Fig. 2. Output power and power-added efficiency versus input power after postlayout simulation.

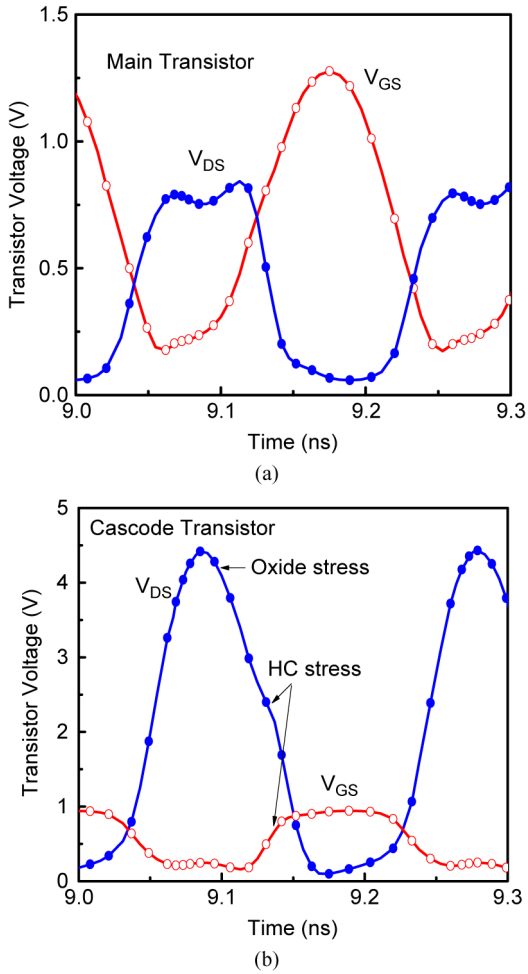

Fig. 3. (a) Simulated gate–source and drain–source voltages of the main transistor. In this simulation, $P_{\rm in} = 0$ dBm and $V_{DD2} = 2.4$ V. (b) Simulated gate–source and drain–source voltages of the cascode transistor. In this simulation, $P_{\rm in} = 0$ dBm and $V_{DD2} = 2.4$ V.

used. Driver transistor M_1 has the channel width of 256 μm. Main transistor M_2 and cascode transistor M_3 have the channel width of 512 and 544 μm, respectively. The dc supply voltage V_{DD1} for the driver stage is set at 1 V. The supply voltage V_{DD2} for the main amplifier is selected to be at 2.4 V. To reduce power consumption, the gate of M_1 is biased at 0.1 V (class-C mode of biasing). The gate dc voltages of M_2 and M_3 are at 0.7 and 1 V, respectively. The spiral inductor and capacitor values used in this design are $L_{\rm in} = 3.61$ nH, $L_{D1} = 1.47$ nH, $L_{D2} = 4.56$ nH, $L_{\rm tr} = 0.27$ nH, $L_S = 3.61$ nH, $C_{\rm in} = 398$ fF, $C_{\rm shunt} = 1.79$ pF, $C_{\rm mid} = 1.68$ pF, $C_{\rm tr} = 804$ fF, $C_S = 398$ fF, and $C_{\rm OUT} = 35.6$ fF. Feedback resistance $R_{\rm feedback}$ is 600 Ω.

The cascode class-E PA was laid out using Cadence Virtuoso software [12], followed by successful Calibre DRC for design rule checking and LVS for layout versus schematic verification. The layout parasitic effects were extracted using the ADS Momentum (electromagnetic) simulation. The postlayout simulation result of output power and power-added efficiency (ηadd) as a function of input power is shown in Fig. 2.

The gate–source and drain–source voltages as a function of time for the cascode and main transistors are shown in Fig. 3 to examine the electrical stress effect on this cascode class-E design. As shown in Fig. 3, the cascode transistor bears more voltage stress at the drain of M_3 than that of main transistor M_2. At high input power, the cascode transistor could suffer hot-electron effect when gate–source and drain–source voltages are high during switching transient [see Fig. 3(b)].

III. RF Stress Experiments

A silicon chip of the designed PA was fabricated using TSMC 0.18-μm mixed-signal CMOS technology. The silicon chip is shown in Fig. 4, and its size is 820 × 887 μm^2. In this figure, spiral inductors, capacitors, transistors, ground–signal–ground RF input and output pads, dc supply voltage pads, and gate bias pads are displayed.

The PA's performances before and after RF stress are measured. The measurement was performed at room temperature. The PA was then stressed with an RF input power value of 0 dBm and different V_{DD2} stress levels at 3.5, 4, or 4.5 V for 10 h. After continuous RF and elevated dc stresses, the RF parameters were measured again to compare with the experimental data obtained at the fresh circuit condition. For the circuit at the normal operation, dc biases of $V_{G1} = 0.1$ V, $V_{G2} = 0.7$ V, $V_{DD1} = 1$ V, and $V_{DD2} = 2.4$ V were used.

Fig. 5 shows the measured small-signal gain S_{21} versus frequency as a function of stress conditions. In Fig. 5, the solid

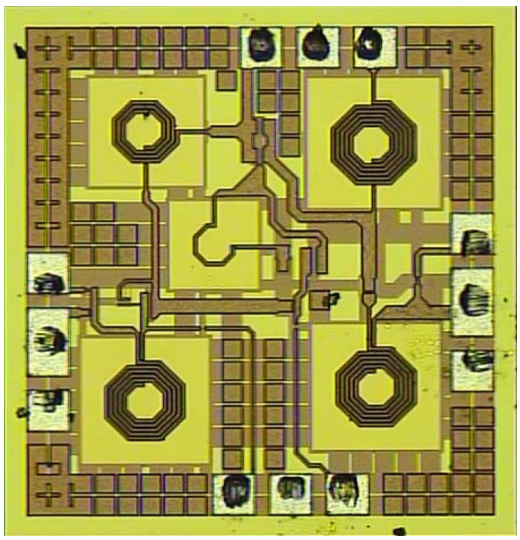

Fig. 4. Chip view of the cascode class-E PA used for RF stress and measurement.

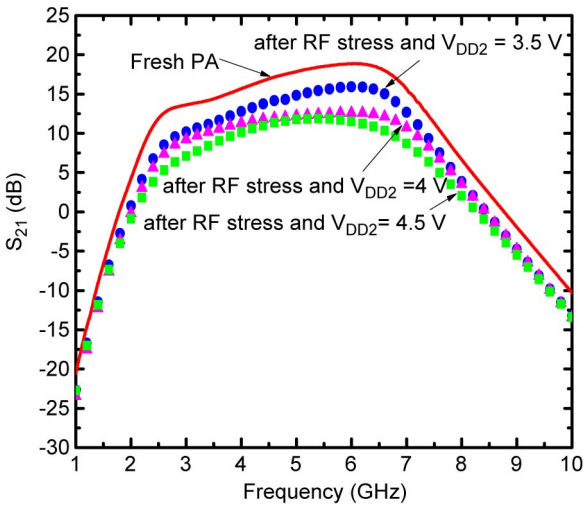

Fig. 5. Measured S_{21} versus frequency before and after RF stress. During the RF stress, $P_{\rm in}$ is at 0 dBm and V_{DD2} was kept at 3.5, 4, or 4.5 V.

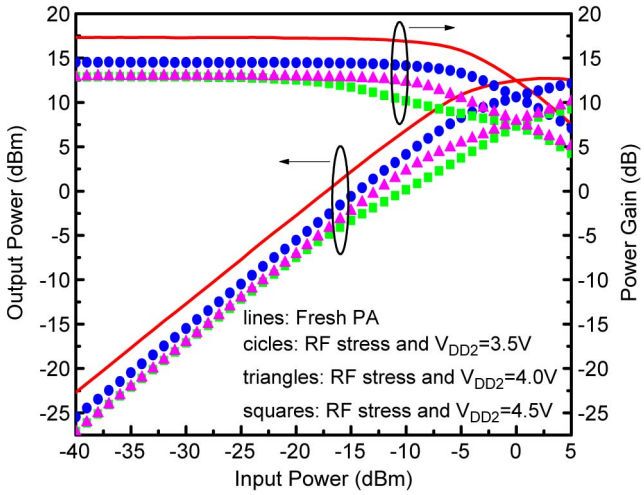

Fig. 6. Measured output power and power gain versus input power before and after RF stress. During this RF stress, $P_{\rm in}$ is at 0 dBm and V_{DD2} was kept at 3.5, 4, or 4.5 V.

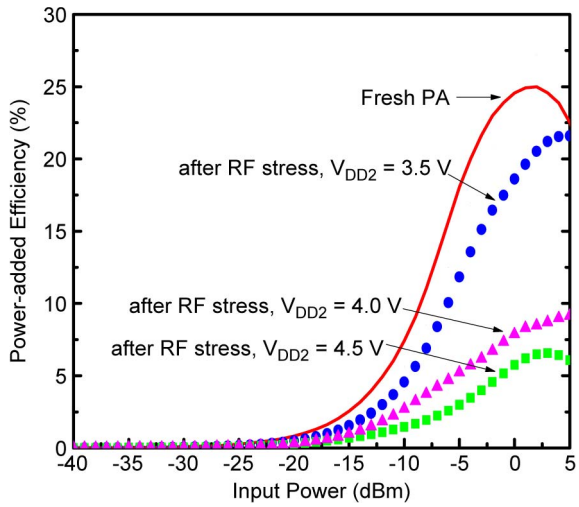

Fig. 7. Measured power-added efficiency versus input power before and after RF stress at 5.2 GHz. During this RF stress, $P_{\rm in}$ is at 0 dBm and V_{DD2} was kept at 3.5, 4, or 4.5 V.

line represents the fresh circuit result, the circles represent the PA's experimental data after 10 h of RF stress at $V_{DD2} = 3.5$ V, the triangles represent the data after 10 h of RF stress at $V_{DD2} = 4$ V, and the squares represent the measured result after 10 h of RF stress at $V_{DD2} = 4.5$ V. As shown in Fig. 5, the larger the elevated stress at high V_{DD2}, the larger the S_{21} degradation over a wide range of frequencies.

At 5.2 GHz, the measured output power and power gain are plotted in Fig. 6. The output power increases with input power and reaches a saturated output power value at high input power, thus making the power gain decrease at high input power. Both the output power and power gain decrease after RF stress, particularly when the V_{DD2} stress level is increased. The degradations of RF circuit performances are attributed to hot-electron effect on the output transistor. More detailed physical explanations are given in Section IV.

The measured power-added efficiency is illustrated in Fig. 7. Power-added efficiency increases with input power, reaches saturation, and then decreases with input power due to reduced output power and increased dc power dissipation at very high input power. The power-added efficiency is defined as (RF output power–RF input power)/total dc power dissipation including the power stage's and driver stage's. Note that the power-added efficiency is lower than the drain efficiency because of additional power dissipation from the driver stage. At 5.2 GHz, the peak power-added efficiency of the fresh PA approaches 25% (a somewhat lower value than expected due to layout parasitic effect and additional dc power dissipation in the driver stage). After RF stress, the peak power efficiency significantly decreases, particularly when the V_{DD2} stress level is high.

Table I lists the small-signal gain S_{21} at 5.2 GHz, output power at the input power of 0 dBm, power gain (po/pi) at the input power of -20 dBm, and maximum power-added efficiency before and after RF stress. Their normalized parameter shifts such as $\Delta S_{21}/S_{21}$, $\Delta p_o/p_o$, $\Delta(p_o/p_i)/(p_o/p_i)$, and

TABLE I
RF PARAMETER DEGRADATIONS

RF parameters	S_{21} @5.2 GHZ	p_o@ p_i=0dBm	p_o@ p_i=0dBm	peak η_{add}
Fresh	18.2 dB	12.5 dBm	17.3 dB	25%
After RF stress[1]	15.2 dB	10.6 dBm	14.5 dB	21.6%
After RF stress[2]	12.3 dB	7.9 dBm	12.9 dB	9.1%
After RF stress[3]	11.9 dB	7.3 dBm	12.5 dB	6.6%
Change[1]	-16.5%	-15.2%	-16.2%	-13.6%
Change[2]	-32.4%	-36.8%	-25.4%	-63.6%
Change[3]	-34.6%	-41.6%	-27.7%	-73.6%

[1] RF stress at p_i = 0 dBm and V_{DD2} = 3.5V for 10 hours
[2] RF stress at p_i = 0 dBm and V_{DD2} = 4.0V for 10 hours
[3] RF stress at p_i = 0 dBm and V_{DD2} = 4.5V for 10 hours

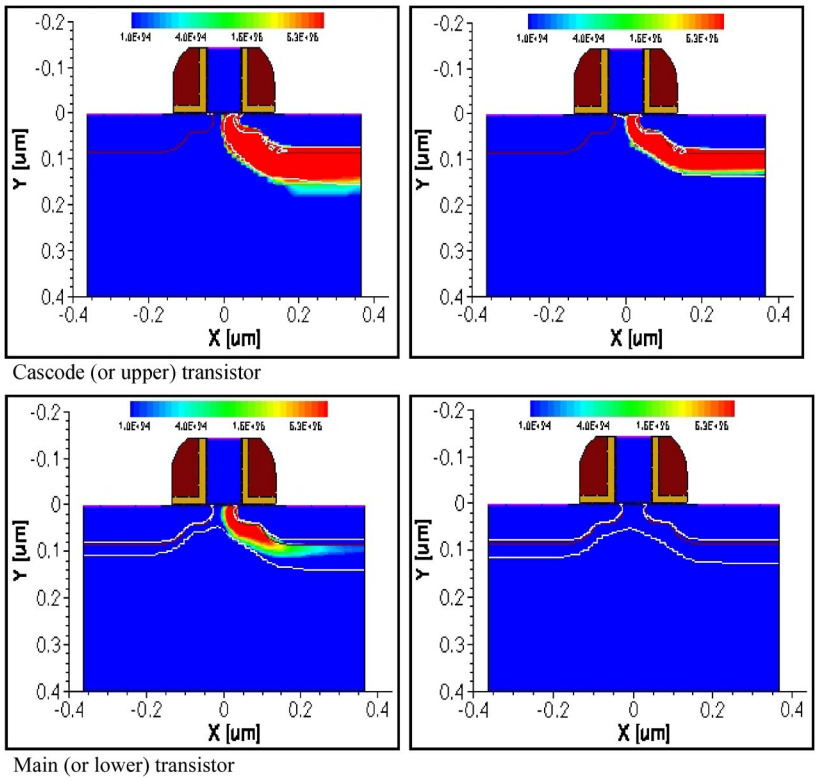

Fig. 8. Measured S_{21} versus frequency before and after RF stress. During the RF stress, $P_{\rm in}$ is at 0 dBm and V_{DD2} was kept at 3.5, 4, or 4.5 V.

$\Delta\eta_{\rm add}/\eta_{\rm add} \times 100\%$ from the fresh condition are also shown in Table I.

IV. PHYSICAL INSIGHT THROUGH THE MIXED-MODE DEVICE AND CIRCUIT SIMULATION

To evaluate the physical insight of hot-electron effect in the cascode PA, the Sentaurus TCAD software is used [13] and the class-E amplifier stage of the cascode PA in Fig. 1 is simulated. It is worth pointing out that the mixed-mode device and circuit simulation provides the examination of device physical insight under the practical circuit operation condition. Fig. 8 shows impact ionization rates for the cascode and main transistors with increased supply voltage $V_{DD2} = 3.5$ V for accelerated aging. As shown in Fig. 8, the impact ionization rates of the cascode transistor are much higher than those of the main transistor due to higher electric field at the drain of the cascode transistor. Larger drain–source voltage also makes impact ionization rates at the peak of output voltage transient (see left figure) higher than those during output switching (see right figure), as shown in Fig. 8. High impact ionization rates near the drain of a MOS transistor ($\sim 6.3 \times 10^{26}$ /cm^3/s) suggest that a large amount of hot electrons may inject into the gate of the MOSFET. Some hot electrons could be trapped within the oxide without reaching the gate contact. The accumulated trapped electron charges over a period of time increase the threshold voltage of the MOSFET. In addition, the interfacial layer between the SiO_2 and Si interface near the drain region may be damaged or degraded by the channel hot electrons. Thus, the effective electron mobility of the MOSFET decreases. Consequently, the drain current and transconductance of the MOSFET decrease. The reduction in drain current could decrease the output power and efficiency of the PA, as demonstrated by the experimental data in Figs. 6 and 7.

Fig. 9 displays the lattice temperature of the cascode and main transistors. In the Sentaurus simulation, Thermodynamic,

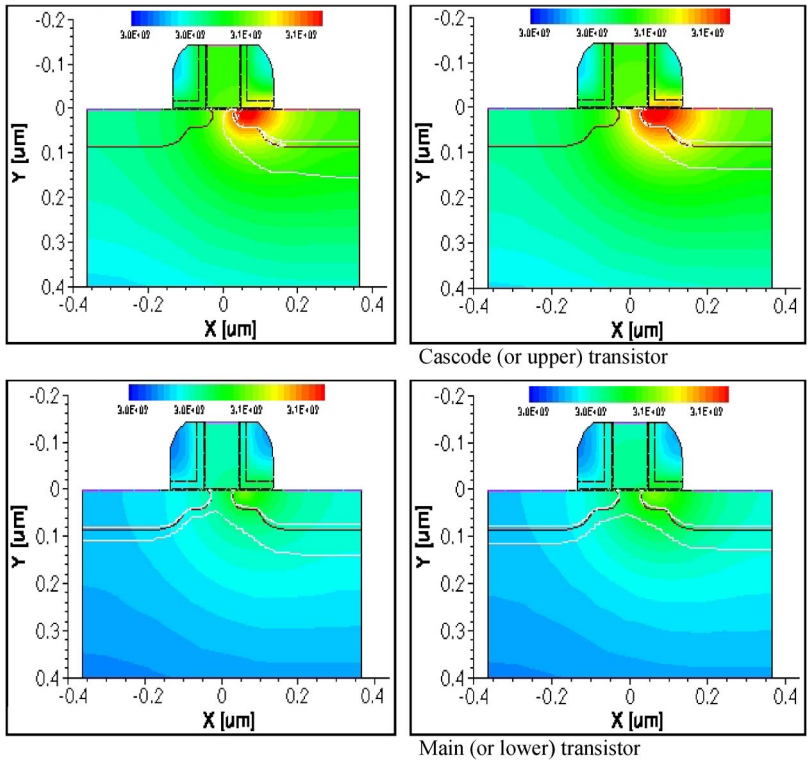

Fig. 9. Lattice temperature of (upper plots) the cascode transistor and (lower plots) the main transistor at (left figures) the maximum and (right figures) middle of the output voltage transient. In this mixed-mode device and circuit simulation, $V_{DD2} = 3.5$ V.

Thermode, RecGenHeat, and AnalyticTEP models are used to account for lattice heating. The thermodynamic model extends the drift–diffusion approach to account for electrothermal effects. A Thermode is a boundary where the Dirichlet boundary condition is set for the lattice. RecGenHeat includes generation–recombination heat sources. AnalyticTEP gives analytical expression for thermoelectric power. The substrate of the nMOS is set to be at 300 K. In Fig. 9, the cascode transistor has a higher peak lattice temperature ($\sim$310 K) than that in the main transistor because of larger drain–source voltage and power dissipation in the cascode transistor. The self-heating effect is enhanced during output voltage switching (see the right figures in Fig. 9) because of relatively high drain–source voltage and high drain current simultaneously. High temperature rise resulting from lattice self-heating could further reduce the drain current of the PA. Consequently, the output power and power-added efficiency of the PA degrade even more due to lattice heating. Note that it is well known that the class-E PA is vulnerable to the gate oxide breakdown due to very high drain–gate field stress. In this paper, however, we have demonstrated the experimental data in Section III that the cascode class-E PA is degraded by hot-electron effect during high output voltage switching. The mixed-mode device and circuit simulation of high impact ionization rates for the cascode transistor here supports the experimental finding of the PA degradation subjected to dc supply voltage for 10 h of continued RF stress at the input power of 0 dBm. Impact ionization leads to the formation of electron–hole pairs, i.e., electrons can be trapped in the gate oxide, whereas holes can generate interface states. Trapped electrons increase the threshold voltage of the n-channel MOSFET, whereas interface states may degrade the effective channel electron mobility. For the PA performance degradation, threshold voltage shift is more important than mobility degradation [14]. Note that high-input-power RF stress could result in more degradation in hot-electron effect than that under dc stress [15].

Additional mixed-mode simulation at RF stress under $V_{DD2} = 4.5$ V condition indicates that the peak impact ionization rates increase to 6.3×10^{27} /cm^3/s and the maximum lattice temperature of the cascade transistor is about 320 K. This suggests that the hot-electron effect and lattice heating are enhanced resulting from a higher drain electric field when V_{DD2} is at 4.5 V. High temperature from lattice heating, however, could reduce the hot-electron effect compared to that without self-heating [16]. On the other hand, high temperature enhances gate oxide breakdown, which is a strong function of temperature and electric field [17]. In our stress experiments, however, no noticeable increase in gate leakage current was detected when V_{DD2} was stressed at 3.5, 4, and 4.5 V. This suggests that no transistor oxide hard breakdown occurred since hard breakdown typically results in a sudden surge of gate current [18], [19] and could collapse RF performances. In addition, the ADS circuit simulation indicates that the peak drain–gate voltage of the cascode transistor with the oxide thickness of 4.08 nm results in a smaller electric field than the critical field for oxide breakdown [20]. The oxide under this high RF and elevated dc stresses at $V_{DD2} = 4.5$ V may experience some kind of soft breakdown [20], which deteriorates the PA circuit performances further. Soft breakdown increases the gate leakage current noise due to formulation of random defects and conducting path within the oxide [21]. After soft breakdown, the nMOS transistor's threshold voltage is increased [22], [23]

due to more trapped charge or defect density in the oxide. The increase in threshold voltage causes a decrease in drain current. Consequently, the PA's output power and power efficiency decrease after soft breakdown (to the first order, $\Delta P_o/P_o$ is proportional to $\Delta I_D/I_D$ [14]).

V. Conclusion

A cascode class-E PA at 5.2 GHz has been designed and fabricated. A mixed-mode device and circuit simulation is used to examine impact ionization rates and lattice heating of the cascode and main transistors in the circuit environment. The cascode transistor suffers more impact ionization and self-heating than the main transistor. The measured PA circuit performances after RF stress at different elevated V_{DD2} conditions are examined and compared with the experimental data obtained from the fresh circuit condition. The measured power gain, output power, power-added efficiency, and linearity are degraded after RF and increased dc stresses. The circuit performance degradations are larger at high V_{DD2} stress level. Hot-electron effect seems to be the dominant reliability mechanism for the degradation of cascode class-E PA evaluated at high input power and elevated supply voltage stress for 10 h. By increasing the cascode transistor's supply voltage from 3.5 to 4.5 V at high-input-power RF stress, soft breakdown may contribute additional degradation to the output power and power efficiency of the cascode class-E PA.

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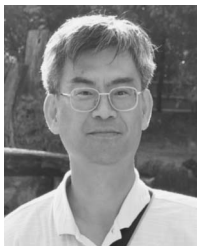

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