Characterization of SOA in Time Domain and the Improvement Techniques for Using in High-Voltage Integrated Circuits

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***Abstract*—Safe operating area (SOA) in power semiconductors is one of the most important factors affecting device reliability. The SOA region of power MOSFETs must be well characterized for using in circuit design to meet the specification of applications, particularly including the time domain of circuit operations. In this paper, the characterization of SOA in the time domain is performed with the experimental measurement on silicon devices, and the useful techniques to improve SOA of power MOSFETs for using in high-voltage integrated circuits are overviewed.**

***Index Terms*—Electrical safe operating area (SOA) (eSOA), power MOSFETs, SOA, snapback, thermal SOA (tSOA).**

I. Introduction

HIGH-VOLTAGE (HV) and high current operations are common requirements for semiconductor devices in power applications. To sustain the high operating voltage ($V_{\rm CC}$), sufficient device breakdown voltage ($BV_{\rm DSS}$) is a must for power semiconductors. To minimize the power consumption over a switching transistor, device turn-on resistance per unit area, i.e., the specific on-resistance $R_{\rm SP}$, is another important factor for the development of power devices. Safe operating area (SOA), as the third factor to meet the HV and high current operating requirements, defines the I–V boundary in which a power transistor can safely switch. These three factors, $BV_{\rm DSS}$, $R_{\rm SP}$, and SOA, are therefore known as the design triangle of power semiconductor devices as shown in Fig. 1[1].

Among power MOS field effect transistors (MOSFETs), lateral DMOS (LDMOS) devices have been used a lot because LDMOS have device cross-sections that are easier to be integrated into processes. Various DMOS structures featuring advantages in different aspects have also been devised. For example, a quasi-vertical trench DMOS integrated into a planar process can exhibit a better $R_{\rm SP}$ performance than its planar counterpart [2].

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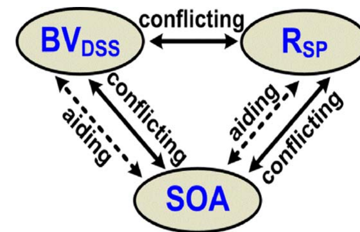

Fig. 1. Design triangle of power semiconductor devices (redrawn after [1]).

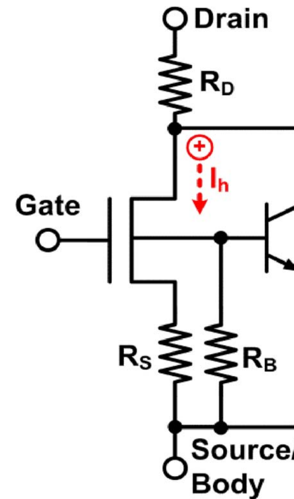

Fig. 2. Equivalent circuit model of a HV NMOS, shown with the parasitic bipolar junction transistor (BJT) in the device structure.

In this paper, the characterization of SOA in time domain and the useful techniques for SOA improvement of power MOSFETs are presented with the experimental data measured from silicon devices. This paper mainly focuses on LDMOS devices as they are popular devices in most power technologies. Results from this paper will be very useful for the designers to well adjust their designs to achieve safe operations of the power integrated circuits for field applications.

II. Physical Limitation of SOA

The physical limitation of SOA in a power MOSFET lies in the triggering of intrinsic bipolar junction transistors (BJTs) [3]. The equivalent circuit model of a HV NMOS is shown in Fig. 2. $R_{\rm D}$, $R_{\rm S}$, and $R_{\rm B}$ are, respectively drain, source, and body (parasitic) resistors of the HV NMOS; and the $I_{\rm h}$ is the hole current that can forward bias the BJT base–emitter junction

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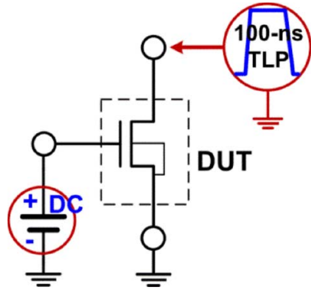

Fig. 3. Test setup for eSOA measurement by 100-ns TLP pulses.

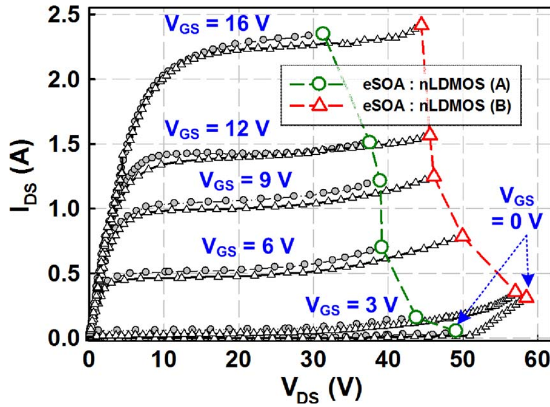

Fig. 4. Measured eSOA boundaries of two nLDMOS transistors by 100-ns TLP pulses.

through R_{B} to trigger on the intrinsic NPN BJT. Major sources of the current I_{h} include avalanche-generated holes (I_{AV}) and thermal generation (I_{TG}) due to device self-heating, which can be expressed as

$$I_h = I_{\mathrm{AV}} + I_{\mathrm{TG}}. \tag{1}$$

In (1), I_{AV} is a function of the drain–source current I_{DS} and avalanche multiplication factor M [3]. To minimize the effect of device self-heating and to estimate the impact of I_{AV} to SOA, device under tests (DUTs) are usually stressed by the pulses with a short pulse width. Such an electrical SOA (eSOA) boundary is important when thermal effect is not strongly involved during operation. For example, small devices that benefit from good lateral thermal spreading [1]. A 50-Ω transmission line pulsing (TLP) system that delivers square pulses with an 100-ns pulse width is usually adopted for the measurement of eSOA [1], [4]. The setup of eSOA measurement is shown in Fig. 3, and the TLP-measured eSOA boundaries of two 24-V n-channel lateral DMOS (nLDMOS) devices are shown in Fig. 4. Since snapback (triggering of the intrinsic BJT) usually causes irreversible damage to a power MOSFET or circuit malfunctions, the eSOA boundary is defined by sweeping different gate biases and connecting the I–V points right before the device snapback (indicated by the symbols of circles and triangles in Fig. 3). A higher gate bias causes a reduction in V_{DS} rating because a higher I_{DS} accelerates the electron–hole pair generation and leads to a higher I_{AV}. The eSOA differences between the two devices A and B in Fig. 4 are discussed later in this paper (Section IV-A).

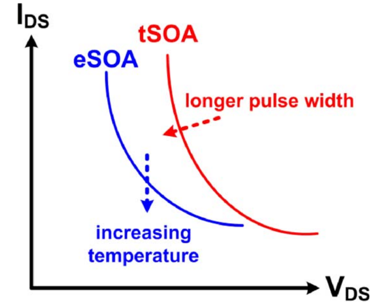

Fig. 5. Diagram showing tendencies of eSOA and tSOA with respect to temperature and pulse widths.

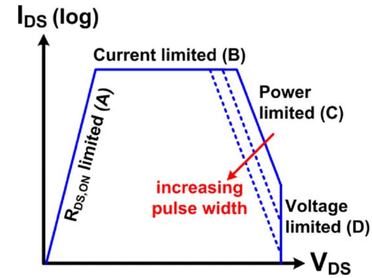

Fig. 6. Diagram showing SOA of a power MOSFET.

When a power MOSFET operates with strong device self-heating, the second term in (1), I_{TG}, can become the dominating factor. Thermal SOA (tSOA) defines the boundary of device failure initiated by thermal instability [1], [5]. Tendencies of eSOA and tSOA boundaries with respect to temperature and pulse widths are depicted in Fig. 5 [1], [6]. When temperature increases, usually the eSOA shifts downward. A longer pulse width induces a stronger device self-heating, and the tSOA shifts inward. At a certain pulse width the tSOA boundary becomes enclosed within the eSOA. The tSOA is accordingly important for a large-area power MOSFET, or when a power MOSFET is operated with a long ($\sim$ms) pulse time, solenoid drivers for example.

Though eSOA and tSOA define boundaries from different mechanisms, the two effects are usually coupled in nature as an electrothermal effect [6], [7]. R_{D}, R_{S}, and R_{B} resistors in the equivalent circuit model have positive temperature coefficients. The increases in R_{D} and R_{S} resistances under high temperature can suppress I_{AV} due to a reduced I_{DS}. The increase in R_{B} resistance, on the contrary, help forward bias the base–emitter junction and make the parasitic BJT easier to be triggered on. Avalanche multiplication factor M and the built-in potential of a bipolar base–emitter junction are also functions of temperature [1]. Techniques to decouple the electrical and thermal effects through deactivating the parasitic BJT showed appreciable electrothermal coupling to determine the SOA of power MOSFETs [8], [9]. It is therefore hard to acquire pure electrical or thermal SOA under different gate biases, and the SOA chart of a power MOSFET usually shows boundaries under different pulse widths.

Fig. 6 is an example showing different regions of SOA for a power MSOFET. There are four regions in Fig. 6; region (A) is limited by the turn-on resistance $R_{\mathrm{DS,ON}}$ of the power MOSFET. Region (B) is limited by the current carrying

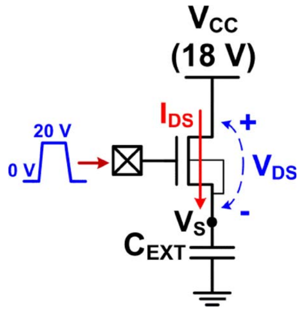

Fig. 7. Circuit diagram of an nLDMOS switching an external capacitor.

capability either from the power MOSFET or the package. Region (C) is determined by the operating current and voltage across the power MOSFET (power limited). When pulse width increases, region (C) moves downward due to the increasing device self-heating and the electrothermal coupling. Region (D) is defined by the maximum drain to source voltage rating, the BV_{DSS}. In Fig. 6, because boundaries are defined when turning the power transistor into on-state, it is referred to as the forward-biased SOA (FB-SOA).

III. Switching Reactive Loads

Power transistors are used to drive various loads in industrial and automotive applications. A switching trajectory within the SOA boundary ensures safe operation of a power transistor. Accordingly, it is equally important to understand the I–V loci when switching different loads.

A. Capacitive Load

When switching a resistive load, the I–V loci follow the Ohm's law and are relatively simple. However, when switching a reactive load, the switching loci become complicated. Voltage and current can have phase differences, resulting in high voltage and high current to occur at the same time. Test circuit of an nLDMOS to drive a large external discrete capacitor, output of a gate driver IC for example, is shown in Fig. 7. Capacitances used in the test circuits were 2.7, 4.7, and 10 nF. Device dimension (W/L) of the nLDMOS is 9600 μm/0.35 μm. When the nLDMOS is switched on, C_{EXT} is charged up through the I_{DS} current of the nLDMOS. However, due to the RC time delay from resistances of nLDMOS and metal wiring, and the capacitance of C_{EXT}, source voltage (V_{S}) of the nLDMOS is not pulled high immediately. Measured I–V waveforms in Fig. 8(a) clearly show the high I_{DS} and V_{DS} across the nLDMOS when switching a load capacitor. The I_{DS} current in Fig. 8 is acquired from a current probe; the V_{DS} voltage is calculated from $(V_{\mathrm{CC}} - V_{\mathrm{S}})$, where V_{S} is measured by using a voltage probe. When C_{EXT} is increased, a larger RC time delay causes a larger and a longer $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ stress across the nLDMOS. The I–V switching trajectories in Fig. 8(a) are redrawn in Fig. 8(b). Even though the peak I_{DS} and V_{DS} do not occur at the same time when charge/discharge a capacitor, Fig. 8 demonstrates the importance of SOA to HV transistors. Waveforms in Fig. 8(a) also suggested that when switching a capacitive load, eSOA is important due to the relatively short I–V stress time across the switching transistor [1].

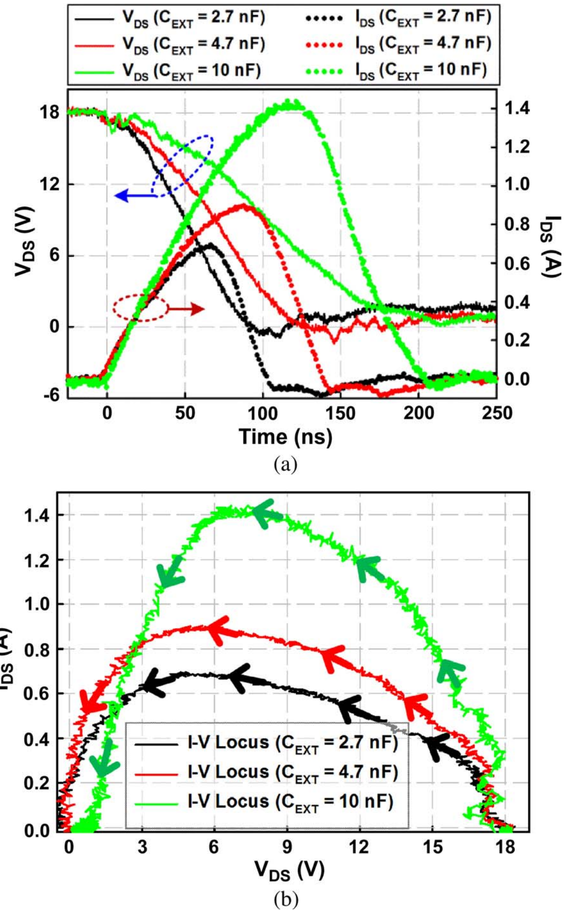

Fig. 8. Measured (a) turn-on waveforms and (b) I–V trajectories of an nLDMOS switching capacitors with different capacitance values.

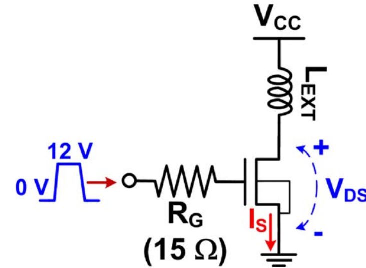

Fig. 9. Test circuit for unclamped inductive switching of an nLDMOS.

B. Inductive Load (Unclamped Inductive Switching)

Another typical example is the switching trajectory for inductive turn-off. Application example includes the solenoid driver or the relay actuator. The test circuit and some parameters used are shown in Fig. 9. Without additional clamping element, this test is usually referred to as the unclamped inductive switching (UIS) and is important for stringent operating environments such as automotive electronics [10]–[12].

When the nLDMOS is turned on, the current increasing rate follows the relationship of

$$\frac{di}{dt} \approx \frac{V_{\mathrm{CC}}}{L_{\mathrm{EXT}}} \tag{2}$$

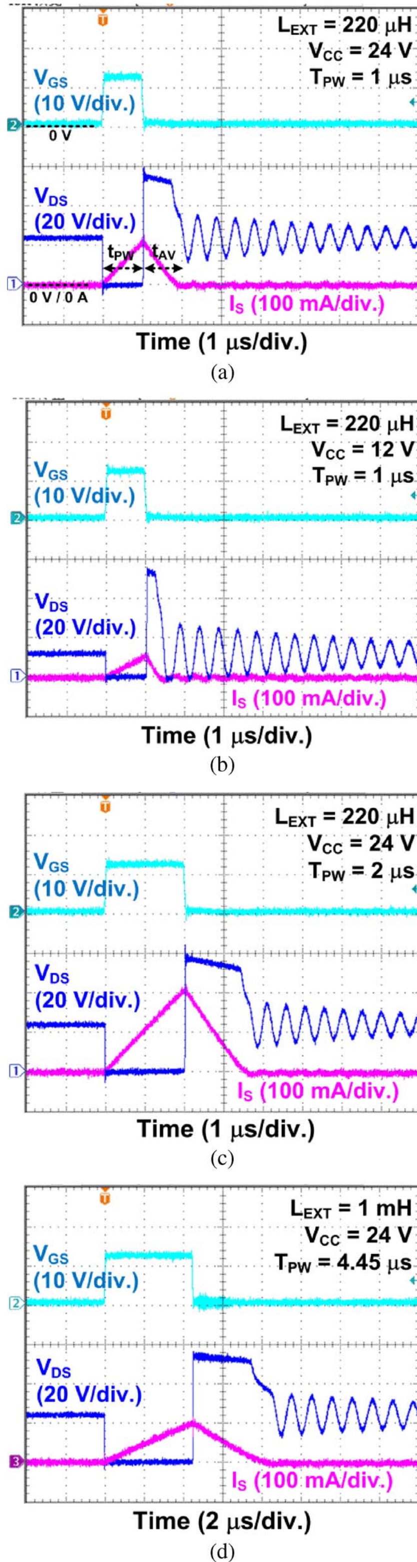

Fig. 10. Measured UIS waveforms with different L_{EXT}, V_{CC}, or T_{PW} parameters. (a) $L_{\mathrm{EXT}} = 220$ μH, $V_{\mathrm{CC}} = 24$ V, and $T_{\mathrm{PW}} = 1$ μS; (b) $L_{\mathrm{EXT}} = 220$ μH, $V_{\mathrm{CC}} = 12$ V, and $T_{\mathrm{PW}} = 1$ μS; (c) $L_{\mathrm{EXT}} = 220$ μH, $V_{\mathrm{CC}} = 24$ V, and $T_{\mathrm{PW}} = 2$ μS; and (d) $L_{\mathrm{EXT}} = 1$ mH, $V_{\mathrm{CC}} = 24$ V, and $T_{\mathrm{PW}} = 4.45$ μS.

where the total series resistance along the circuit is assumed to be small. As the measured I–V waveforms shown in Fig. 10(a), within the turn-on period T_{PW} (pulse width of the gate signal V_{GS}) the measured I_{S} current linearly increases with time and the V_{DS} has a voltage level close to the ground. During the turn-on stage, the total energy stored in the inductor is given by

$$E = \frac{1}{2} L_{\mathrm{EXT}} I_{\mathrm{AS}}^2 \tag{3}$$

where I_{AS} is the load current right before switching off the nLDMOS. I_{AS} in Fig. 10(a) is $\sim$110 mA, for example.

When the nLDMOS is switched off, the current flowing through the inductor cannot immediately drop to zero. The energy stored in the inductor drives up the V_{DS} voltage of the nLDMOS and forces the nLDMOS to discharge the load energy through avalanche breakdown [13]–[15]. The peak current I_{AS} corresponds to the avalanche current I_{AV} in (1), and the energy E_{AS} to be dissipated during inductive turn-off is

$$E_{\mathrm{AS}} = \frac{1}{2} L_{\mathrm{EXT}} I_{\mathrm{AS}}^2 \frac{BV}{BV - V_{\mathrm{CC}}}. \tag{4}$$

As the measured waveforms shown in Fig. 10(a), when the V_{GS} is turned off, the V_{DS} voltage shoots up to the breakdown voltage (BV) of the nLDMOS ($\sim$58 V); current begins to decrease linearly and the V_{DS} voltage is kept high until I_{S} drops to zero. The current decreasing rate during inductive turn-off follows:

$$\frac{di}{dt} = \frac{BV - V_{\mathrm{CC}}}{L_{\mathrm{EXT}}}. \tag{5}$$

Since the switching transistor is operated under avalanche breakdown, the time to discharge the energy stored in the inductor is usually referred to as t_{AV}. From (5), t_{AV} can be derived as [15]

$$t_{\mathrm{AV}} = \frac{L_{\mathrm{EXT}} \times I_{\mathrm{AS}}}{BV - V_{\mathrm{CC}}}. \tag{6}$$

With the above equations, several parameters affecting the UIS waveforms can be observed from Fig. 10. When V_{CC} voltage is reduced from 24 to 12 V, (2) and (6) suggest that I_{AS} should be reduced to a half and t_{AV} is shortened as well [see Fig. 10(a) and (b)]. Increasing the T_{PW} width from 1 to 2 μs doubles I_{AV}; t_{AV} increases as well [see Fig. 10(a) and (c)]. When the inductance is increased from 220 μH to 1 mH, T_{PW} to reach the same I_{AV} current magnitude is increased from 1 to 4.45 μs [see Fig. 10(a) and (d)]. From (4) and (6), at the same I_{AV} the larger inductance results in a longer t_{AV} and a larger energy to be dissipated, i.e., the transistor is stressed more severely.

From Fig. 10(a) and (c), dependence between the peak V_{DS} voltage and the I_{AV} magnitude during inductive turn-off, though weak, is also observed. For a gate-grounded nLDMOS entering avalanche breakdown, the I–V characteristic is illustrated as Fig. 11. When the V_{DS} voltage across an nLDMOS is higher than its BV_{DSS}, avalanche current I_{AV} starts to flow; snapback does not happen immediately until the current magnitude reaches I_{t1}, at which the BJT base–emitter junction is forward biased through R_{B} (see Fig. 2). The I_{AS} current level during UIS test cannot exceed I_{t1}, otherwise the nLDMOS snaps back and a latchup-like electrical overstress

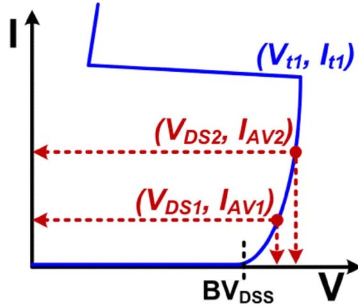

Fig. 11. Diagram depicting the I–V characteristic of a gate-grounded nLDMOS.

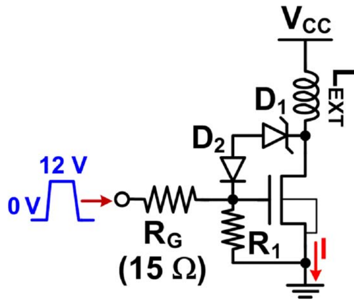

Fig. 12. CIS test circuit using a Zener diode to clamp the nLDMOS drain voltage during inductive turn-off.

will permanently damage the nLDMOS. For an UIS test with a peak inductor current $I_{\rm AS1}$, the energy stored in the inductor will correspondingly charge up the drain voltage to $V_{\rm DS1}$ during inductive turn-off so as to keep current continuity. From Fig. 11, it is known that a higher peak inductor current $I_{\rm AV2}$ causes a higher voltage $V_{\rm DS2}$ during inductive turn-off. Note that $I_{\rm TG}$ in (1) can contribute greatly to the device snapback in UIS because of the high power during avalanche breakdown and the long $t_{\rm AV}$ during inductive turn-off (from several μs up to several tens of ms) [16].

Because the stress across the transistor in an UIS test happens when turning off the transistor, it is classified as the reverse-biased SOA (RB-SOA) and usually uses different rating methods than the FB-SOA [17]. The term RB-SOA is often reserved for BJTs switching unclamped inductive load, and for MOSFETs UIS is used more often. To evaluate the transistor ruggedness against UIS, two parameters are usually adopted as the benchmark. The first parameter is the maximum allowable switching current $(I_{\rm AS,Max})$ without inducing transistor failure [10], [18]. The other rating method uses (4), the maximum energy $E_{\rm AS,Max}$ dissipated in the switching transistor without inducing failure, as the benchmark. The second method is also known as the energy capability of a power MOSFET [11].

C. Inductive Load (Clamped Inductive Switching)

Due to the high junction temperature over a MOSFET during avalanche breakdown, UIS is a harsh test for power MOSFETs. In practical designs, the clamped inductive switching (CIS) is usually used to bypass the energy during inductive turn-off without avalanching the switching transistor.

An example of the CIS circuit is shown in Fig. 12 [8], [19]. When switching off the inductive load, the Zener diode D_1

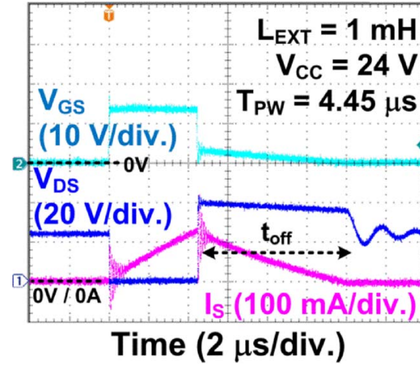

Fig. 13. Measured I–V waveforms of the CIS test circuit. The breakdown voltage of the Zener diode is 37 V.

breaks down and a current $I_{\rm Z}$ pulls high the gate potential of the nLDMOS through the diode D_2 and the R_1 resistor. The D_1 diode is chosen to have a breakdown voltage $BV_{\rm Z}$ smaller than the $BV_{\rm Dss}$ of the nLDMOS so as to prevent nLDMOS from avalanche breakdown. The drain voltage of the nLDMOS during inductive turn-off is therefore limited at $V_{\rm clamp} = BV_z + V_{\rm diode} + (R_1 \times I_z)$. With the gate potential pulled high, the energy stored in the inductor is mainly discharged through the channel current of the nLDMOS. Measured I–V waveforms of the CIS test circuit are shown in Fig. 13; $BV_{\rm Z}$ of the Zener diode D_1 in Fig. 13 is 37 V, and the nLDMOS is the same transistor used to measure Fig. 10. When switching off the inductor, the measured $V_{\rm DS}$ voltage is clearly limited at a lower voltage level around the $BV_{\rm Z}$ of D_1. Note that in a CIS circuit, FB-SOA of the switching transistor is important as well because the transistor has to sustain $V_{\rm clamp}$ and the inductive turn-off current at the same time.

In the CIS circuit, because the drain voltage of the nLDMOS is limited at $V_{\rm clamp}$, the time $t_{\rm off}$ to dissipate the energy stored in the inductor becomes

$$t_{\rm off} = \frac{L_{\rm EXT} \times I_{\rm MAX}}{V_{\rm clamp} - V_{\rm CC}} \tag{7}$$

where $I_{\rm MAX}$ is the current right before switching off the nLDMOS. Comparing (6) and (7), with the $V_{\rm clamp}$ smaller than the breakdown voltage of the nLDMOS, the CIS circuit results in a longer inductive turn-off time as shown in Fig. 13. The energy dissipated in the nLDMOS during inductive turn-off becomes

$$E_{\rm AS} = \frac{1}{2} L_{\rm EXT} I_{\rm MAX}^2 \frac{V_{\rm clamp}}{V_{\rm clamp} - V_{\rm CC}}. \tag{8}$$

When measuring energy capabilities, (4) and (8) show that different inductances, current magnitudes, Zener diodes . . . etc. have to be changed during tests to figure out the $E_{\rm AS,MAX}$ of a DUT. The test procedures are inconvenient and difficult to control. To facilitate the measurement, alternative rectangular power pulsing (RPP) test methods which use rectangular voltage or current pulses with different pulse widths have been proposed [19]. Voltage and current RPP testing circuits are shown in Fig. 14(a) and (b), respectively. The RPP tests save the usage of external inductors. Energy capabilities of DUTs can be easily figured out simply by varying pulse widths or magnitudes of delivered voltage/current pulses. Though in a

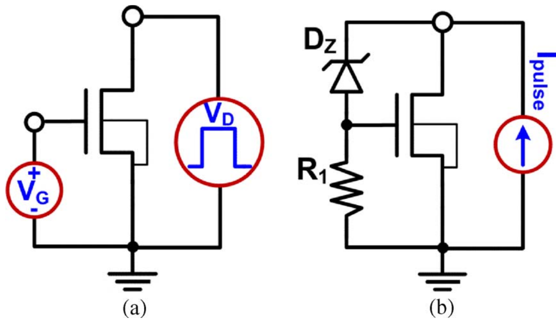

Fig. 14. Measurement setups for (a) voltage and (b) current rectangular power pulsing test circuits (redrawn after [19]).

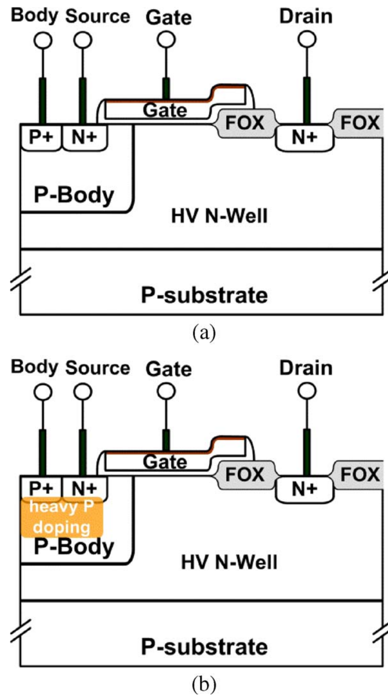

Fig. 15. Device cross-sections of (a) a regular nLDMOS and (b) an nLDMOS with additional P-type implantation at body to improve SOA.

real inductive switching condition the current waveform is in a triangular shape, RPP tests have been verified to deliver reasonably accurate results [19].

IV. Techniques to SOA Improvement in High-Voltage Integrated Circuits

A power MOSFET with wide intrinsic SOA can enhance device reliability under different load conditions. As a result, aside from the CIS method to assist transistors, various techniques to improve the intrinsic SOA of power MOSFETs have been proposed.

A. Additional Body Implantation

Since the criterion for a BJT to be triggered on is the forward conduction of its base–emitter junction, reducing the resistance of R_B in Fig. 2 is effective in widening the MOSFET SOA [20]–[23]. The process integration method in reducing the R_B resistor is illustrated in Fig. 15. Comparing to the regular nLDMOS structure shown in Fig. 15(a), an additional

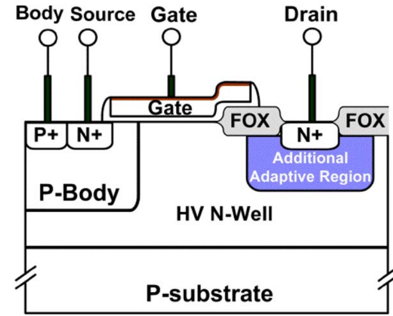

Fig. 16. Device cross-sectional view of an nLDMOS with the additional drain adaptive region to improve SOA.

P-type body implantation (PBI) is added to elevate the doping concentration of P-body [see Fig. 15(b)]. An nLDMOS which does not have the PBI layer showed the measured eSOA boundary (A) in Fig. 4; another nLDMOS with the additional PBI layer has the eSOA boundary (B) in Fig. 4. Except for the additional body implantation, both devices have the same layout and device dimension, 4800 μm/0.35 μm. It is clear from Fig. 4 that the additional P-type body implantation substantially improves the FB-SOA of power MOSFETs. With the reduced R_B, $I_\mathrm{AS,MAX}$ in an UIS test for the 4800-μm nLDMOS improves from 100 to 350 mA as well, a result consistent to previous publications [20], [21].

B. Drift Configuration

It is well known that for a power MOSFET under high current conduction, the kirk effect shifts the high electric field region toward the transistor drain contacts [24]. Since the avalanche current that induces both the triggering of parasitic BJTs and the electrothermal coupling is a result of the high electric field, engineering the drift region of a power MOSFET is another approach to the SOA adjustment. A higher doping concentration in the drift region of an nLDMOS can compensate the negative electron charges during transistor on-state and hence push the onset of kirk effect to a higher current level [25]. However, increasing the doping concentration in the drift region reduces the device BV_DSS as well [26]. Lengthening the drift region is another method to adjust the device SOA because the higher series resistance from the drift region limits the transistor saturation current. This, however, results in a higher transistor R_SP. Accordingly, an adaptive method that introduces an additional n-type adaptive doping region was proposed to counteract the drawbacks and to improve the transistor SOA [23], [26]–[28]. The device cross-sectional view of an nLDMOS with the adaptive doping region is shown in Fig. 16; the adaptive region has a doping concentration higher than that of the HV N-Well. Besides the benefit on the SOA, the drain profile has also been reported as a key device parameter for implementing power MOSFETs with high electrostatic discharge (ESD) protection levels [23], [29]–[33].

C. Dotted-Channel LDMOS

Using additional body implantation to reduce the R_B resistance and to suppress the BJT action is useful, but often inaccessible to fabless IC design companies. A dotted-channel layout

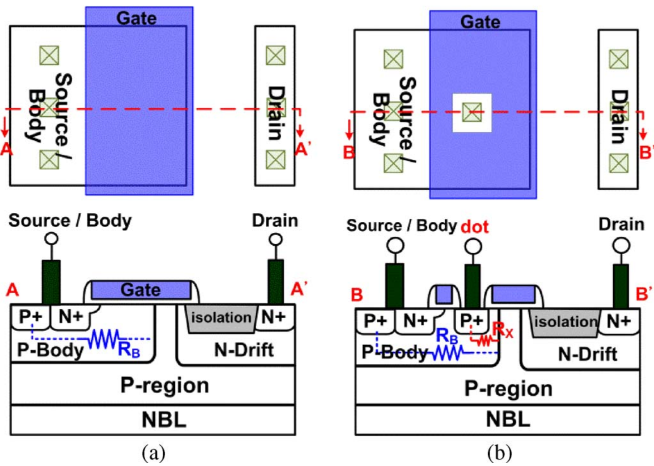

Fig. 17. Layout and device cross-sectional views of (a) a regular LDMOS and (b) a dotted-channel LDMOS (redrawn after [34]).

technique for the SOA improvement without modifying process steps or mask layers is reported in [34]. As illustrated in Fig. 17, poly gate in a dotted-channel LDMOS is intentionally opened with squares to insert P+ diffusion regions and metal contacts (dots). When these dots are grounded through metallurgical connection, an additional parasitic resistor R_{X} is formed [see Fig. 17(b)]; R_{X} is in parallel with the body resistor R_{B} of a regular LDMOS and hence, the effective body resistance R_{B}' in a dotted-channel LDMOS becomes $(R_{\mathrm{B}}//R_{\mathrm{X}})$, and the parasitic BJT is suppressed.

In the dotted-channel layout, in order to open dots in transistor poly gate the gate length may need to be extended, depending on the technology node being used. Moreover, to prevent transistor breakdown voltage from being affected by the dots, the distance between the dotted contact and the drift region has to be larger than the minimum allowable channel length [34]. These restrictions result in a negative impact to transistor R_{SP}, and the quantity of impact is highly process-dependent. Recently, a poly-bending layout structure that bends the poly gate in 45° was proposed. The poly-bending layout has ground dots as well to improve the degraded SOA of an nLDMOS due to the insertion of a silicon controlled rectifier [35]. This poly-bending layout can also be implemented on an nLDMOS. Layout top view of an nLDMOS utilizing the poly-bending layout is illustrated in Fig. 18(a), and the device cross-sectional view along the $C-C'$ line is shown in Fig. 18(b). The ground dots in the poly-bending nLDMOS create an additional R_{X} similar to the dotted-channel LDMOS, thus making the poly-bending layout promising for the SOA improvement of nLDMOS transistors.

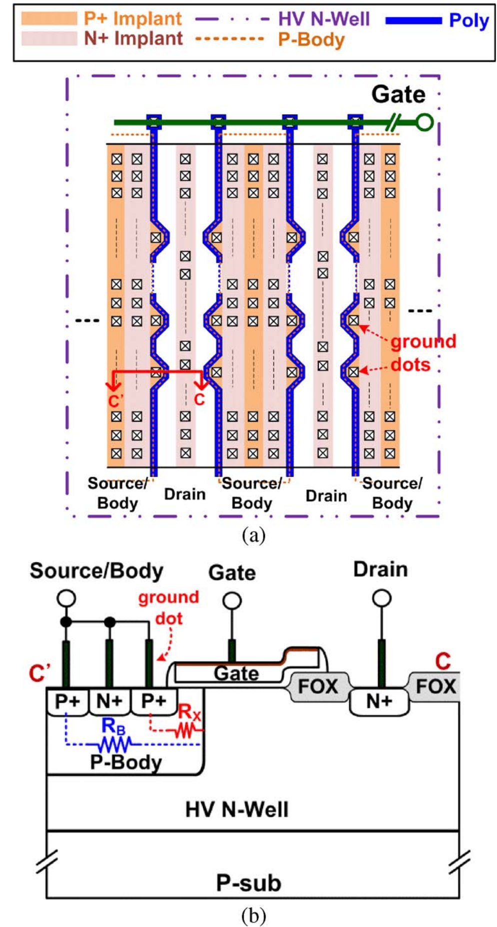

Fig. 18. (a) Layout top view and (b) device cross-sectional view along $C-C'$ line of a poly-bending nLDMOS.

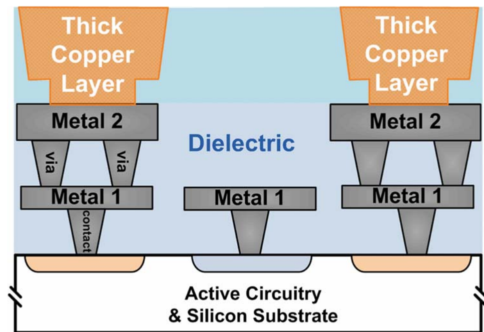

Fig. 19. Illustration of the thick copper metallization in power ICs for the improvement of transistor SOA.

D. Thick Copper Metallization

For a power transistor that operates with a long on-state period or has a large device area ($\sim$mm^2), thermal effect is prominent and the transistor junction temperature can become high enough to initiate thermal runaway [36], [37]. The removal of the temperature rise within the active transistor in response to the dissipated energy accordingly helps improve the device stability. In power technologies, this can be accomplished by using a heat sink over the power transistor. Due to the good thermal properties and mature process integration techniques to handle with, copper is chosen over other metal materials. As illustrated in Fig. 19, thick copper metal layers are plated over active circuitry to serve as a waver-level heat sink [38]–[40]. This on-chip technique is equally important for sub-millisecond operations where the time is not enough for the IC packaging to give an effect to the device temperature [41], [42]. The copper metallization has been demonstrated to substantially improve the transistor energy capability, and a thicker copper metallization further enhances the improvement [38]–[42]. Moreover, it

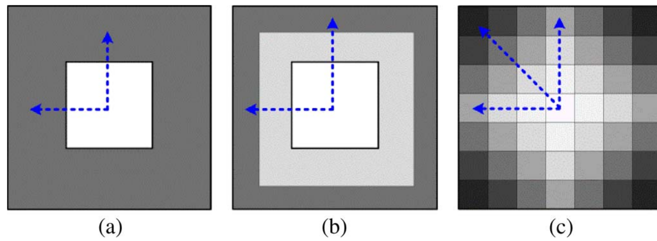

Fig. 20. Illustration of power MOSFET arrays with (a) single-step, (b) dual step, and (c) checkerboard layout design for improving the uniformity of power distribution (redrawn after [44]).

is also used as a surface layer of metal wiring to solve the voltage de-biasing effect [43] in large power MOSFETs and to save power consumption through the reduced overall R_{ON}[38], [40].

E. Power Distribution

With the strong device self-heating involved in switching a large power MOSFET, the temperature spread across the transistor array is found to be inhomogeneous. Device edges benefit from a better thermal removal through surrounding silicon and the weak spot (highest temperature) hence locates at the center of the array [37], [44]. A uniform temperature distribution across the power transistor array eliminates the weak spot and improves the transistor energy capability.

From the 1-dimensional heat flow theory, a simple relationship between power dissipation P, temperature increase ΔT and time t is

$$\Delta T = \frac{2P}{\sqrt{\pi k \rho c_p} A_E}\sqrt{t} \tag{9}$$

where k is thermal conductivity, ρ is density, c_p is specific heat capacity, and A_E is active area. From (9), the temperature increase is proportional to the power dissipation and the square root of time. Having different operating time among an array is less practical; uniform power distribution across a power MOSFET array is more feasible. With the MOSFET saturation current being

$$I_{D,\mathrm{sat}} = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L}(V_{\mathrm{GS}} - V_t)^2 \tag{10}$$

a multi-step layout design utilizing different current carrying capabilities is proposed to engineer the power distribution (see Fig. 20) [44]. Power MOSFET arrays are divided into regions of different channel lengths (L) or oxide thickness. Arrows in Fig. 20 indicate the direction of increasing current carrying capability (shorter channel length for example). Experimental results in [44] showed a more than 20% improvement on the energy capability and less than 10% increase on transistor turn-on resistance. Moreover, with a proper design, the simple single-step layout shown in Fig. 20(a) was able to optimize the power distribution to its fullest already [44].

V. Conclusion

A wide SOA is required to sustain the high voltage and high current at the same time that happens across a power MOSFET during the circuit operations with the switching of reactive loads. Through the circuit design technique, clamped inductive switching can help improve SOA when driving an inductive load. Process integration approaches such as a heavily doped body region, an adaptive drift implantation, or a thick plated copper layer can improve intrinsic SOA of power MOSFETs. Besides the circuit and the process integration methods, layout modifications can also enhance SOA of power MOSFETs. In summary, safe operating area is one of the most important indicators for the reliability of power MOSFETs. Improvement techniques on the SOA will keep continuing as an essential and critical factor in the development of power MOSFETs for using in high-voltage integrated circuits.

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