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Effect of Gate Length on Device Performances of AlSb/InAs High Electron Mobility Transistors Fabricated Using BCl_3 Dry Etching

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In this paper, we present the development of a mesa isolation process for AlSb/InAs high electron mobility transistors (HEMTs) using inductively coupled plasma (ICP) etching with BCl_3 gas. Devices with different gate lengths (L_g: 60, 100, and 200 nm) fabricated by this dry etching technique show good DC and RF performances. With an appropriate L_g/gate-channel distance ratio, the 200-nm-gate has very high peak transconductances of 781 mS/mm at $V_{DS} = 0.1$ V and 2000 mS/mm at $V_{DS} = 0.5$ V. Moreover, an extrinsic current gain cutoff frequency of 137 GHz and maximum oscillation frequency of 97 GHz were achieved at a drain bias voltage $V_{DS} = 0.3$ V, indicating the great potential for such a device operating at high frequency with extremely low DC power consumption. © 2012 The Japan Society of Applied Physics

Electronic and optical devices based on binary alloys of the 6.1 Å family including InAs (6.058 Å), GaSb (6.096 Å), and AlSb (6.136 Å) have attracted much attention recently. Antimonide-based compound semiconductor AlSb/InAs high electron mobility transistors (Sb HEMTs) have been demonstrated for extremely low voltage operations due to the combination of high peak electron velocity ($\sim 4 \times 10^7$ cm/s) at a low electric field and high channel conductivity with the high electron confinement barrier (1.35 eV) of the InAs/AlSb interface.[1,2] In fact, these values for Sb HEMTs are nearly two times higher than those of In-rich $In_xGa_{1-x}As$/InP HEMTs, demonstrating their great potential for phased-array and satellite systems, which require ultralow-power consumption.[3–5]

The $Al_xGa_{1-x}Sb_yAs_{1-y}$/InAs material system has proven to be a viable choice for advanced AlSb/InAs HEMTs with metamorphic growth on a GaAs substrate and an AlSb/AlGaSb buffer layer can eliminate the dislocations effectively.[6] Unfortunately, AlSb is extremely liable to be oxidized in air. Additionally, wet etching of the AlSb and InAlAs stacked layers is hard to control to achieve the required depth and is not repeatable in mesa isolation steps. As a result, it is essential to develop a dry etching technique for a more controlled and less labor-intensive fabrication process.

Gate length scaling is a well-known technique to boost the operating frequency of devices. However, in some cases, scaling the gate length (L_g) alone may not be as effective as expected. It is thus our motivation to investigate the effect of gate length scaling on the device performance of Sb HEMTs.

In this study, we fabricate AlSb/InAs HEMTs with L_g of 60, 100, and 200 nm using an ICP etcher with BCl_3 gas. The effect of L_g on AlSb/InAs HEMTs performances has also been investigated. The fabricated devices demonstrate excellent DC and RF performances after dry etching, indicating the successful fabrication of AlSb/InAs HEMTs using this BCl_3 dry etching process for mesa etching.

Figure 1 shows the epitaxial structure of the Sb HEMTs. The AlSb/InAs heterostructure was grown on a 3-in. GaAs substrate by solid-source molecular beam epitaxy (MBE). The composite AlSb/$Al_{0.7}Ga_{0.3}Sb$ metamorphic buffer layer was utilized to accommodate the lattice mismatch between the GaAs substrate and device layer. Te planar doping was

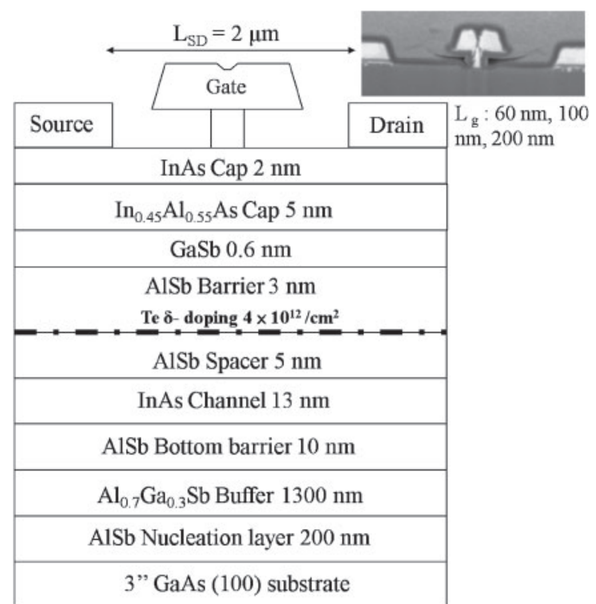

Fig. 1. Epitaxial structure of the AlSb/InAs HEMT device. The inserted SEM image is the T-shaped gate after silicon nitride passivation. Devices with L_g between 60 and 200 nm were fabricated.

employed in the AlSb barrier layer to attain high electron transfer efficiency and reduce the gate-to-channel distance.[7] A 5-nm-thick $In_{0.45}Al_{0.55}As$ layer was capped on the GaSb and AlSb layers to prevent air exposure and provide a chemically stable surface layer. The electron sheet carrier density and mobility at room temperature were measured to be 1.7×10^{12} cm^{-2} and 22,400 cm^2 V^{-1} s^{-1}, respectively.

The fabrication process started with mesa isolation through a novel inductively coupled plasma (ICP) process using BCl_3 gas (ULVAC NE-950EX etcher) and the dry etching was stopped at the $Al_{0.7}Ga_{0.3}Sb$ buffer layer. BCl_3 gas has been found to be more effective for etching AlGaSb than Cl_2-based gases.[8] The critical step in guaranteeing the performance of the fabricated Sb HEMTs is mesa formation by dry etching, which must be well controlled so that it stops at the $Al_{0.7}Ga_{0.3}Sb$ buffer, where 30% Ga is added to avoid the oxidation of AlSb.[9] Figure 2(a) shows the etching depth as a function of etching time for the device etched with BCl_3

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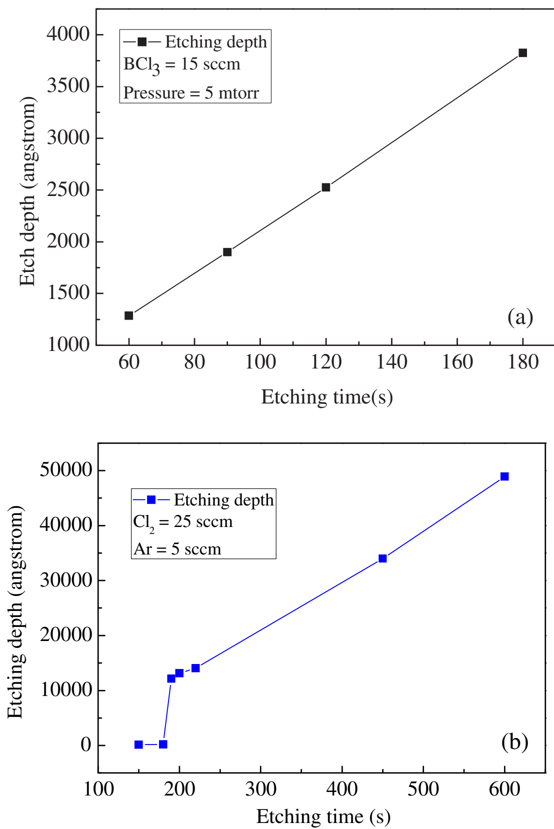

Fig. 2. (Color online) (a) Etch depth as a function of the etching time for the Sb HEMT using BCl_3 and (b) etch depth as a function of the etching time for the Sb HEMT using Cl_2/Ar.

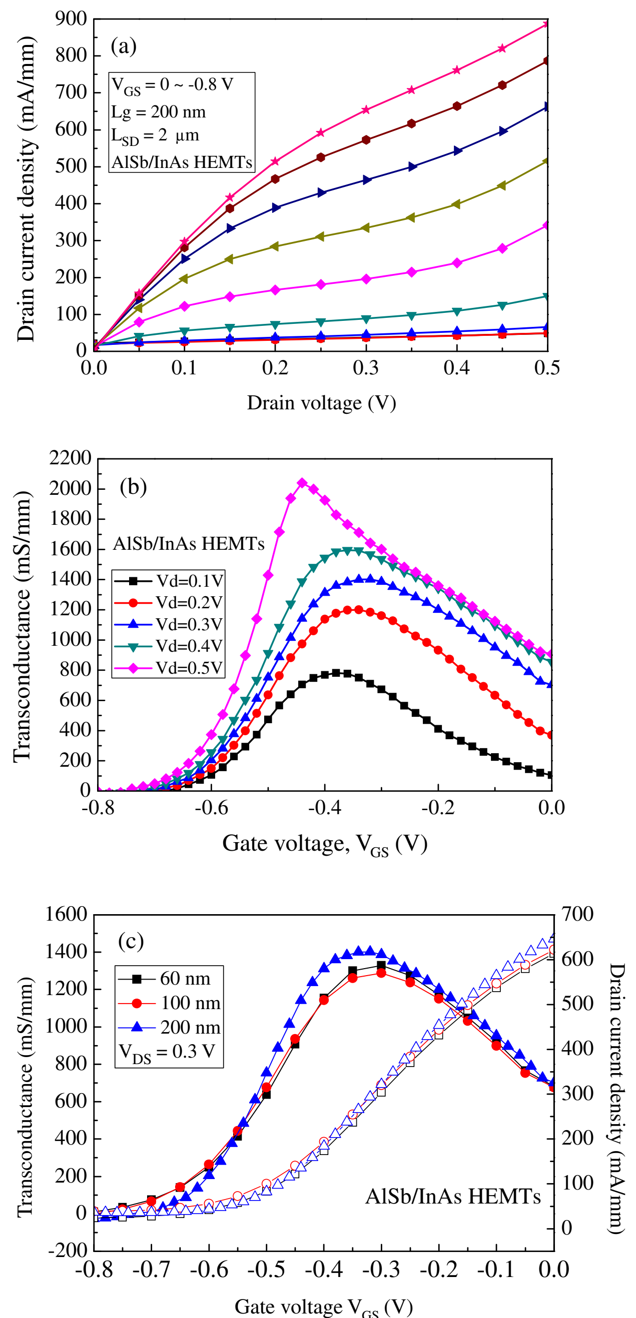

Fig. 3. (Color online) (a) Drain and (b) transfer characteristics of the 200 nm AlSb/InAs HEMT. The gate width is 20 × 2 µm and the source–drain spacing is 2 µm. (c) g_m versus V_{GS} with different gate lengths at V_{DS} = 0.3 V.

gas. The etching rate is well controlled to obtain shallow mesa isolation. The measured etch depth as a function of the etching time with Cl_2/Ar mixed gas is depicted in Fig. 2(b). As observed from the figure, it is hard to control the etching depth using Cl_2/Ar due to the drastic increase in depth when the etching time is approximately 200 s. The depth of the device mesa was measured to be approximately 1500 Å by KLA-Tencor P-10 surface profiler. Pd/Pt/Au ohmic contacts were evaporated and subsequently annealed at 300 °C for 30 s in N_2 ambient, resulting in a low contact resistance of 0.027 Ω mm and a sheet resistance of 157 Ω/sq. Non-recessed Pt/Ti/Pt/Au T-shaped gates were defined on the InAs cap layer using trilayer resist and electron beam lithography. The inserted scanning electron microscopy (SEM) image in Fig. 1 is the 60 nm T-shaped gate after silicon nitride passivation. Finally, a 100-nm-thick SiN passivation layer was deposited by low-temperature plasma-enhanced chemical vapor deposition (PECVD) to protect the devices.

Figure 3(a) shows the drain–source current (I_{DS}) as a function of drain–source voltage (V_{DS}) with the gate–source voltage (V_{GS}) varied from 0 to −0.8 V for the 200-nm-gate and 2 × 20-µm^2-width device. The device exhibits a maximum drain current density of 900 mA/mm at a gate bias of 0 V and a drain bias of 500 mV. Figure 3(b) shows the DC transconductance (g_m) as a function of gate voltage at different V_{DS} for the same device. A maximum DC g_m of 2000 mS/mm is achieved at the same bias. At room temperature, the measured on-resistance R_{ON} was 0.33 Ω mm.

The IV characteristics in Fig. 3 illustrate the advantages of the Sb HEMT with low-voltage operation, low R_{ON}, and high g_m, which are necessary for ultralow-power and high-frequency applications. Such a high current density and g_m value result from the high peak electron velocity at a low electric field and the high channel conductivity, which enable the operation of AlSb/InAs HEMTs at very low drain bias voltages. As observed from Fig. 3(b), the drastic increase in the g_m peak value for V_{DS} greater than 0.4 V is due to the impact ionization in the channel resulting from the staggered band lineup at InAs/AlSb heterojunctions. Since the staggered band alignment at such heterojunctions does

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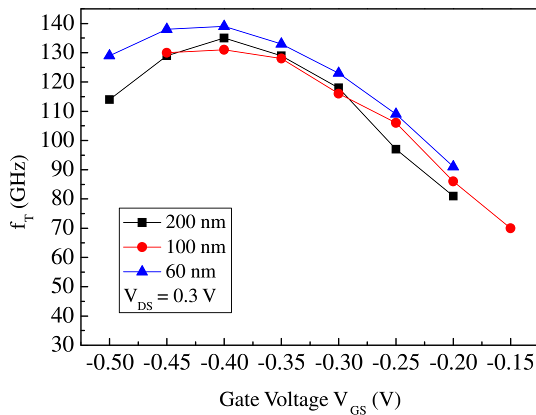

Fig. 4. (Color online) f_T as a function of gate voltage for different gate lengths.

not confine holes, electron flows into the channel, increasing the channel current and g_m.[10]

The transconductance and drain–source current plotted as a function of gate voltage for devices with different gate lengths at $V_{DS} = 0.3$ V is shown in Fig. 3(c). The peak g_m of the 200 nm device (1401 mS/mm) is slightly higher than those of the 100 nm (1288 mS/mm) and 60 nm (1329 mS/mm) devices.

The *S*-parameter of the devices was measured from 2 to 110 GHz using an on-wafer probe system with an HP8510XF network analyzer. The extrinsic cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were extracted from extrapolation of the measured current gain (H_{21}) and Mason's unilateral gain (U) using a -20 dB/decade slope. The 200 nm device exhibited f_T and f_{max} of 137 and 97 GHz at $V_{DS} = 0.3$ V, respectively. These results also demonstrate the feasibility of BCl_3 dry etching for shallow mesa formation in Sb HEMTs fabrication.

f_T as a function of gate voltage for different gate lengths is shown in Fig. 4. As shown, high f_T and f_{max} were achieved at low bias levels for all devices due to the good transport properties in the InAs channel. Interestingly, it is observed that the 60 nm device does not significantly outperform the others as expected. The extracted intrinsic RF g_m was 1250 mS/mm for the 60 nm device, 1175 mS/mm for the 100 nm device, and 1225 mS/mm for 200 nm device, which showed a similar trend to that depicted in Fig. 4. Apparently, merely scaling the gate length is not enough to boost the f_T if the gate-channel distance is not optimized with the L_g aspect ratio, which agrees with the results of Guerra *et al.*[11] Another reason for this phenomenon is the occurrence of the ballistic effect in the electron transport under the gate electrode for the 60 and 100 nm devices.[12]

In summary, an ICP dry etching process using BCl_3 gas has been developed to precisely control the etching depth for shallow mesa isolation in the fabrication of AlSb/InAs HEMTs. Effect of the gate lengths on device performances was also investigated. Good DC and RF performances, with an extrinsic f_T/f_{max} of 137/97 GHz, were achieved at $V_{DS} = 0.3$ V for $2 \times 20\,\mu$m HEMTs with a 200 nm gate length. These results demonstrate the potential of Sb HEMTs for low-voltage operation at high frequencies.

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