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Characteristics of n-Type Asymmetric Schottky-Barrier Transistors with Silicided Schottky-Barrier Source and Heavily n-Type Doped Channel and Drain

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In this study, we explore the operation of operation a novel asymmetric Schottky-barrier transistor (ASSBT) through using technology computer aided design (TCAD). The new ASSBT features a silicided Schottky-barrier (SB) source, with the channel and drain made of heavily n-doped silicon. By eliminating the SB drain junction contained in conventional symmetrical-type SB metal–oxide–semiconductor field-effect transistors (MOSFETs), a larger on-state current is achievable. Moreover, combined with the adoption of fully depleted thin-film channel, the off-state leakage current can be efficiently suppressed as well. In addition, we also comprehensively analyze the transport mechanisms dominating in different operational regions of this new ASSBT. A pseudo-subthreshold region that shows worse subthreshold swing (SS) than the subthreshold region is identified. A decrease in channel and/or gate oxide thicknesses can contribute to the improvement of the SS of this region. A modified form of scaling length (λ) is also introduced to describe the impacts of structural parameters and gate configurations on the SS characteristics of this new ASSBT.

1. Introduction

The Schottky-barrier (SB) metal–oxide–semiconductor (MOS) transistor with the source and drain (S/D) made of metallic silicides has been proposed as one of the promising candidates for replacing conventional doped S/D metal–oxide–semiconductor field-effect transistors (MOSFETs), since silicided S/D can provide shallow and abrupt junctions with a low serious resistance.[1–5] Device operation mechanisms of conventional inversion-mode SB transistor with symmetrical[6] or asymmetrical S/D[7] have been reported in the literature. Usually, a symmetric SB transistor (SSBT) that has silicided SB S/D suffers from a large leakage current due to the inherent ambipolar characteristics.[1–5] Such an issue could be addressed with an asymmetric SB transistor (ASSBT) proposed by Uchida *et al.*[7] In a previous work, devices with a silicided source and a heavily doped drain (i.e., with a conventional p–n junction) were built on a bulk substrate. The use of the doped drain junction in lieu of the silicided one greatly suppresses the leakage in the off-state.

On the other hand, for conventional MOSFETs, the provision of abrupt and uniform S/D junctions becomes increasingly difficult as the devices are continuously scaling down. To address this issue, junctionless transistors that have a heavily doped channel with doping concentrations higher than $10^{19}\,\mathrm{cm}^{-3}$ and of the same type as that of the S/D have been proposed for nano scale complementary MOS (CMOS).[8–10] In addition, junctionless transistors have also been proposed for applications in three-dimensional (3D) stacked NAND flash memories.[11] The combination of the heavily doped channel and SB S/D is a very intriguing research topic. In this work, by using technology computer aided design (TACD),[12] we propose and explore a new ASSBT that features SB only on the source side, while the channel and drain are both n^+-doped. That is the drain is "junctionless-like". Our simulation results show that excellent on/off device characteristics are achieved with such a scheme. Dominant conduction mechanisms in different operation regions and the effects of channel thickness and gate oxide thickness are also studied.

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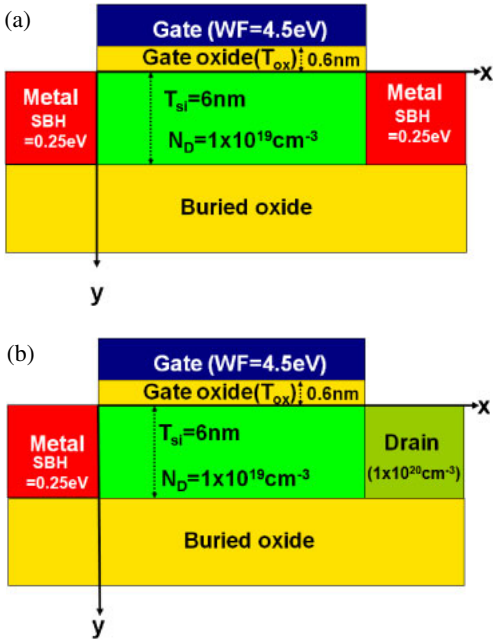


Fig. 1. (Color online) Schematic diagrams of the (a) SSBT with silicided SB S/D and (b) ASSBT with silicided SB only on the source side investigated in this work. $T_{si} = 6\,\mathrm{nm}$, $T_{ox} = 0.6\,\mathrm{nm}$, WF = 0.5 eV, and SBH = 0.25 eV. Channel doping $N_D = 1 \times 10^{19}\,\mathrm{cm}^{-3}$.

2. Subthreshold Characteristics of ASSBT

Figures 1(a) and 1(b) show the simulated device structures of single-gated (SG) SSBT and the proposed ASSBT, respectively, both with a heavily n^+-doped channel. The former is with the symmetrical silicided SB source/drain while the latter has silicided SB formed only on the source side. In Fig. 1(b), the proposed new structure eliminates the need for the p–n drain junction in previously reported ASSBTs.[7] Such a junctionless-like feature of the new ASSBT requires an ultra thin channel in order to effectively switch off the current conduction of the device. It should be noted that, although the channel doping of the proposed structure is of the same type as that of the drain, which is akin to that of conventional accumulation-mode (AM) device, the high channel doping ($10^{19}\,\mathrm{cm}^{-3}$) of the present

Table I. Major parameters of SSBT and ASSBT used in simulation.

Gate work function, WF (eV)	4.5
Gate oxide thickness, T_{ox} (nm)	0.6
Silicon thin film thickness, T_{si} (nm)	6
Doping concentration in drain (cm^{-3})	1×10^{20}
Doping concentration in channel (cm^{-3})	1×10^{19}
Schottky-barrier height, SBH (eV)	0.25

structure makes its operation quite different. While conventional AM devices adopt a channel doping concentrations typically ranging from 4×10^{16} and 5×10^{17},[13–15] which are much lower than those of the drain. When an AM device is turned on, an accumulation layer (carrier concentration typically $\geqq 10^{19}\,cm^{-3} \gg$ channel doping) is formed and current conduction take place near the oxide/channel interface. In contrast, current conduction in the present scheme in the on-state is mainly through the whole channel rather than close to the oxide interface (see later in the analysis part). Therefore, the operation characteristics are different from those of the AM devices.

Detailed parameters used for the simulation of the devices are listed in Table I. The directions of x and y shown in Figs. 1(a) and 1(b) are parallel and perpendicular to the source-to-drain direction, respectively. A two-dimensional (2D) TCAD tool "DESSIS"[12] is employed in this work for the simulation analysis. The tunneling current conducting through the SB is examined using a non local tunneling model with with effective masses of 0.26 and $0.36\,m_0$ for electrons and holes, respectively. Figures 2(a) and 2(b) show comparisons of the calculated drain current–gate voltage (I_D–V_G) characteristics of SSBT and the new ASSBT with gate length (L_G) values of 100 and 22 nm, respectively. Similar to the conventional inversion-mode SB-MOSFETs, the SSBTs with a heavily n^+-doped channel show ambipolar behavior, i.e., a large gate-induced drain leakage (GIDL)-like current is conducting in the off-state,[2] resulting in low on/off current ratios. In contrast, the ASSBT shows unipolar transfer characteristics with a significantly reduced off-state current, owing to the suppression of hole current injection from the drain side as gate voltage is sufficiently negative. Moreover, the on-state current of the ASSBT is also slightly improved, owing to the reduction of the drain resistance component. Although the I_D–V_G characteristics of heavily n^+-doped channel SB transistors appear similar to the conventional inversion-mode SB transistors,[2] their operational physical mechanisms are quite different. The most striking feature associated with the operation of the present devices is that they must be turned off by depleting the heavily doped channel.[16] The dominant transport mechanism depends on the operation condition. To help understand the situations, a typical I_D–V_G curve of an ASSBT with an n^+-doped channel is shown in Fig. 3, which is divided into three regions corresponding to different transport mechanisms. To elaborate on the mechanisms, electron density and electric potentials in the silicon channel along the y-direction near the source at $x = 3$ nm for various gate voltages are simulated, and the results are shown in Figs. 4–6 for regions I, II, and III, respectively. Moreover, the conduction band edges of the heavily n^+-doped channel along the x-direction at $y = 1$ nm in regions I, II, and III are also individually

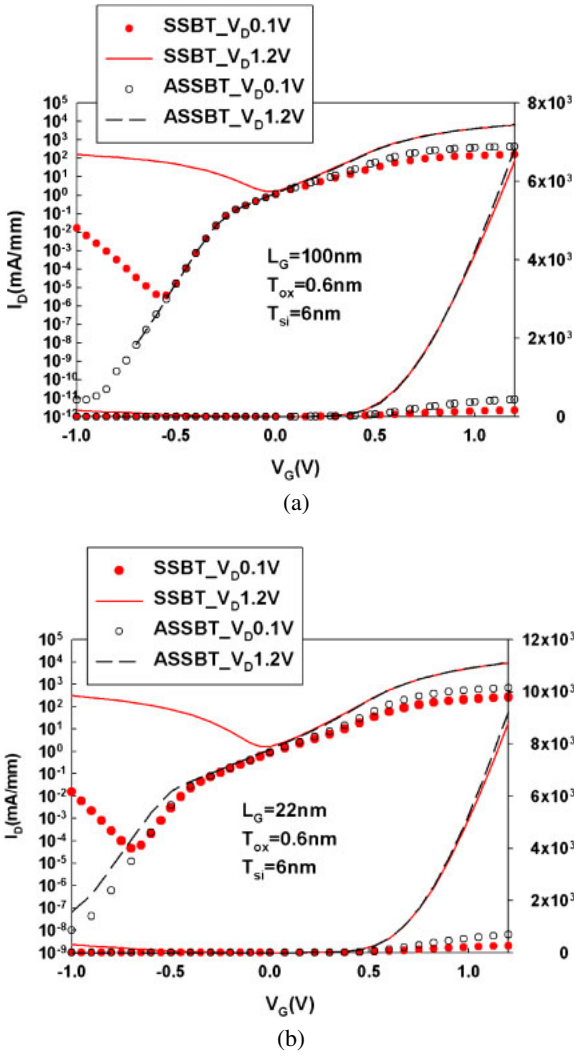


Fig. 2. (Color online) Comparison of the I_D–V_G characteristics between SSBT and ASSBT with channel lengths of (a) 100 and (b) 22 nm.

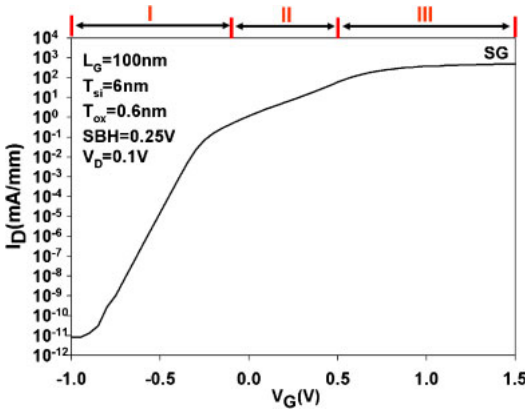


Fig. 3. (Color online) Operation regions presented in the I_D–V_G characteristics of an ASSBT.

shown in Figs. 4(c), 5(c), and 6(c), respectively, to explain the impact of the SB profile on device operation. Region I is the subthreshold region and, as shown in Figs. 4(a) and 4(b), the carrier concentration is significantly reduced while the strength of electric field in the channel near the source is not

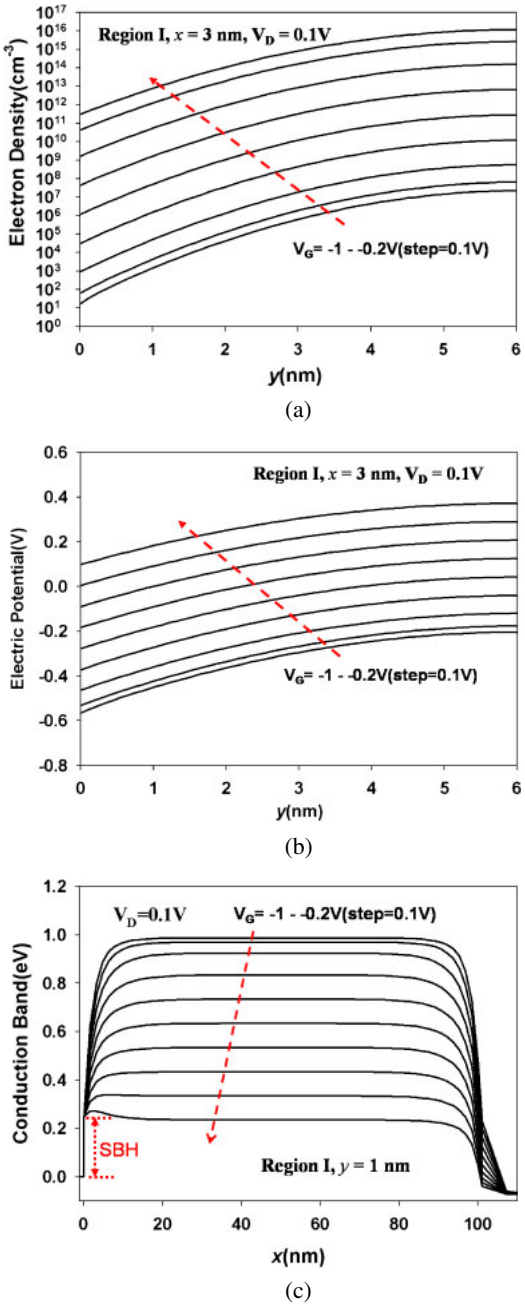


Fig. 4. (Color online) (a) Electron density and (b) electric potential through the silicon channel along the y-direction at $x = 3$ nm, and (c) the potential diagram along the x-direction while the ASSBT is operated in region I.

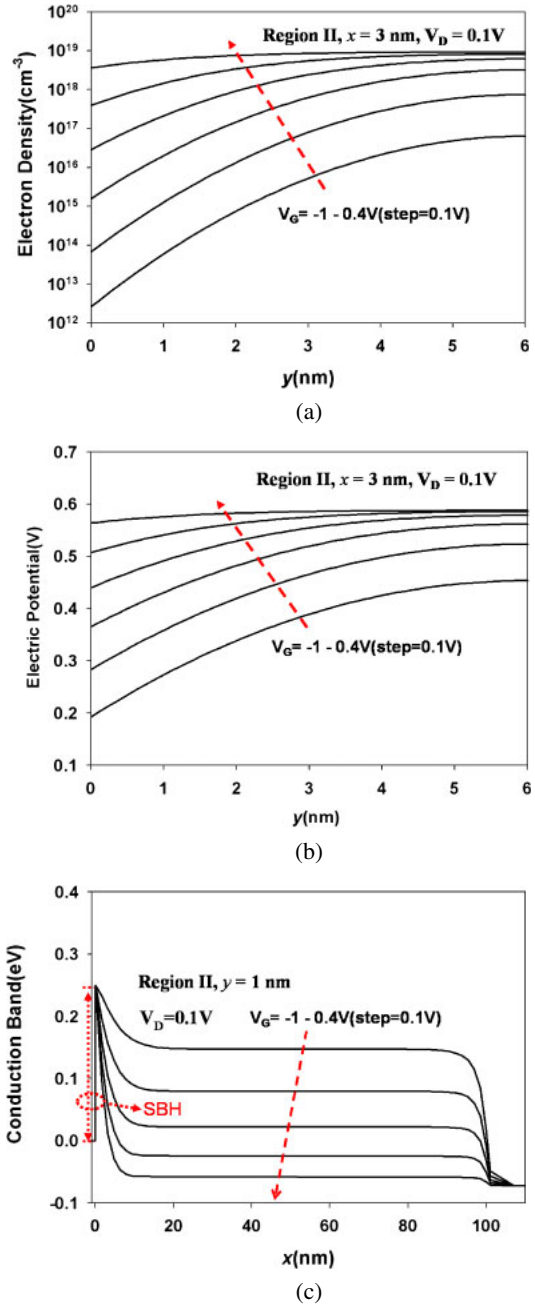


Fig. 5. (Color online) (a) Electron density and (b) electric potential through the silicon channel along the y-direction at $x = 3$ nm, and (c) the potential diagram along the x-direction while the ASSBT is operated in region II.

high. The potential barrier for electrons in the source, as shown in Fig. 4(c), is much larger than the Schottky barrier height (SBH) at the source/channel interface. Thus, the injection of electrons from the source to the channel is mainly governed by the thermionic emission, similar to that of conventional MOS devices operated in the subthreshold regime. Moreover, by using extra small channel thickness ($T_{si} = 6$ nm), a subthreshold swing (SS) close to the ideal value of 60 mV/dec is achieved. When gate voltage increases from region I to region II, which is also called the pseudo-subthreshold region, Fig. 5(a) shows the increase in carrier concentration accompanied by the increase in with the rise of electric potential, as shown in Fig. 5(b). In addition, as shown in Fig. 5(c), the potential at the channel center decreases to a level lower than the top of the SB; thus, its operational mechanism is determined by the thermionic field emission (TFE) in combination with thermionic emission and tunneling current,[17] as shown in Fig. 7. As can be noted in Fig. 5(c), the SBH is essentially not affected by gate voltage when operated in this region, so does the thermionic emission current component. On the other hand, the width of the barrier for the thermally activated electrons in the silicided SB source to the tunnel through as well as the potential at the channel center (Φ_1 in Fig. 7) is effectively modulated by gate voltage. As a result, the TFE current dominates the conduction in region II, resulting in a larger SS.

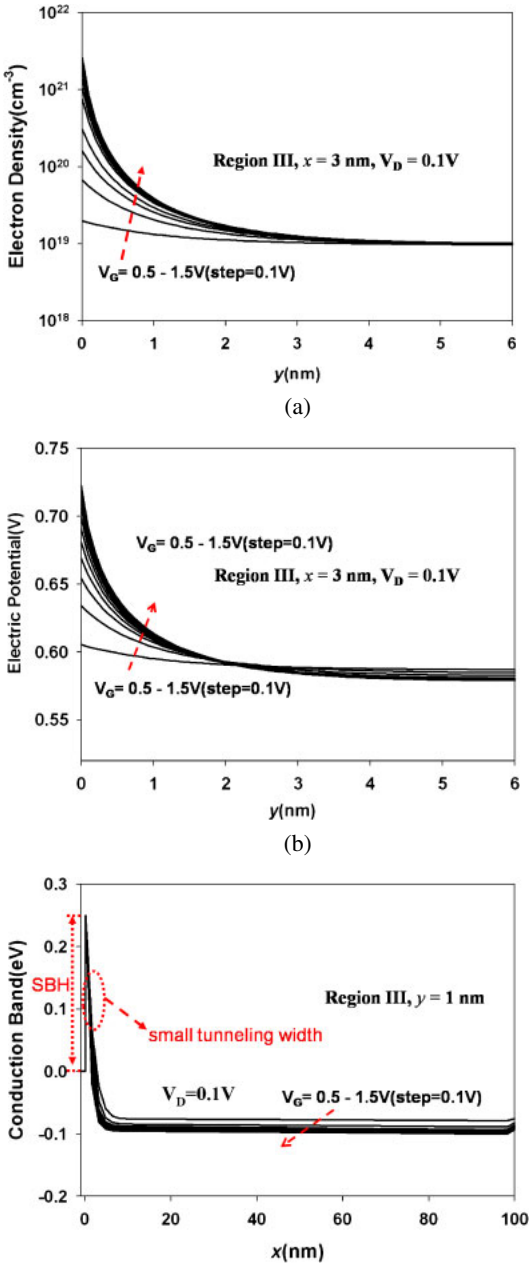


Fig. 6. (Color online) (a) Electron density and (b) electric potential through the silicon channel along the y-direction at $x = 3$ nm, and (c) the potential diagram along the x-direction while the ASSBT is operated in region III.

As the gate voltage increases further and reaches beyond flat-band voltage, the device is switched from region II to region III (i.e., the on-state) where a large number of electrons accumulate near the interface between the channel and gate oxide, as shown in Fig. 6(a). Under such a condition the tunneling barrier is so thin that the tunneling mechanism overwhelms the thermionic process. However, as gate voltage further increases, the tunneling width of the SB junction is not modulated effectively anymore, as illustrated in Fig. 6(c); therefore, the transport current of ASSBT gradually saturates.

3. Impacts of T_{ox} and T_{si} on SS

In the above section, we show that the ASSBT exhibits an

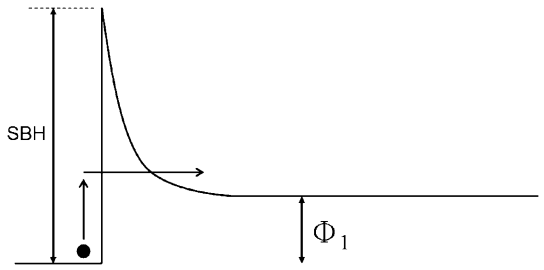


Fig. 7. Band diagram of the ASSBT operated in region II showing the thermionic field emission process.

inferior SS in region II owing to the inefficient modulation of barrier height and the tunneling width of the SB junction. Since the SBH is 0.25 eV and is difficult for the gate bias to modulate, it is therefore desirable to enhance the capability of the gate bias in modulating the tunneling width of SB. In this section, we will demonstrate how a thinner channel and/or a thinner effective gate oxide yields improvement of SS in region II. Figures 8(a) and 8(b) show the I_D–V_G characteristics of ASSBTs with various channel and gate oxide thicknesses, respectively. SS extracted from region II of the transfer curves for devices with channel thicknesses varying from 4 to 10 nm is plotted as a function of T_{ox} in Fig. 8(c). It can be seen that SS is improved as channel and gate oxide thicknesses decrease. The decrease in SS with decreasing T_{si} could be understood from the results shown in Fig. 5(b). In this figure, we can observe that the modulation of the potential by the gate bias is weakened in a deeper position. A reduction in channel thickness could thus enhance the overall gate controllability in modulating the tunneling width of the SB. A reduction in oxide thickness may have the same effect; thus, the SS is improved.

Similar trends were also observed in conventional inversion-mode SB transistors.[18–20] According to the previous studies, the electrostatic problem of conventional fully depleted inversion-mode SB MOSFETs could be solved by a simple 1D differential equation, which is expressed as[18,19]

$$\frac{d^2\Phi(x)}{dx^2} - \frac{\Phi(x) - V_g + V_{bi}}{\lambda^2} = \frac{\rho_{tot}(x)}{\varepsilon_{si}}, \quad (1)$$

$$\lambda = \sqrt{T_{si}T_{ox}\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}\right)}, \quad (2)$$

where $\Phi(x)$, V_{bi}, V_g, and ρ_{tot} are the electric potential, build-in potential, applied gate voltage and mobile charges, respectively. λ is the scaling length and describes how the potential variation is exponentially screened. According to eqs. (1) and (2), decreases in T_{si} and T_{ox} lead to a smaller λ, which would in turn reduce the tunneling width of the SB and improve SS. For heavily n^+-doped-channel ASSBT, the concept of scaling length "λ" is still suitable to describe the impact of T_{si} and T_{ox} on SS while the device is operated in region II. However, a modification of λ is essential. From Fig. 5(a), it can be seen that the location of maximum electron concentration is deep in the channel. This is in contrast to the case of conventional inversion-mode SB MOSFET, and suggests that the effective gate oxide thickness is large for the n-type ASSBT with a heavily n^+-

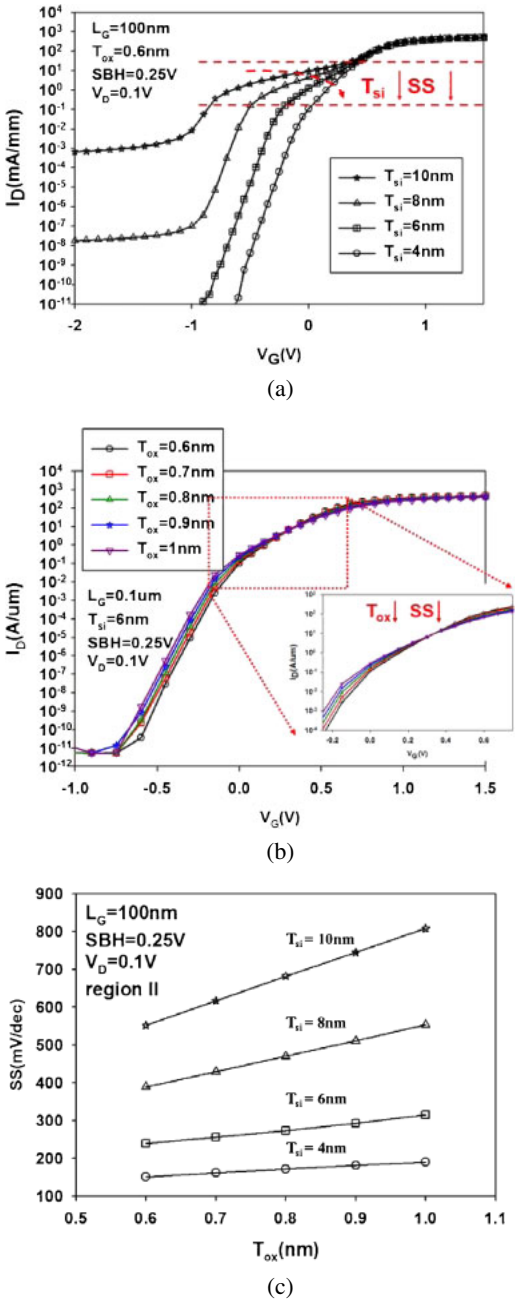


Fig. 8. (Color online) I_D–V_G characteristics of ASSBTs with various (a) T_{si} and (b) T_{ox}. and (c) SS versus T_{ox} with T_{si} as a parameter for ASSBTs operated in region II.

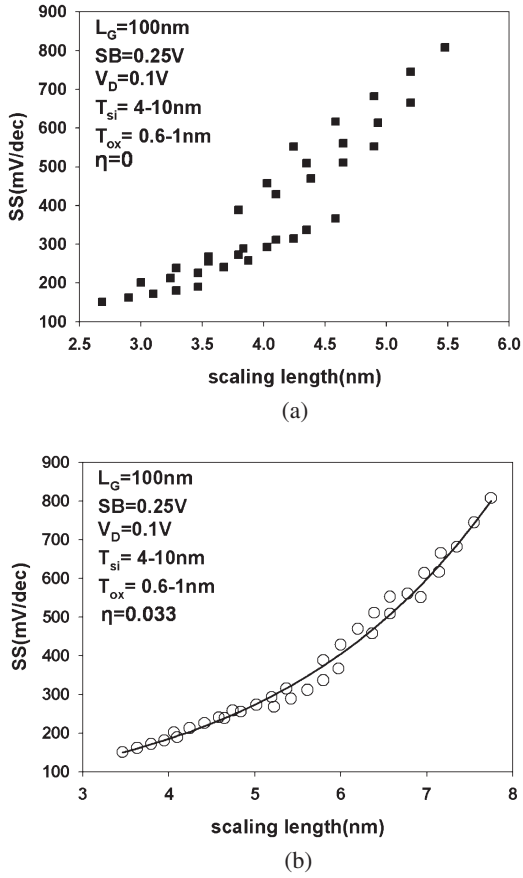


Fig. 9. SS versus λ with (a) $\eta = 0$ and (b) $\eta = 0.3$. In (b), the data are described well by a fitting curve.

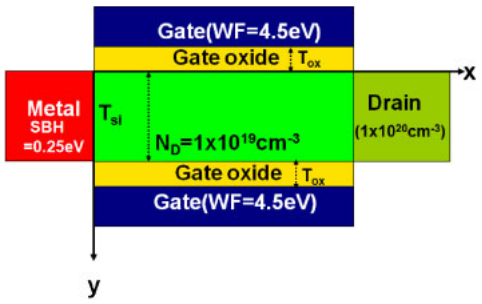


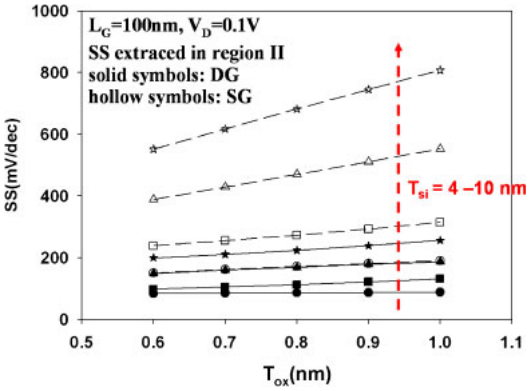
Fig. 10. (Color online) Schematic diagram of the DG ASSBT with SBH = 0.25 eV.

doped channel. An empirical form for the modified λ can be expressed as:

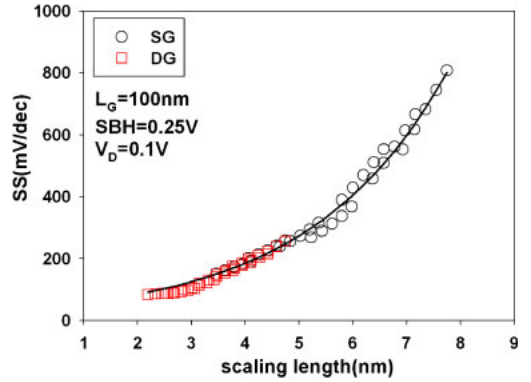
$$\lambda = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} T_{si}\left(\eta \frac{\varepsilon_{ox}}{\varepsilon_{si}} T_{si} + T_{ox.}\right)}, \quad (3)$$

where η is the fitting parameter used to reflect the effective thicker gate oxide. If no modification is carried out on the effective gate oxide thickness for heavily n^+-doped channel ASSBTs (i.e., $\eta = 0$), the plot of SS versus λ of heavily n^+-doped-channel ASSBTs with various T_{si} and T_{ox} cannot be arranged in the same regression curve, as shown in Fig. 9(a). However, as shown in Fig. 9(b), as the above mentioned modified form for λ ($\eta = 0.3$) is implemented, the concept of λ can work well again to reflect the influence of gate oxide and channel thicknesses on SS in region II.

In order to further improve the SS of the ASSBT in region II, double-gated (DG) configuration is also investigated. Figure 10 shows a plot of the schematic 2D structure of the DG ASSBT with a heavily n^+-doped channel. The comparison of SS between DG and SG devices is shown in Fig. 11(a), where the thicknesses of gate oxide and silicon channel are varied from 0.6 to 1 nm and 4 to 10 nm, respectively. Owing to the stronger gate control ability, significant improvement of SS is demonstrated for the DG configuration. Figure 11(b) shows the plot of SS versus λ of heavily n^+-doped channel DG ASSBT, together with the results of devices with a SG configuration. It can be



(a)



(b)

Fig. 11. (Color online) (a) Comparison of SS between SG and DG ASSBTs with various T_{si} and T_{ox}. (b) SS versus λ for SG and DG ASSBTs with $\eta = 0.3$.

noted that both DG and SG configurations fit in the same regression curve, which means that the concept of λ works well regardless of the gate configuration. Note that T_{si} in eq. (3) is corrected to $T_{si}/2$ for DG configuration.

4. Conclusions

The new n-type ASSBT structure studied in this work, which features the SB source and junctionless-like drain, distinguishes itself from all the previously reported ASSBTs in the new junctionless-drain feature, combined with the fully depleted thin-film channel cannot only suppress off-state leakage but also eliminate the steps and issues associated with the formation of p–n junctions. Through TCAD simulation, we have explored the operation of the new ASSBT. As compared with the SSBT equipped with symmetrical silicided SB S/D, it is confirmed that the new ASSBT exhibits much reduced off-state current and improved on-current. The dominant conduction mechanisms of the ASSBT are also studied. In addition to the subthreshold and on-state regions, a pseudo-subthreshold region in which thermionic field emission conduction process dominates is identified. A reduction in either the channel or gate oxide thickness contributes to the reduction of reducing the SS of pseudo-subthreshold region. Finally, the concept of scaling length (λ) is adopted but with a modified empirical form to reflect the impacts of gate oxide and channel thicknesses on the characteristics of the devices.

Acknowledgments

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