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High-Performance Excimer-Laser-Crystallized Polycrystalline Silicon Thin-Film Transistors with the Pre-Patterned Recessed Channel

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High-performance polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have been achieved using an excimer laser crystallization method on a prepatterned recessed channel (RC). Such a prepatterned RC TFT exhibited an excellent field-effect mobility of 412 $cm^2 V^{-1} s^{-1}$ and an on/off current ratio higher than 1.1×10^8 as compared with 125 $cm^2 V^{-1} s^{-1}$ and 2.2×10^7 for the conventional ones, respectively. This is attributed to the two-dimensional control of the grain boundary location and the resultant cross-shaped grain boundary structures within the recessed regions. Therefore, the prepatterned RC TFTs with only one grain boundary parallel to the channel direction as the TFTs could be fabricated to avoid the perpendicular grain boundary. This technology is thus promising for the future applications of poly-Si TFTs in the system-on-panel (SOP) and three-dimensional integrated circuits (3D-ICs). © 2012 The Japan Society of Applied Physics

1. Introduction

High-performance low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) were key devices in the production of high-quality active-matrix flat panel displays (AMFPDs) and three-dimensional integrated circuits (3D-ICs)[1–3] using inexpensive glass substrates. The excimer laser crystallization (ELC) of amorphous silicon (a-Si) was proven to be a promising method for the LTPS TFT fabrication.[4] It has been reported that the grain size could be increased to improve the device performance through the lateral grain growth by laser recrystallization after pre-patterning the a-Si films.[5–7] However, the small-dimensional TFTs fabricated by the crystallization method exhibited a higher mobility but with the poor uniformity of the device performance because grain boundaries were randomly distributed and were a critical issue for scale down to achieve the SOP with the integrated TFT circuits and 3D-ICs. Thus, various grain-boundary-controlled methods via the laser crystallization of a prepatterned active layer, such as the adoption of an air gap structure[8,9] and a light absorption layer[10] have been proposed. However, these methods required complex fabrication processes to control the locations of grain boundaries two-dimensionally.

In our previous work, the laser crystallization with an unpatterned recessed channel (RC) has been reported and demonstrated to produce 1D location-controlled grain boundaries.[11] The purpose of this study was to demonstrate the laser crystallization on a prepatterned RC that enables the 2D location control of the grain boundaries. Via the prepatterned RC structure, the polycrystalline silicon (poly-Si) TFTs could be successfully fabricated with only one parallel grain boundary along the channel direction. Consequently, the RC-structured TFTs exhibited not only superior device performance but also much better device-to-device uniformity than the conventional ones.

2. Experimental Procedure

The schematic diagram of the prepatterned RC TFT via the proposed crystallization method is shown in Fig. 1. First, a 1000-Å-thick a-Si thin film was deposited on an oxidized silicon substrate using a low-pressure chemical vapor deposition (LPCVD) system at 550 °C and then patterned as

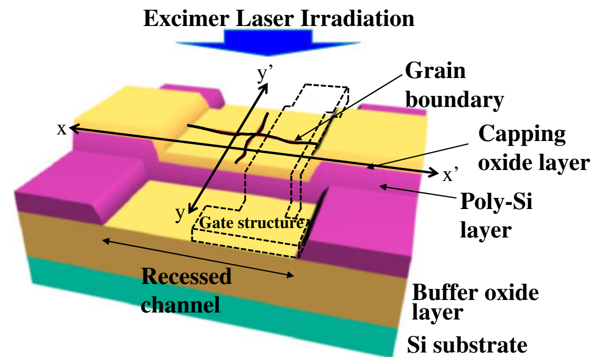

Fig. 1. (Color online) Schematic diagram of the prepatterned RC TFT via the proposed crystallization method.

strips with an interspacing of 1.5 µm. Subsequently, another a-Si thin film with a thickness of 1000 Å and a thin capping oxide layer with a thickness of 500 Å that prevents the a-Si from ablation during laser irradiation were deposited by LPCVD at 550 °C. Next, the capping oxide layer and a-Si thin film were etched to form the active channel perpendicularly to the patterned a-Si strip islands. Then, laser crystallization was performed using a KrF excimer laser ($\lambda = 248$ nm) in a vacuum chamber pumped down to 10^{-3} Torr at room temperature. The laser was controlled with a laser density of 320 mJ/cm^2 and 20 shots, i.e., 95% overlapping. After the laser irradiation and capping oxide removal, a 1000-Å-thick tetraethyl orthosilicate (TEOS) gate oxide was deposited by LPCVD and subsequently an *in-situ* phosphorus doped poly-Si layer with a thickness of 2000 Å was deposited by LPCVD as the gate electrode. Then, the poly-Si and gate oxide layers were etched to form the gate structure. To obtain the high-performance electrical characteristics, the channel region was placed to be away from the primary grain boundary perpendicular to the channel direction. Then, self-aligned phosphorus ion implantation (5×10^{15} cm^{-2}, 40 keV) was carried out to form the source and drain regions. Next, a passivation oxide layer was deposited and the implanted dopants were activated by thermal annealing at 600 °C for 9 h in a furnace with the nitrogen ambient. Finally, contact hole opening, and metallization were completed to fabricate the proposed TFTs. For comparison, the conventional poly-Si TFTs

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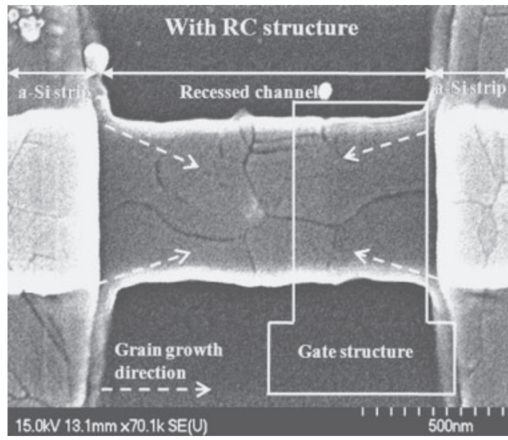
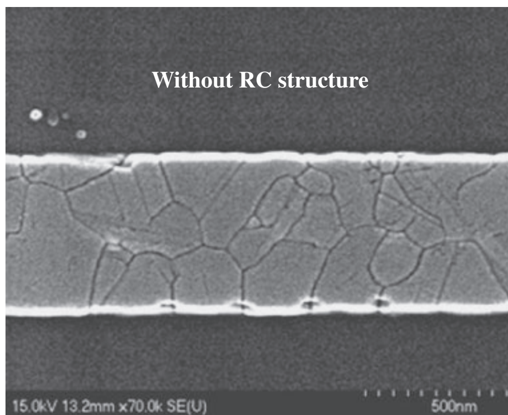


(a)



(b)

Fig. 2. Plan views of Secco-etched SEM images of the grain structure after laser irradiation on the prepatterned silicon thin films (a) with and (b) without RC structure.

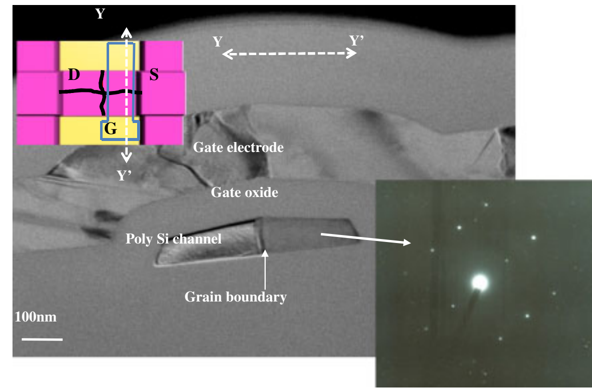


Fig. 3. (Color online) Cross-sectional TEM image of the prepatterned RC TFT. The insets show the schematics of the prepatterned RC TFT with the FIB cutting direction Y–Y' and [113] electron diffraction pattern for one of the two grains in the channel.

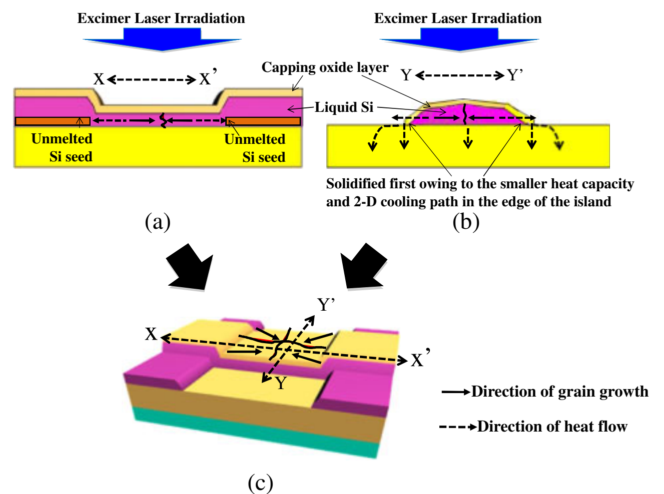


Fig. 4. (Color online) Illustration of the mechanism of the laser crystallization method on the prepatterned RC that leads to 2D location-controlled grain boundary formation.

without the RC structures were also fabricated as reference samples.

3. Results and Discussion

Figures 2(a) and 2(b) show the Secco-etched scanning electron microscopy (SEM) images of the grain structure after laser irradiation on the prepatterned silicon thin films with and without the RC structure, respectively. In the case of the prepatterned silicon thin film with the RC structure, as shown in Fig. 2(a), four grains impinged at the center of the recessed region and a cross-shaped grain boundary with one perpendicular and one parallel to the channel direction can be formed in the recessed region. As the gate structure is located at one side of the cross-shaped grain boundary structure, the channel region can be controlled to contain one parallel grain boundary, shown as the white-line area. In contrast, in the prepatterned silicon thin film without the RC structure, as can be seen in Fig. 2(b), many uncontrolled nucleation sites are formed along the edge of the prepatterned active layer and grow toward the center. Therefore, the location and size of the grains are randomly distributed.

Figure 3 displays the cross-sectional TEM image of the prepatterned RC TFT. The image indicates that only one grain boundary is parallel to the channel direction in the channel and the edge of the channel layer is thinner than the central region. The grain structure is determined using its electron diffraction pattern to be [113]-orientated for one of the two grains in the channel, reflecting its high crystallinity. The mechanism of the crystallization method is therefore illustrated in Fig. 4. As shown in Fig. 4(a), when an proper laser energy density irradiation, the recessed region completely melts and the thick a-Si region only partially melts; thus, a significant lateral thermal gradient along the X–X' direction occurs.[12] In the meantime, the lateral thermal gradient along the Y–Y' direction also exists owing to the surface tension effect and the 2D cooling path during laser irradiation. The cooling rate of the edge region is faster than that of the central region and leads to solidification first because of the smaller heat capacity of the thinner silicon thin film[8,9] and 2D cooling path,[10] as shown in Fig. 4(b). Figure 4(c) illustrates that the spatially 2D thermal gradient can therefore lead to the lateral grain growth from the solid portions toward the melted recessed region and form the cross-shaped grain boundary structure in the recessed region.

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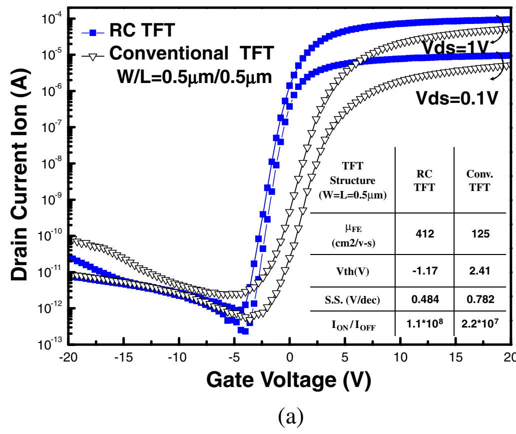
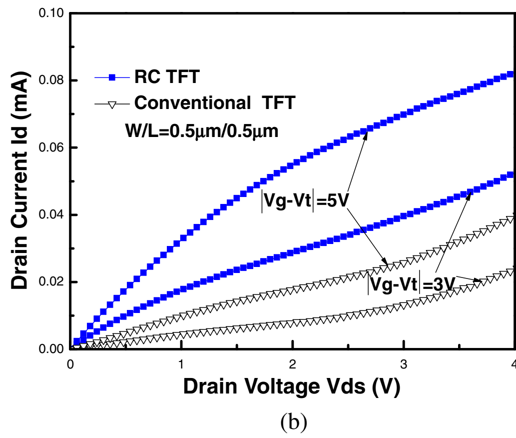
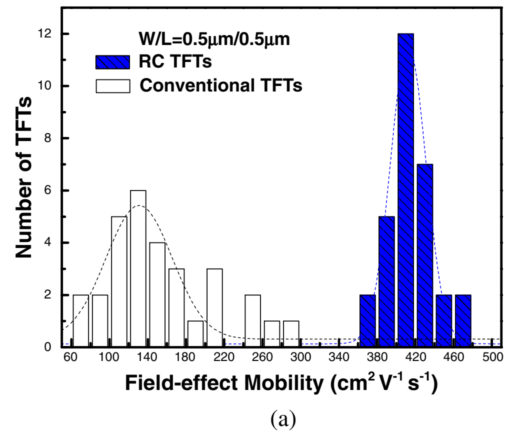


(a)

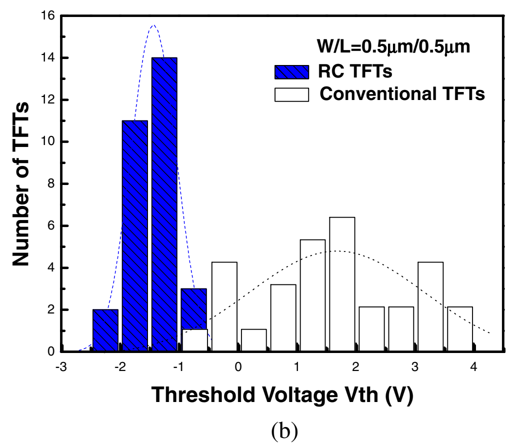


(b)

Fig. 5. (Color online) (a) Transfer and (b) output characteristics of the prepatterned RC and the conventional TFTs with $W = L = 0.5\,\mu\text{m}$.



(a)



(b)

Fig. 6. (Color online) Measured (a) field-effect mobility and (b) threshold voltage distributions of the prepatterned RC and the conventional TFTs with $W = L = 0.5\,\mu\text{m}$.

Typical transfer and output characteristics of the pre-patterned RC and conventional TFTs for $W = L = 0.5\,\mu\text{m}$ are shown in Figs. 5(a) and 5(b), respectively. The inset table summarizes the several important parameters of the device characteristics of these two different TFT structures. The field-effect mobility (μ_{FE}) and subthreshold swing (SS) are evaluated from the linear region at $V_{\text{ds}} = 0.1$ V, and the on/off current ratio is defined at $V_{\text{ds}} = 1$ V. The threshold voltage (V_{th}) is defined according to the normalized drain current of $I_{\text{ds}} = (L/W) \times 10^{-8}$ at $V_{\text{ds}} = 0.1$ V. Obvious improvements in the device characteristics are obtained for the pre-patterned RC TFTs than for the conventional ones. The prepatterned RC TFTs attain an excellent field-effect mobility of $412\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, low subthreshold swing of 0.484 V/dec, and high on/off current ratio of 1.1×10^8, whereas the conventional ones show a field-effect mobility of $125\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, subthreshold swing of 0.782 V/dec, and an on/off current ratio of 2.2×10^7 accordingly. The superior performance of the prepatterned RC TFTs is attributed to the presence of only one parallel grain boundary along the channel direction, owing to the location-controlled grain boundaries via the proposed crystallization method. To investigate the uniformities of prepatterned RC and conventional TFTs, thirty TFTs are measured. Figures 6(a) and 6(b) show the field-effect mobility and threshold voltage distributions of these two different TFTs with $W = L = 0.5\,\mu\text{m}$. It can be observed that the prepatterned RC TFTs exhibit a relatively smaller deviation in field-effect mobility (from 372 to $465\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$) than the conventional ones (from 68 to $286\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$). The threshold voltage dispersion of the prepatterned RC TFTs (from -0.60 to -2.33 V) is also much smaller than that of the conventional ones (from -0.80 to 3.95 V). It is generally believed that the field-effect mobility and threshold voltage deviations can be due to the grain boundary and defects inside the channel. Therefore, the prepatterned RC TFTs will show a superior device-to-device uniformity owing to the presence of only one parallel grain boundary along the channel direction. In contrast, the conventional ones have many defects and randomly distributed grain boundaries inside the channel region.

4. Conclusions

A 2D grain boundary location-controlled method via laser irradiation on a prepatterned recessed channel has been proposed to achieve the cross-shaped grain boundary structures. The prepatterned RC TFTs with only one grain boundary along the channel direction could therefore be fabricated to attain a field-effect mobility as high as 412 $\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ and an on/off current ratio higher than 1.1×10^8 as compared with $125\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ and 2.2×10^7 for the conventional ones, respectively. In addition, the prepatterned RC TFTs also exhibited a much more improved device uniformity than the conventional ones. This indicates that the proposed prepatterned RC TFTs are promising for application in SOP and 3D-ICs.

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Acknowledgments

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1) T. Tanaka, H. Asuma, K. Ogawa, Y. Shinagawa, K. Ono, and N. Konishi: IEDM Tech. Dig., 1993, p. 389.
2) Y. I. Park, T. J. Ahn, S. K. Kim, J. Y. Park, J. S. Yoo, C. Y. Kim, and C. D. Kim: SID Symp. Dig. Tech. Pap. **34** (2003) 487.
3) J. H. Park, P. Krishna, K. C. Saraswat, and H. Peng: Appl. Phys. Lett. **91** (2007) 143107.
4) J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider: J. Appl. Phys. **53** (1982) 1193.
5) M. Cao, S. Talwar, K. J. Kramer, T. W. Sigmon, and K. C. Saraswat: IEEE Trans. Electron Devices **43** (1996) 561.
6) G. K. Giust and T. W. Sigmon: J. Appl. Phys. **81** (1997) 1204.
7) G. K. Giust and T. W. Sigmon: IEEE Electron Device Lett. **18** (1997) 296.
8) C.-H. Kim, I.-H. Song, W.-J. Nam, and M.-K. Han: IEEE Electron Device Lett. **23** (2002) 315.
9) I. H. Song, S. H. Kang, W. J. Nam, and M. K. Han: IEEE Electron Device Lett. **24** (2003) 580.
10) M. Ozawa, C. H. Oh, and M. Matsumura: Jpn. J. Appl. Phys. **38** (1999) 5700.
11) H. C. Cheng, L. J. Cheng, C. W. Lin, Y. L. Lu, and C. Y. Chen: AMLCDs Tech. Dig., 2000, p. 281.
12) C. W. Lin, L. J. Cheng, Y. L. Lu, Y. H. Lee, and H. C. Cheng: IEEE Electron Device Lett. **22** (2001) 269.

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