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Semicond. Sci. Technol. 27 (2012) 065010 (9pp) doi:10.1088/0268-1242/27/6/065010

A study on low-power, nanosecond operation and multilevel bipolar resistance switching in $Ti/ZrO_2/Pt$ nonvolatile memory with 1T1R architecture

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Received 11 March 2012, in final form 31 March 2012
Published 3 May 2012
Online at stacks.iop.org/SST/27/065010

Abstract
Low-power, bipolar resistive switching (RS) characteristics in the $Ti/ZrO_2/Pt$ nonvolatile memory with one transistor and one resistor (1T1R) architecture were reported. Multilevel storage behavior was observed by modulating the amplitude of the MOSFET gate voltage, in which the transistor functions as a current limiter. Furthermore, multilevel storage was also executed by controlling the reset voltage, leading the resistive random access memory (RRAM) to the multiple metastable low resistance state (LRS). The experimental results on the measured electrical properties of the various sized devices confirm that the RS mechanism of the $Ti/ZrO_2/Pt$ structure obeys the conducting filaments model. In application, the devices exhibit high-speed switching performances (250 ns) with suitable high/low resistance state ratio (HRS/LRS > 10). The LRS of the devices with 10 year retention ability at 80 °C, based on the Arrhenius equation, is also demonstrated in the thermal accelerating test. Furthermore, the ramping gate voltage method with fixed drain voltage is used to switch the 1T1R memory cells for upgrading the memory performances. Our experimental results suggest that the ZrO_2-based RRAM is a prospective alternative for nonvolatile multilevel memory device applications.

(Some figures may appear in colour only in the online journal)

1. Introduction

As devices are scaling down, a flash memory device will also meet its physical limitation leading to unacceptable degradation of retention characteristic due to the increasing difficulty of retaining electrons in shrinking dimensions. Resistive random access memory (RRAM) is extensively studied and is expected to possibly replace the flash memory device owing to its advantages of high operation speed, long retention time, nondestructive readout, low operation voltage, multibit data storage and simple structure. Various material systems including ternary oxides of $SrZrO_3$ (SZO) [1–4], $SrTiO_3$ (STO) [5] and $Bi_4Ti_3O_{12}$ (BTO) [6] and binary oxides such as CuO [7–10], Al_2O_3 [11], NiO [12–14], TiO_2 [15–19], HfO_2 [20, 21] and ZrO_2 [22–30] were reported to exhibit excellent electrical properties in resistive switching (RS) memory application. It was also reported that Cu-doped ZrO_2 could appreciably improve the resistance ratio and show the forming-less characteristic, where ZrO_2 is regarded as solid electrolyte [27]. However, the metallic ionic conducting

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filaments system has a high temperature retention failure issue needing to be solved. Liu *et al* reported that the Au implanted ZrO_2 film exhibits lower forming voltage and stable resistive switching behavior, nevertheless the original resistance of the device decreases obviously and obstructs low-power memory application [28]. We have previously reported the influence of top electrode material on the resistive switching properties of ZrO_2-based memory film using Pt as a bottom electrode, where the inert bottom electrode does not react with resistive switching layer and simplify the system [22, 23]. In comparison with Pt/ZrO_2/Pt, Al/ZrO_2/Pt and W-probe/ZrO_2/Pt devices, where the broad dispersions of resistive switching characteristics in the W-probe, Pt and Al top electrode devices are generally observed during successive resistive switching, the Ti/ZrO_2/Pt device exhibits suppressed switching parameter dispersions. It is more important that the Ti top electrode changes the ZrO_2 system from nonploar resistive switching to excellent bipolar resistive switching characteristic. The influences of the Ti top electrode are further elucidated and we are convinced that an interfacial layer between Ti and ZrO_2 thin film is formed, where the induced interfacial layer can degrade the dielectric strength of the ZrO_2 further lowering the forming voltage and function as an oxygen reservoir to stabilize the bipolar resistive switching characteristic [25]. It is certain that the resistive switching mechanism is dominated by the formation and rupture of conduction filaments consisting of oxygen vacancies through the ZrO_2 thin film. However, the MIM structure devices still face the high reset current (I_{reset}, defined as the peak current during reset process) and high operation power issues, which are the main constraints for the commercialization [24, 25]. As mentioned in the work reported by Kinoshita *et al* [14], the I_{set} and I_{reset} of the RRAM depend on the parasitic capacitance from the RRAM device and the measurement system. They proposed a transient current flow through the parasitic capacitance during the set process so as to cause no parasitic capacitance contributing to the I_{set}/I_{reset} linear relationship. Recently, the serious compliance current overshoot phenomenon was found to significantly affect the RRAM behaviors, which are observed in the MIM structure device *in situ* [16, 19]. However, no compliance current overshoot was observed in the memory device with a transistor, which functioned as a perfect current limiter [10]. In the ZrO_2-based devices, the 1T1R devices with Pt top electrode and P^+ Si bottom electrode were fabricated and showed submicroampere reset current behavior [29]. Furthermore, according to our previous work, the forming voltage and the original leakage current of the Ti/ZrO_2/Pt RRAM devices can be modulated by controlling the thickness of the Ti top electrode [25]. Then, we fabricated the Ti/ZrO_2/Pt-based RRAM, connected with an internal transistor, to investigate its original electrical properties without the compliance current overshoot behavior. The bipolar resistive switching devices show low switching voltage (set/reset, 0.8/−1 V), the lowest operation current for ZrO_2-based RRAM devices (20 μA) and reliable data retention for LRS [30]. In this work, we perform more extensive electrical characterizations of the Ti/ZrO_2/Pt-based RRAM with 1T1R architecture, and provide the results about electrical properties and reliability of the devices in more detail. It confirms that the RS mechanism obeys the rupture and formation of conducting filaments based on electrical measurement results. The devices with different sizes are also fabricated to verify the conducting filament model. It reveals the considerable scaling potential of ZrO_2-based RRAM. The pulse measurement results show that the devices have high-speed switching behavior. Moreover, a few works have paid attention to the thermal instability of operation parameters of RRAM devices [21, 31], especially for the multibit storage devices. Therefore, the thermal instability of Ti/ZrO_2/Pt-based 1T1R memory cells is investigated to provide key insight into operation parameters of the devices, including operation voltage and LRS resistance. Furthermore, we also perform the alternative operation methodology for studying 1T1R memory cells, which switches the cells by the ramping gate voltage method with a fixed drain voltage.

2. Experiment

A RRAM device consisting of a Ti/ZrO_2/Pt/Ti stack was integrated in a standard CMOS architecture, where the memory cell was fabricated under the drain (or source) side contact hole of the n-type control transistor. After the contact hole formation process by I-line lithography and dry etching, the Ti adhesion layer (5 nm) and Pt thin film (80 nm) were deposited on the drain (or source) in sequence by electron-beam evaporation at room temperature, and patterned by the I-line lithography system and lift-off process. Subsequently, a 19 nm-thick ZrO_2 layer was deposited using a radiofrequency (rf) magnetron sputtering at 200 °C. The detailed fabrication process for the ZrO_2 memory cells can be found elsewhere [24]. Finally, a 150 nm thick Ti top electrode pad was grown on ZrO_2 by electron beam evaporation at room temperature and patterned through the lift-off photolithographic process to complete the Ti/ZrO_2/Pt/Ti RRAM devices. For implementing the size effect test, the contact holes with various areas ranging from 1 to 22 500 $(\mu\text{m})^2$ were formed by using I-line lithography and dry etching to fabricate the various sized device cells. Besides, the channel width and length of the transistor are 48 and 5 μm, respectively, to supply the sufficient operation current for the set and reset processes. Finally, the ZrO_2 thin films on the gate and source (or drain) side contact holes were also removed by lithography and dry etching processes. The electrical characterizations were performed using the Keithley 4200 semiconductor characterization system in dc and ac operation modes.

3. Results and discussion

3.1. I–V characteristics of a Ti/ZrO_2/Pt-based 1T1R memory cell

During the forming or set process, switching the RRAM from fresh state to LRS, the positive voltage is applied on the gate and drain; meanwhile, the source is grounded. It is noted that the original leakage current of the RRAM is below 0.1 μA at

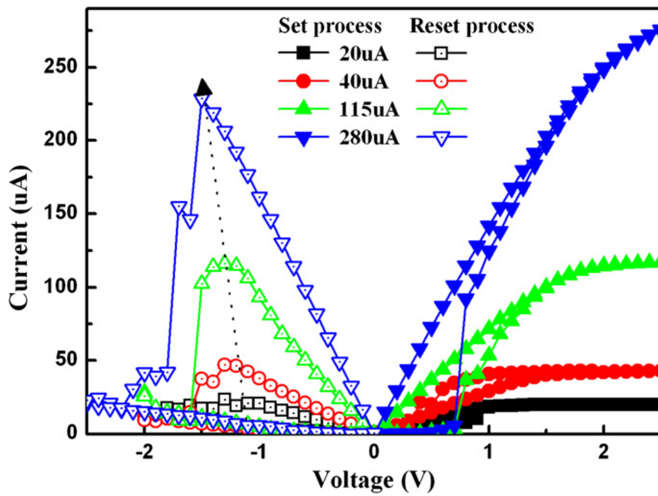


Figure 1. Typical *I–V* curve of multilevel resistance switching characteristic for the Ti/ZrO_2/Pt 1T1R RRAM.

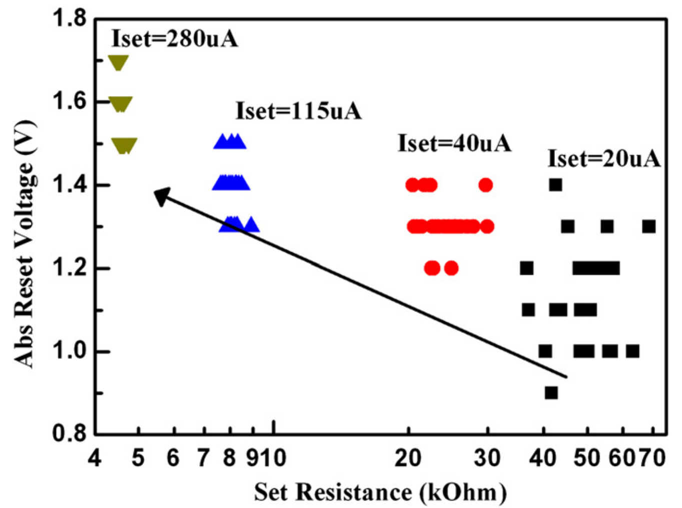


Figure 2. Relationship between the reset voltage and set currents ranging from 20 to 280 μA.

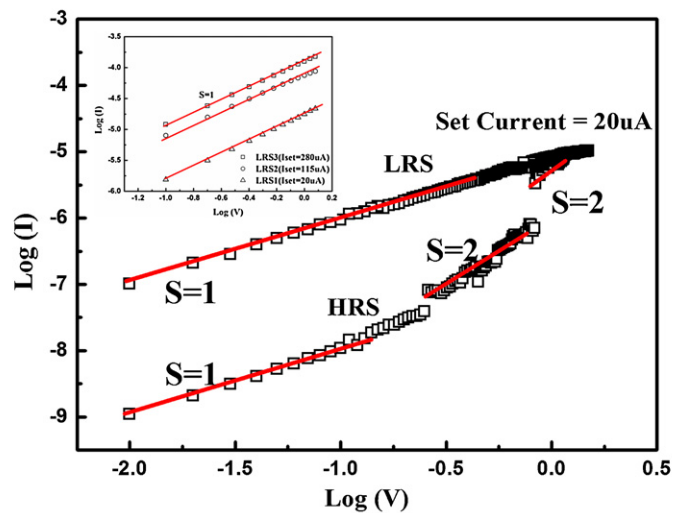


Figure 3. *I–V* characteristics of the set process in a double-logarithmic plot. The inset shows the *I–V* characteristics of each LRS state in a double-logarithmic scale.

1 V read voltage (data not shown), providing the possibility for low operation current. After the forming process, the RRAM device can be switched between LRS and HRS. During the reset process, the positive sweeping voltage is applied on the source with constant bias of 2 V on gate, and the drain is grounded. The operation method for this measurement is as follows: when positive bias is applied on the source and the drain grounded, it is similar to applying negative bias at the drain. Meanwhile, the constant gate voltage decides the current value from MOSFET, which is much larger than the reset current for the reset process. Figure 1 shows the typical *I–V* switching characteristics of the 1T1R architecture device, where the transistor functions as a perfect current limiter. Small set and reset currents, as low as 20 μA, are observed and the operation voltage down to 1 V, indicating that the ZrO_2-based RRAM is not only suitable for low-voltage application but also appropriate for a low-power logic circuit. Furthermore, figure 1 also shows that the RRAM can be switched to multiple levels of R_{LRS} by controlling the set currents ranging from 20 to 280 μA via modulating the gate voltage of the transistor. It is noted that the I_{set} is comparable to I_{reset} at all LRS owing to the excellent current limiter. This phenomenon is similar to the reported result [10]. As another noteworthy aspect of the switching property, the high I_{set} leading to the slightly higher reset voltage (V_{reset}) was observed. To study the phenomenon in detail, the relationship of I_{set} with V_{reset} is established and shown in figure 2, where the measured data were collected from the operation process repeated 20 times. Figure 2 demonstrates the dependence of V_{reset} on the I_{set}, indicating that the higher I_{set} leads to higher V_{reset}. It can be proposed that the higher I_{set} induces the formation of stronger and larger sized conducting filaments in the resistance switching thin film, so that in turn it requires larger V_{reset} and I_{reset} for their rupture. To further elucidate the resistive switching mechanism of the devices, the curve fitting is performed for the set region of the initial *I–V* characteristics of the 1T1R devices, and the double-logarithmic scale plots are shown in figure 3. The conduction mechanism in HRS of the 1T1R devices agrees with the Ohmic conduction (slope = 1) in the low-voltage region, which indicates that the number of thermal-generated free carriers within the ZrO_2 thin film is larger than that of the injected charge carriers. In the high-voltage region, the conduction mechanism follows the space charge limited current (SCLC, slope = 2) theory, which is caused by the injected excess carriers dominating over the thermal-generated free carriers, where the SCLC conduction is controlled by the shallow traps. In even higher voltage regions, the *I–V* characteristics maintain at the slope of 2 due to the trapping centers occupied by the injected carriers, creating a space charge near the electrode and then resulting in a field to impede further carrier injection trap-filled SCLC. Moreover, as the voltage increases, the filaments are completely formed leading to the *I–V* characteristics of the LRS with slope 1. Therefore, the LRS is dominated by Ohmic conduction (slope = 1), which indicates that the switching process from HRS to LRS is caused by the conducting filaments formed within the ZrO_2. Furthermore, the *I–V* curves of various LRS levels were also

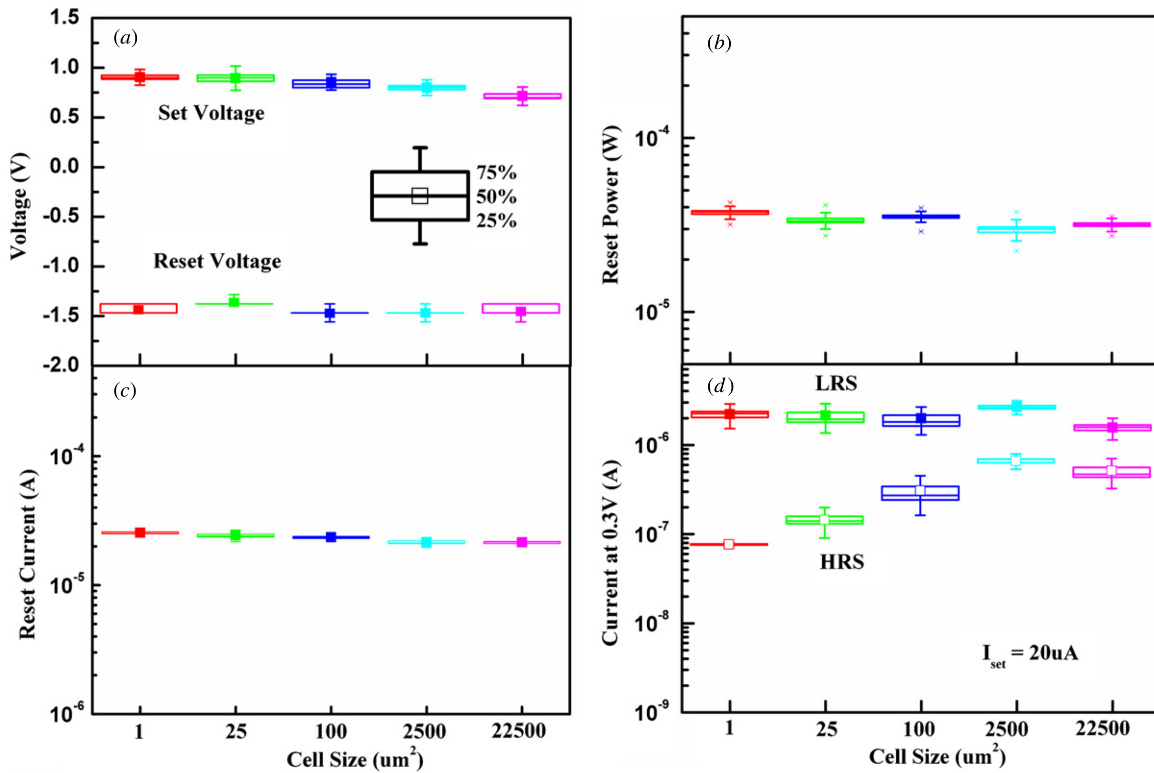


Figure 4. Statistical charts for the variations of the operation voltage, reset current, reset power and LRS/HRS current with cell sizes ranging from 1 to 22 500 (μm)^2.

replotted in a double-logarithmic scale to confirm the conduction mechanism of each LRS level, as displayed in the inset of figure 3. The conduction mechanism of each LRS level ranging from I_{set} = 20 to 280 μA essentially obeys Ohmic conduction. The 1T1R devices operated in the low voltage region exhibit the same carrier conduction behavior as that in the Ti/ZrO_2/Pt MIM structure devices reported in our previous paper [24]. That is, the rupture and formation of conducting filaments near the interface of Ti/ZrO_2 can be employed to well explain the set/reset process of our devices, where the interface layer between Ti and ZrO_2 was reported as an effective oxygen reservoir [25]. To further confirm the RS mechanism of the ZrO_2-based RRAM dominated by the conducting filament model, the relationship between the electrical properties and the geometrical size of the device cells is established and shown in figures 4(*a*)–(*d*). The operation parameters including operation voltage, reset current and reset power are independent of the cell size, as shown in figures 4(*a*)–(*c*). It is clearly observed that the resistance in LRS is independent of the cell size, as shown in figure 4(*d*), indicating that the current is distributed as locally confined filament paths formed in the ZrO_2 matrix [26, 32]. In contrast, the HRS resistance decreases slightly with an increase of the cell size, which shows that the ZrO_2 film still has residual tiny filaments after the reset process, as shown in figure 4(*d*). It was reported that the resistances in LRS and HRS were increased with an increase of cell size, belonging to the bulk switching behavior and not the localized conducting filament mechanism [18]. Furthermore, their experimental results on current–voltage relationship show that the resistance switching mechanism belongs to trap-filled/unfilled space-charge-limited-current (SCLC) model. However, our size effect test results indicate that the resistance of LRS does not depend on the size of the memory cells, which are in good agreement with the faucet model [33] and not consistent in the reported result [18]. We believe that the localized conducting filaments dominate the switching behavior of our memory devices, although the conduction mechanism in the high voltage region of the HRS follows the unfilled-shallow traps SCLC theory based on the curve fitting results of the relationship between current and voltage. On the other hand, the resistance in HRS only slightly depends on the memory cell size in reverse proportion, while the resistance in LRS is independent of cell size, which reveals promising scaling down prospect for ZrO_2-based devices. It is worth pointing out that the set/reset voltage and reset power ($P_{reset} = I_{reset} \times V_{reset}$) are independent of the memory cell size, and the ultra-low reset current/power is obtained down to 20 μA/20 μW with I_{set} = 20 μA condition, respectively. In addition, we also demonstrate that the multilevel resistance states of ZrO_2-based RRAM with 1T1R architecture can be obtained by carefully controlling the reset voltage. The devices can be switched to the intermediate states, locating between LRS and HRS owing to various size and number of conducting filaments through the ZrO_2 film caused by different reset stop voltages, as shown in figure 5(*a*). It indicates that the first sweep is applied on the source with reset voltage from 0 to 1.1 V, which is denoted as V_{stop} = 1.1 V, leading to the ZrO_2-based RRAM being switched from LRS to an intermediate state. Such an intermediate state is stable until the second voltage sweep with V_{stop} = 1.2 V

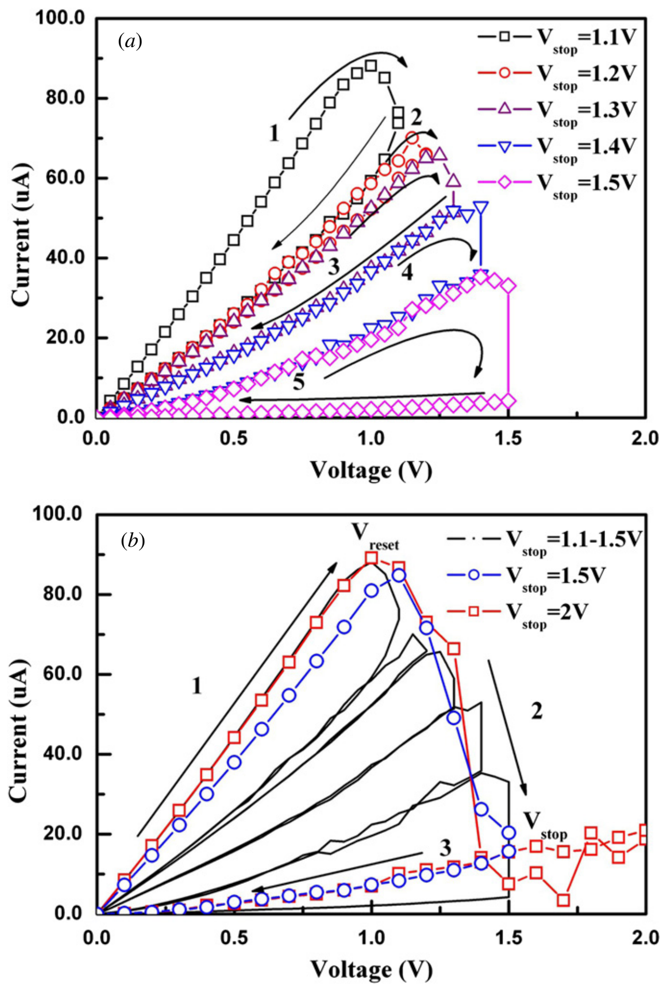


Figure 5. (*a*) Multilevel reset switching behaviors by controlling the V_{stop} ranging from 1.1 to 1.5 V. (*b*) Reset process behavior with the sweeping V_{stop} up to 2 V.

is applied to the new state, resulting in the resistance of the device being changed to another value between the new state and HRS. Therefore, the device can be switched to several resistance states by controlling V_{stop}. When V_{stop} exceeds to 1.5 V, the device switches back to the HRS, which keeps stable even when V_{stop} up to 2 V, as shown in figure 5(*b*). Such a tendency is analogous to the results reported by Wang *et al* [7] and Chae *et al* [17]. The presence of the multilevel LRS can be explained as the partial rupture of conducting filaments during the reset process. Based on conducting filaments theory, these conducting filaments consisting of oxygen vacancies are formed by current flowing across the ZrO_2 film during the set process as a result of soft breakdown [26, 34], where the strength and number of the conducting filaments are proportional to the I_{set}, so that I_{set} is comparable to I_{reset}. In the present case, the more the number of and the stronger the conducting filaments with larger size formed by higher I_{set}, the higher the V_{reset} is required to provide more movable oxygen ions from the interfacial layer between the ZrO_2 thin film and Ti top electrode to reoxidize the residual conducting filaments. As the negative sweeping voltage increases, more oxygen ions are repelled from the interfacial layer back to the ZrO_2 thin film, and react with the oxygen vacancies near the interface. Therefore, more conducting filaments are reoxidized and the resistance of the device increases until the voltage reaches to the maximum stop voltage and the resistance state is switched back to HRS again. However, the multibit storage by the controlling reset voltage method is not suitable for realizing practical application because the stop voltage cannot be precisely controlled to switch the RRAM back to the designated resistance state. Figure 6(*a*) indicates the dynamic resistive switching operation characteristics of the ZrO_2-based 1T1R memory cell. During the set process, a 250 ns pulse width with 2.5 V pulse amplitude is applied on the drain pad. Meanwhile, a small positive voltage bias is applied on the gate and the source is grounded to ensure the MOSFET keeping at the saturation situation to provide the suitable operation current. The device is then switched from HRS to LRS. For the reset process, the source is applied with a 250 ns pulse width with 2.5 V pulse amplitude. Meanwhile, the gate is biased at 2 V, with the drain grounded to ensure the MOSFET providing sufficient drive current for the device switched back to HRS. The results show that the devices could be switched under high-speed operation (250 ns) and low operation voltage. It is clear that the effective resistive switching region locates near the Ti/ZrO_2 interface and the small reactive region results in high-speed operation. Furthermore, the higher the conductivity achieved in the bulk oxide layer, the larger the voltage drop applied on the interface, leading to the lower required operating voltage. Moreover, the relationships between the pulse width and pulse amplitude for the set and reset processes were also investigated and the statistical charts are shown in figures 6(*b*) and (*c*). It is clearly shown that an increase of pulse amplitude (set/reset voltage) is required to successfully trigger the set/reset switching as a decrease of pulse width. For a fixed pulse width measurement (1000 ns), the current–voltage relation shows that the HRS current decreases as an increase of reset voltage (figure 6(*d*)); the multibit operation can be achieved by controlling the reset voltage. As indicated in the above results, the 1T1R memory cell with reproducible high speed and low switching operation voltage characteristics can be obtained for potential practical applications.

3.2. Temperature instability and retention properties

The *I–V* characteristics of the devices in LRS with 20 μA set current, and HRS at the various temperatures ranging from 25 to 150 °C, are shown in figure 7(*a*). The electrical characteristic of HRS exhibits a semiconductor-like behavior, where the current increases with an increase in temperature. The semiconductor-like Ohmic conduction is expressed as [35]

$$J \sim V \exp\left(\frac{-C}{T}\right) \qquad (1)$$

where T is the absolute temperature and C is a constant. Besides, the current in LRS also increases slightly with an increase in temperature, which also shows a semiconductor-like behavior, not a metallic conduction (electronic conduction) behavior. The ionic conduction is expressed as [35]

$$J \sim \frac{V}{T} \exp\left(-\frac{d}{T}\right) \qquad (2)$$

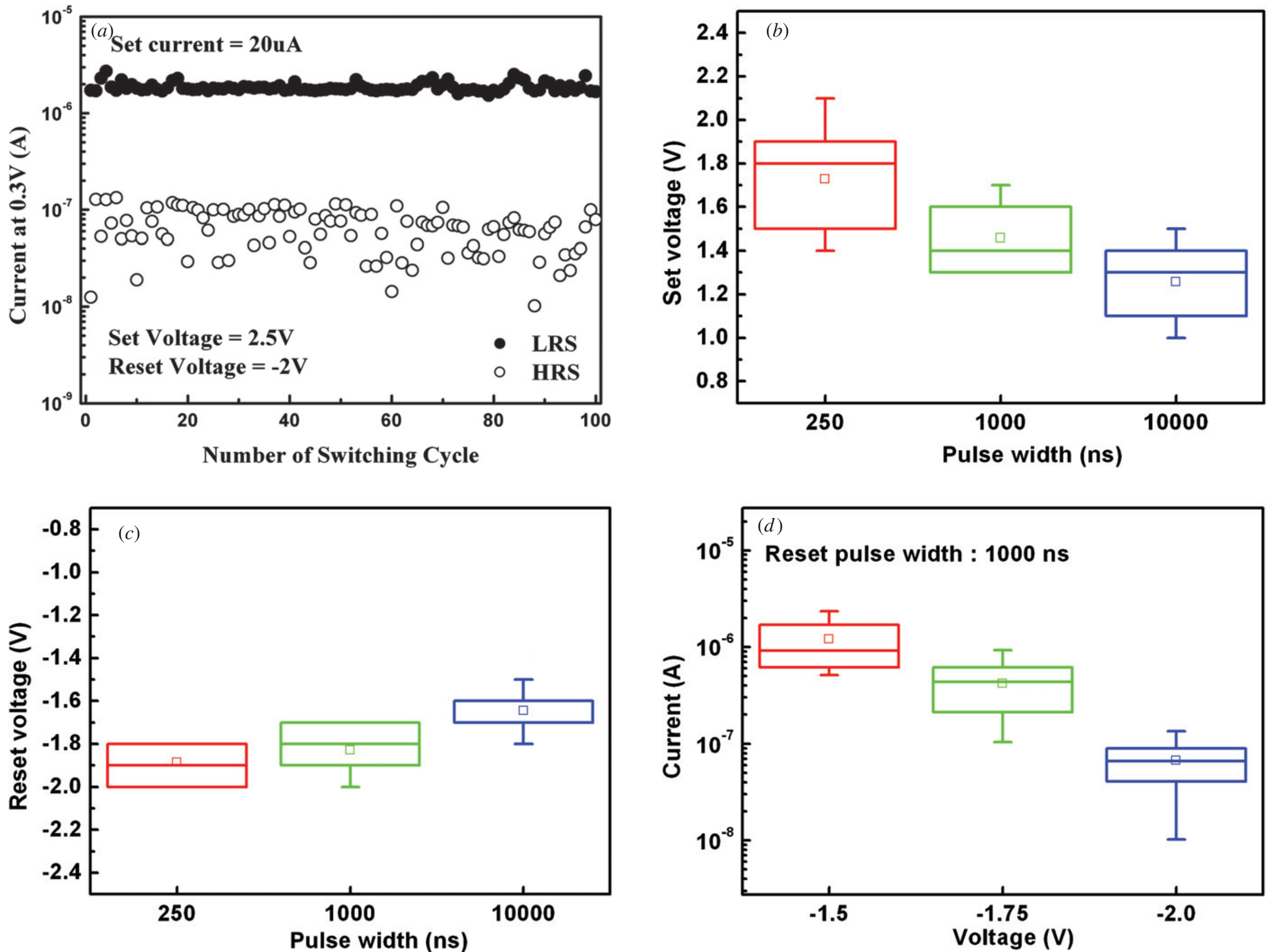


Figure 6. (*a*) Endurance test of device with the 250 ns pulse–width voltage. The relationship between the pulse width and pulse amplitude (*b*) for the set and (*c*) for the reset processes. (*d*) HRS current dependence of the pulse amplitude.

where d is a constant. A phenomenon is proposed whereby the biased electron hopping through the conducting filament consisting of oxygen vacancies would be responsible for the LRS conduction mechanism, in which the conduction electrons obtain the energy to jump out of the traps to the next one [3]. As mentioned in the above section, the 1T1R memory cells can display the multibit operation through modulating the set current to switch the devices to different LRS during the set process. However, the instability issue of each LRS may be the main obstacle for realizing the practical multibit storage applications. The temperature dependence of resistances in four LRS with respective set current of 20, 40, 115, 280 μA from 25 to 150 °C is shown in figure 7(*b*). The current in each LRS keeps relatively stable. It shows a sufficient memory window at the test temperature range, indicating that the memory devices with multibit storage behavior have stable operation in a wide temperature range. The thermal accelerating test under temperatures ranging from 150 to 200 °C was executed to confirm the retention reliability of each LRS. Cagli *et al* [36] indicated that the RRAM devices show a more stable retention behavior with an increase in conducting filament size. As mentioned above, it is conceivable that the conducting filaments formed in LRS under 20 μA set current would be weak and unstable. Therefore, we pay attention to the retention characteristics of the LRS with 20 μA set current at high temperature. In the retention test, the current of LRS falling below 0.5 μA with 0.1 V read voltage is defined as retention failure time. It is noteworthy that the 0.1 V read voltage for the reading operation is small enough to ignore the influence of the voltage stress on the retention test. The result indicates that the retention failure time decreases with an increase of temperature, where the mean retention failure times at 150, 175 and 200 °C are 26 400, 11 000 and 470 s, respectively. Such behavior can be attributed to accelerated oxygen ion diffusion caused by thermal stress. An oxygen ion must overcome the potential energy barrier for its diffusion. Therefore, for a specific diffusion barrier height, the oxygen ion has higher probability to pass the energy barrier at higher ambient temperature [37]. In fact, retention failure times in the thermal accelerating test present detectable fluctuations owing to the random paths and shapes of the conducting filaments. Therefore, the mean retention failure time, which is an average value of ten measured results at each test temperature, is adopted to present the results. Figure 8 depicts the relationship between mean retention failure time and reciprocal test temperature, which presents the data

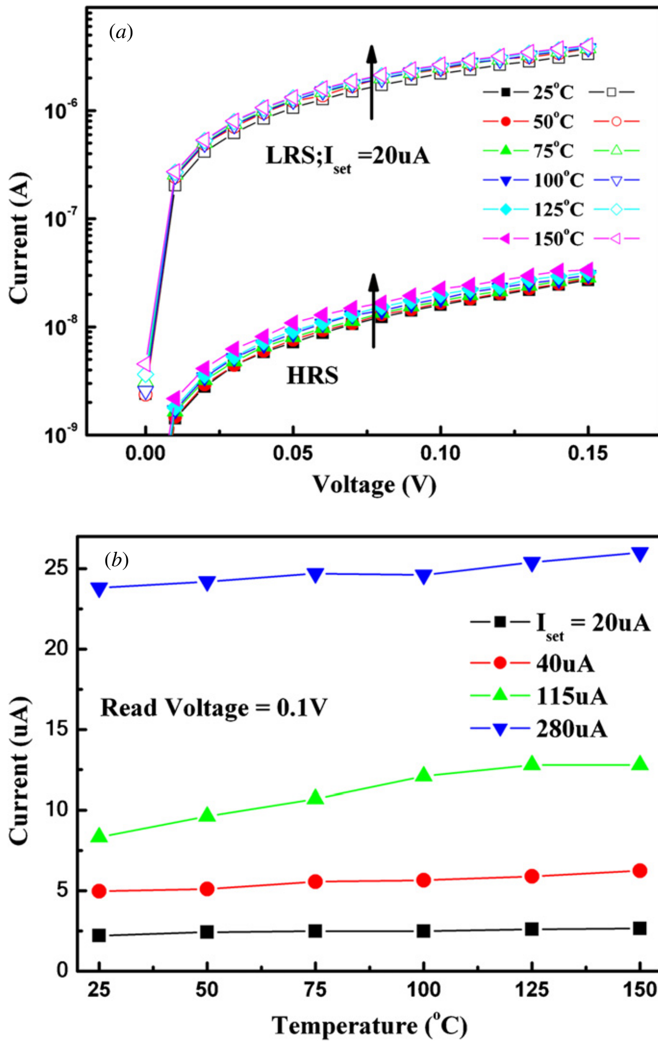


Figure 7. (*a*) Temperature dependence of currents in HRS and LRS with 20 μA set current. (*b*) Temperature dependence of the current of LRS at a different set current.

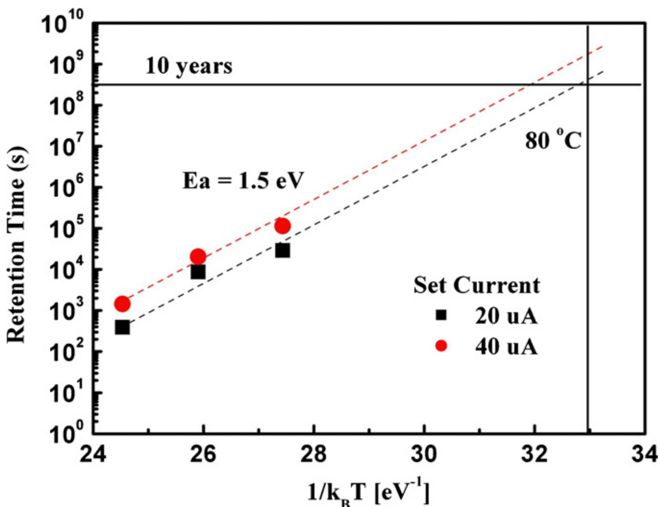


Figure 8. Arrhenius plot and extrapolation for the data retention time.

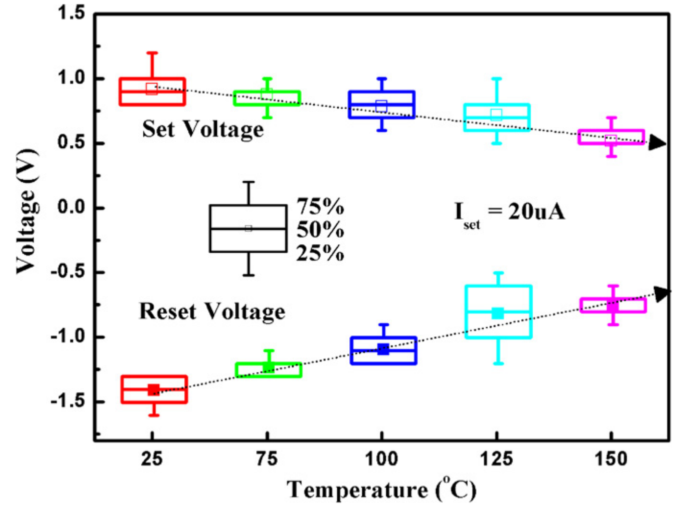


Figure 9. Plot of relationship between temperature and operation voltage.

retention ability in LRS of our devices with 20 μA set current through the Arrhenius equation. This equation is expressed as [8, 9, 31]

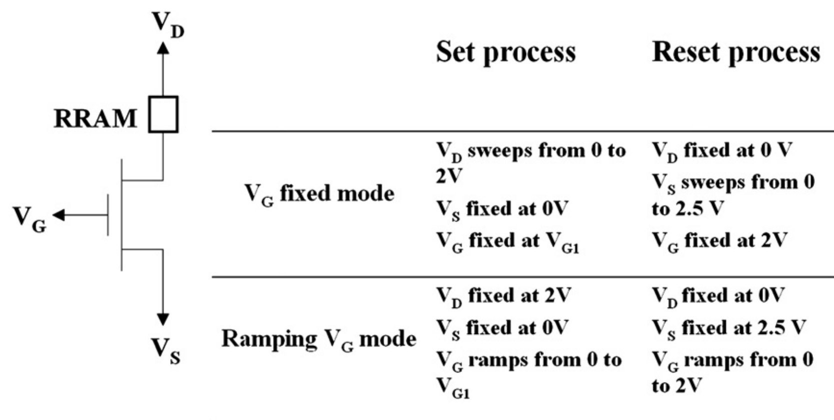
$$t_f \sim \exp\left(\frac{E_a}{k_B T}\right) \tag{3}$$

where t_f is the retention failure time, E_a is the activation energy for the oxygen ion diffusion and the reoxidation process, k_B is the Boltzmann constant and T is the ambient temperature. The E_a estimated from the slope of the dash line fitting in figure 8 is about 1.5 eV. Moreover, it is also shown in figure 8 that the retention lifetime for 80 °C is about 10 years by an extrapolation result of the Arrhenius equation. The thermal accelerating test for the LRS with 40 μA set current was also performed; the result shows that it has a longer retention failure time than LRS with 20 μA set current. Therefore, such results imply that the strength of conducting filaments controlled by the I_{set} is a key factor affecting the retention property. Furthermore, the change in operation parameters with changing temperature was also studied to provide further understanding of the reliability of the RRAM device. Figure 9 depicts the relationship between the set/reset voltage and test temperatures ranging from 25 to 150 °C, where the data at each temperature are collected from 25 DC sweeping cycles. It can be found that the absolute values of set and reset voltages decrease with an increase in temperature. It is proposed that both, the probability of the oxygen vacancy formation and the diffusion ability of the oxygen ions, increase with an increase of temperature, leading to reduced absolute values of set and reset voltages for formation and rupture of the conducting filaments.

3.3. Ramp gate voltage operation method

Multilevel storage properties of the devices have been demonstrated by modulating the set current. However, the resistance in LRS with smaller set current is larger than those in another LRS with larger set current and closer to the resistance in HRS, which may cause unacceptable HRS/LRS resistance

Table 1. Illustration of different operation modes for ZrO_2-based 1T1R RRAM.



	Set process	Reset process
V_G fixed mode	V_D sweeps from 0 to 2V V_S fixed at 0V V_G fixed at V_{G1}	V_D fixed at 0 V V_S sweeps from 0 to 2.5 V V_G fixed at 2V
Ramping V_G mode	V_D fixed at 2V V_S fixed at 0V V_G ramps from 0 to V_{G1}	V_D fixed at 0V V_S fixed at 2.5 V V_G ramps from 0 to 2V

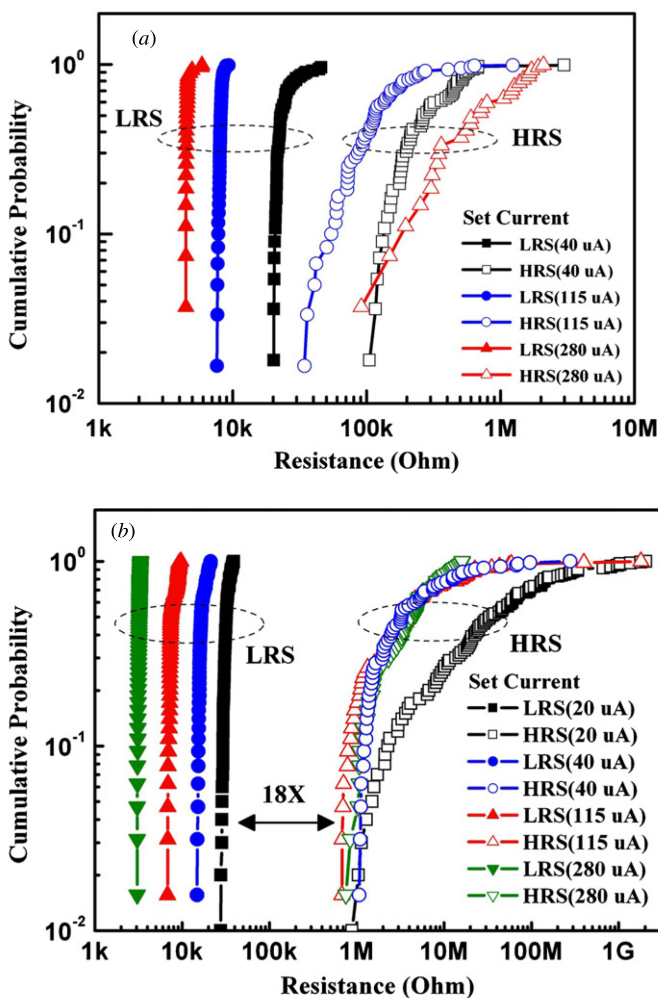


Figure 10. Resistance distributions in LRS and HRS with (*a*) fixed V_G operation mode and (*b*) with ramping V_G operation mode.

ratio and higher error-operation probability. As mentioned above, the increased number and stronger conducting filaments with larger size are formed by higher I_{set}, leading to the increased number of tiny residual conducting filaments in the ZrO_2 thin film after reset process and smaller resistance in HRS. Figure 10 depicts the cumulative probability plots of LRS and HRS resistances for the multilevel operation implemented in the devices, indicating relatively narrower distributions in R_{LRS} than in R_{HRS}. It is also indicated in figure 10(*a*) that the LRS with 40 μA set current overlaps with HRS with 115 μA set current, and may yield wrong information. Therefore, an alternative operation methodology for the 1T1R memory cell is performed, which switches the devices by adjusting the set current by ramping V_G with a fixed set voltage cross RRAM during the set process, based on the work of Chen [38]. Figure 10(*b*) indicates that the ramping V_G mode upgrades the memory performances including narrower LRS resistance distribution and higher HRS resistance, resulting in an acceptable HRS/LRS (20 μA set current) resistance ratio of about 18 times. The traditional operation method cannot control the accurate set voltage, resulting in wider LRS resistance distribution. In contrast, this ramping V_G mode applies the fixed set voltage cross RRAM and gradually increases the set current to the setting value. It contributes narrower LRS resistance distribution owing to a fixed set voltage and set current, where the power for the set process can be centered in a specific value, and furthermore, elevates the resistance ratio between HRS and each LRS. On the other hand, the ramping V_G mode applies appropriate voltage ($V_{stop,MAX}$) across RRAM and increases the gate voltage to supply the reset current during the reset process. The higher resistance in HRS can be achieved by using such a method. It was reported that the interface layer between Ti and ZrO_2 serves as an effective oxygen reservoir [23]. In this work, the appropriate fixed negative voltage ($V_{stop,MAX}$) applied on the Ti top electrode causes a certain amount of oxygen ions repelled from the interface layer to the bulk, and consequently, a reoxidation reaction occurs at the interface of Ti/ZrO_2 to rupture the conducting filament. The higher resistance in HRS is achieved due to the $V_{stop,MAX}$ applied. Table 1 lists the above-mentioned two methods and illustrates their influences on the performances of RRAM. Multilevel resistance switching performance can be enhanced by appropriately designing the operation method to minimize the distribution of resistances in LRS levels and contribute higher HRS resistance.

4. Conclusions

The bipolar resistive switching of Ti/ZrO_2/Pt nonvolatile memory with 1T1R architecture is successfully performed. The devices can be modulated to multilevel resistance state by controlling both the set current during the set process and the reset voltage during the reset process. Based on the fitting *I–V* curve and the relationship between the cell size and the resistances in LRS and HRS, the formation/rupture conducting filament model is proposed to be responsible for the resistive switching mechanism of our devices. The devices have high switching speed (250 ns), low operation voltage ($V_{set} = 2.5$ V; $V_{reset} = -2$ V) and acceptable HRS/LRS resistance ratio (>10). The currents in HRS and LRS only slightly increase as the temperature increases from 25 to 150 °C to obtain a stable resistance ratio between memory states. It is also found that the set and reset voltages for 20 μA operation current decrease from 0.9 and −1.4 V to 0.5 and −0.8 V, with ambient temperature change from 25 to 150 °C, respectively. Moreover, the data retention lifetime for LRS with 20 μA set current at 80 °C is more than 10 years, demonstrated by an extrapolation result of the Arrhenius equation. In addition, the narrower LRS resistance distribution and higher HRS resistance can be achieved by using the ramp-V_G method to switch the 1T1R memory cells, resulting in higher resistance ratio between LRS and HRS, appropriate for multibit storage applications. Our Ti/ZrO_2/Pt 1T1R memory devices with excellent performances show high potential for future nonvolatile memory applications.

Acknowledgments

This work was supported by the Winbond Electrics Corporation and by the National Science Council, Taiwan, under project NSC-99-2221-E-009-166-MY3.

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