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COMMUNICATION

Single-crystalline Ge nanowires and Cu_3Ge/Ge nano-heterostructures

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Single-crystalline germanium nanowires were synthesized *via* vapor–liquid–solid mechanism. The characteristics of the Ge nanowires were investigated by a transmission electron microscope to identify the [111] growth direction. The Ge nanowire-based field-effect-transistors on Si_3N_4 dielectrics were fabricated, showing a p-type semiconducting behavior with hole mobility of 47.03 $cm^2\ V^{-1}\ s^{-1}$. The formation of Cu_3Ge/Ge/Cu_3Ge nanoheterostructures was demonstrated with the reaction between copper contacts and Ge nanowires by rapid thermal annealing. The diameter-dependent electrical transport property of Ge nanowires indicates that with diameters of more than 80 nm, the resistivity of Ge nanowires decreased with diameter decrease, while with diameters of less than 80 nm, it increased. With multiple annealing processes, the channel length of the Ge nanowire transistors can be successfully controlled. From electrical measurements of each annealing step, the electrical transport property was significantly improved by sequential formation of Cu_3Ge contacts. The gradual formation of the germanide structure reduces Fermi level pinning effect and increases the Ohmic behavior of electrical transportation.

Introduction

With the pursuit of miniaturization of electronic components, one-dimensional semiconductor nanomaterials have attracted great interest due to their surface effect and surface-to-volume ratio in field effect transistors (FET),[1–3] solar cells[4,5] spintronics[6,7] and sensors[8] in recent years. Transition metal semiconductor nanowires are an extremely broad set of refractory materials, and were widely researched for their unique physical properties, low resistivity and excellent compatibility with contemporary silicon device processing.[9–17] For the device performance and incorporation in the current Complementary Metal–Oxide-Semiconductor (CMOS) technologies, germanium (Ge) nanowires, one of the group IV materials, appear to be favorable because of the quantum confinement effect and high carrier mobility.[17] Nowadays, the introduction of Ge in metal-oxide-semiconductor FET was based on carrier mobility improvement for better device performance.[18] However, metal–germanium interfaces often lead to the Schottky behavior of electrical transportation due to Fermi level pinning effect.[19,20] Moreover, the high specific resistivity of the Ge nanowire between source and grain contacts also restricts the total output current because of the limited enhancement by doping of the nanowires to reduce serial resistance.[21]

In this work, we proposed and demonstrated a method using rapid thermal annealing (RTA) of the fabricated samples to form the Cu_3Ge source/drain contacts with low Schottky barrier height (0.4 eV). With controlled annealing processes, the total resistivity of copper germanide/Ge heterostructure nanowire transistors was decreased with enhanced current owing to increased copper germanide length.

Experimental methods

The Ge nanowires were synthesized on (111)Si substrates with 3 nm thick gold films as catalysts in a vacuum furnace. A mixture containing 200 mg Ge and 200 mg C powder in an alumina boat and the growth substrates were put in the upstream and downstream, respectively. At the fixed system pressure of 6 Torr, the alumina boat was heated to 940 °C while the substrate temperature was held at 550 °C for 90 min. The Ge vapor source was carried by the flowing gas of 40 sccm N_2 and 4 sccm H_2 and then deposited on the substrates to grow single-crystalline Ge nanowires *via* vapor–liquid–solid (VLS) process. After the growth process, the furnace was cooled to room temperature gradually.

To investigate the electrical properties, Ge nanowires were transferred on a Si substrate with a 300 nm thick Si_3N_4 film as a dielectric layer for back-gate-field-effect-transistors (back-gate-FET). E-beam lithography (EBL) was utilized to define the metal electrodes on the Ge nanowires. Then the sample was immersed in dilute hydrofluoric (HF) acid for 30 s to remove native oxide of the metal contact region, followed by the process of Cu deposition with e-beam evaporation system and lift-off. The samples were annealed by RTA in Ar atmosphere from 150 to 250 °C for the reaction between Cu and Ge nanowires to form the Cu_3Ge/Ge nanoheterostructures along the nanowires. A JEOL JSM-6700 field emission scanning electron microscope (FESEM) was used to study the morphology of the as-grown nanowires and germanide

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heterostructures. For identifying the crystal structure of Ge/germanide heterostructures, JOEL JEM-2100F high resolution transmission electron microscope (HRTEM) was performed. Fast Fourier transform (FFT) technique was utilized to obtain the diffraction patterns. The electrical transport property was measured by Agilent B1500A.

Results and discussion

Device structures and TEM analysis

Fig. 1(a) shows the SEM image of the as-grown samples. The Ge nanowires covered the sample surface uniformly and densely. A low magnification TEM image is shown in Fig. 1(b), revealing that the length and diameter are 5–10 μm and 100 nm, respectively. The HRTEM image in Fig. 1(c) and the inset depict the crystallinity and [111] growth direction of the Ge nanowire. Fig. 2(a) and (b) are the schematic illustrations of the fabrication of germanide/Ge/germanide heterostructures before and after RTA process, where Cu diffuses into the Ge nanowires. At the beginning of the process, from the SEM image in Fig. 2(c), the Ge nanowire was straight and uniform before RTA. The formation of germanide was observed at 150 °C RTA for 2 min with a clear interfacial contrast of copper germanide/Ge heterostructures formed. Fig. 2(d) is the SEM image after 150 °C RTA with clear interfaces. The arrows in the figure indicate the heterostructures. At the annealing temperature of 250 °C for 2 min (Fig. 2(e)), the germanide formation process became severe and the growth length of the copper germanide reached 1 μm at both sides. Since the channel length of Ge nanowire between metal pads was defined by EBL and the germanide growth length could be controlled, the channel length of germanide/Ge/germanide can be controlled down to sub-micrometer regime. Notably, the volume expansion and segregation of the copper germanide appeared at the increased annealing temperature. Additionally, the rapid growth of the copper germanide at higher annealing temperatures (>200 °C) would cause the break of nanowires because of the high volume expansion, leading to difficulty in controlling the Ge channel lengths down to sub-100 nm range.

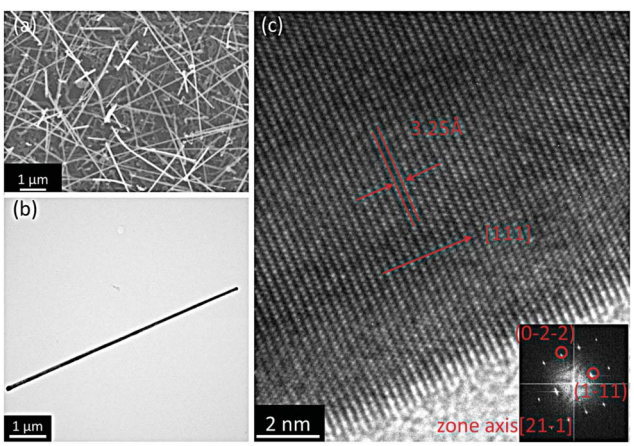

Fig. 1 (a) SEM image of as-grown Ge nanowires on (111)Si substrate. (b) Low magnification TEM image of a single Ge nanowire. (c) HRTEM image of the corresponding Ge nanowire in (b). The inset in (c) shows the corresponding FFT diffraction pattern.

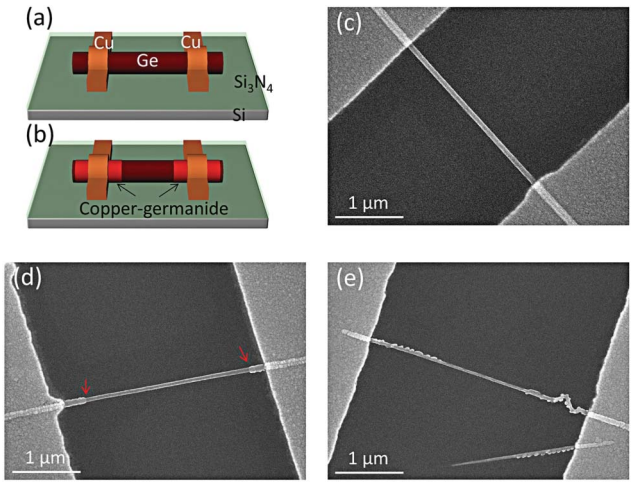

Fig. 2 Schematic illustrations of the formation of the germanide/Ge/germanide heterostructure (a) before and (b) after the RTA process. (c) SEM image of a Ge nanowire before RTA process. (d) SEM image of a germanide/Ge/germanide heterostructure after 150 °C RTA for 2 min. The arrows indicate the interface of the Ge/germanide heterostructure. (e) SEM image of the volume expansion and segregation of the Cu_3Ge at higher annealing temperature (>200 °C).

In order to identify the phase of formed copper germanide, the Ge nanowires were dispersed on TEM samples with a Si_3N_4 membrane window, followed by the back-gate-FET fabrication process as mentioned before to produce the device on the TEM samples. After 150 °C RTA for 10 min, the copper germanide/Ge heterostructures were formed near the Cu pad, as shown in Fig. 3(a). Fig. 3(b) and (c) show the HRTEM images of the germanium and germanide of the nanowire device highlighted by a red square in (a). From the analysis of the atomic planes and the FFT pattern, it shows that the Ge nanowire was grown along the <111> direction with a 0.326 nm plane interspacing (Fig. 3(b)). With calculation by the software (CaRIne Crystallography 3.1),

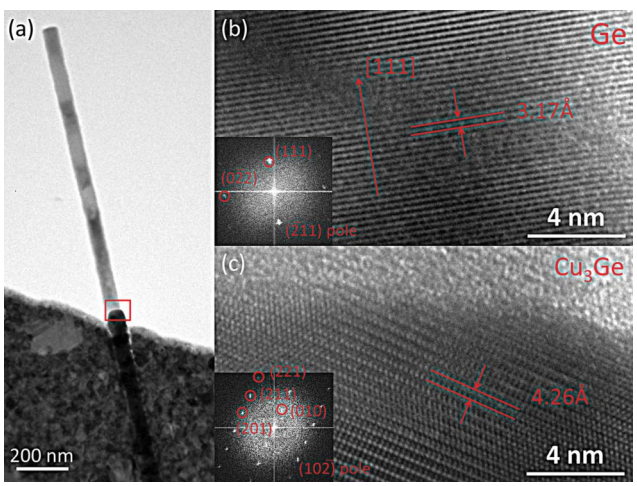

Fig. 3 TEM images of the germanium/germanide heterostructure after RTA process. (a) Low magnification TEM image of the Cu_3Ge/Ge heterostructure. The red square indicates the interface. (b) HRTEM image of the Ge nanowire. (c) HRTEM image of the as-formed orthorhombic Cu_3Ge. The FFT patterns in the insets of (b) and (c) denote the corresponding diffraction patterns.

the as-formed copper germanide was identified to be orthorhombic Cu_3Ge with lattice constants of a = 0.528 nm, b = 0.422 nm, and c = 0.454 nm (space group 59) (Fig. 3(c)). From the HRTEM images and FFT patterns of the Cu_3Ge/Ge heterostructure in Fig. 3, the crystallographic relationships between the Ge and Cu_3Ge are Ge[$\bar{2}$11] ‖ Cu_3Ge[$\bar{1}$02] and Ge(111) ‖ Cu_3Ge(221). The growth direction of Cu_3Ge is along the [221] direction.

FET devices

The electrical properties of the Ge nanowires and Cu_3Ge/Ge/Cu_3Ge nanowire heterostructures before and after the RTA process were investigated. As shown in Fig. 4(a), electrical measurements illustrated an enhanced current after RTA process. Fig. 4(b) revealed the drain source current–gate voltage (I_{ds}–V_g) curve of the as-fabricated Ge nanowire FET without annealing. The Ge nanowire FET shows a typical p-type behavior for the surface states induce hole accumulation.[22,23] The maximum current measured at V_{ds} = 0.5 V under −2 V gate bias is about 9.53 nA, corresponding to a current density of 2.62 × 10^2 A cm^{-2}.

For the Cu_3Ge/Ge/Cu_3Ge nanowire heterostructures after 150 °C RTA for 2 min, the maximum current measured at V_{ds} = 0.5 V is about 53.8 nA, corresponding to a current density of 1.48 × 10^3 A cm^{-2} (Fig. 4(c)).

Apparently, the electrical property has been greatly improved by almost one order of magnitude after the formation of Cu_3Ge/Ge/Cu_3Ge nanoheterostructures. According to the previous studies by Burchhart *et al.*, the small energy barrier (∼ 0.06 eV) between Cu3Ge and Ge would cause an ohmic behavior of heterostructured nanowires.[24] From Fig. 4(d), the I_{ds}–V_{ds} curve also shows a linear behavior after annealing, revealing that a good ohmic contact between the Cu_3Ge and Ge interface exists. From the electrical characteristics, the hole mobility can be extracted from the I_{ds}–V_g curves by using the transconductance (g_m) at a fixed drain bias V_{ds}:

$$\mu = \frac{g_m L^2}{V_{ds} C_{nitride}}$$

where L is the length of the Ge channel and $C_{nitride}$ is the back-gate capacitance, which can be estimated by using the cylinder-on plate model:[25]

$$C_{nitride} = \frac{2\pi\varepsilon_0\varepsilon_{nitride}L}{\cosh^{-1}(r + t_{nitride}/r)}$$

where ε_0 = 8.85 × 10^{-14} F cm^{-1} is the vacuum dielectric constant, $\varepsilon_{nitride}$ is the dielectric constant of Si_3N_4, r is the radius of the Ge nanowire, and $t_{nitride}$ is the thickness of the Si_3N_4 film. Based on the calculation of the hole mobility, the maximum transconductance (g_m) is extracted and the value is 47.03 cm^2 $V^{-1}s^{-1}$, which is lower than what was previously reported.[26] However, the model of the capacitance calculation was coherent with the structure of nanowires in the dielectrics. In our study, the nanowires were on the top of the dielectric layer. Thus, the actual value of capacitance would be smaller than the calculated one. As a result, the mobility would be underestimated.[27]

III V measurements of Ge nanowires

Since the formation of Cu_3Ge heterostructures after annealing demonstrated better performance of Ge nanowire transistors than metal contacts, the effect of germanide on transistors with different scales could be essential. For the study of the resistivity in different diameters, the devices were annealed at 150 °C for 4 min. The SEM images were utilized to identify the reaction to ensure the formation of Cu_3Ge and the lengths of Ge nanowires, and then the resistivity of each Ge nanowire would be estimated. Fig. 5(a) shows the plot of the resistivity as a function of diameter of Ge nanowires ranging from 40 nm to 160 nm. The value of the resistivity tends to increase with an increase in diameter. This result is contrary to most models of carrier transport in nanowires, where the decreased diameter induces the surface scattering of carrier in nanowires. However, it has been illustrated that the conductivity of nanowires is concerned about the carrier accumulation on the surface of the nanowire.[24] Due to the presence of surface states between the gate oxide layer and Ge nanowires,[23] the electron would be captured by surface states when transported in the channel, causing the surface hole accumulation and surface transport effect. It means that the concentration of surface charges would be proportional to the diameter of the nanowire and determine the conductivity of the nanowire, according to the equation:[28]

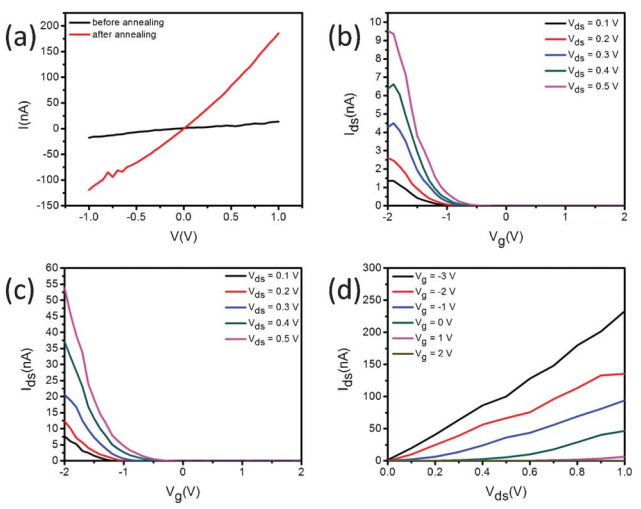

Fig. 4 Electrical measurements of the Ge nanowire transistor. (a) Current–voltage curves measured before and after RTA treatment. (b) I_{ds}–V_g curve of the Ge nanowire transistor before RTA treatment. (c) I_{ds}–V_g curve of the Ge nanowire transistor after RTA treatment. (d) I_{ds}–V_{ds} curve of the Ge nanowire transistor after RTA treatment.

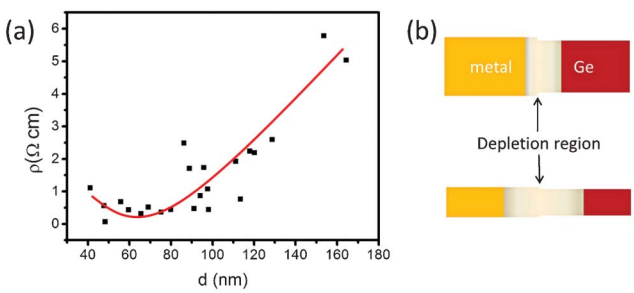

Fig. 5 (a) Plot of the resistivity of Cu_3Ge/Ge/Cu_3Ge as a function of the diameter of Ge nanowires. (b) Schematic illustrations of the increase of the depletion width with the decrease of the nanowire diameter due to the balance of carrier concentrations.

$$\sigma = \left(n_0 + \frac{4n_s}{d}\right) q\mu_h$$

where n_0, n_s, d, μ_h is the intrinsic carrier concentration, induced concentration of holes on the surface of the nanowire, diameter of the nanowire and hole mobility, respectively. As the diameter of Ge nanowire decreased, the portion of surface traps of electrons and induced hole accumulation would be increased. Thus, the conductivity of Ge nanowires would increase (or resistivity decrease) with a decrease in diameter.

Furthermore, it has been demonstrated that a depletion region would form between metal contacts and the Ge nanowire surface due to Fermi level pinning. Also, electron–hole recombination in the depletion region dominated the total current.[29] Similarly, it shows the small bias conductance density of metal/Ge nanowire interfaces increased because the depletion width increased with decreasing diameter, as shown in Fig. 5(b). Although the energy barrier of Cu_3Ge contact between Ge nanowires is smaller compared with copper contact between Ge nanowires, leading to the Fermi level pinning reduced, the existence of the depletion region between Cu_3Ge and Ge nanowires would still decrease the resistivity with the decreasing diameter of Ge nanowires.

Moreover, by using the formation of the depletion region model, it could be explained that the resistivity of Ge nanowires reached a minimum value with the diameter decreased to less than 80 nm. This was caused by diffusion of carriers in the depletion region. In spite of the depletion region increasing with decreasing diameters of nanowires, for the carriers, diffusion on the surface and shift in nanowires of small dimension would be difficult. Therefore, the decrease in resistivity would be retarded and increased as the diameter reduced to less than 80 nm.

Multiple RTA of devices and *I*/*V* measurements

To explore the influence of the gradual growth of Cu_3Ge nanowires on electrical properties, the *I*/*V* measurements and SEM images of device structures were performed to identify the electrical behavior and growth length of Cu_3Ge nanowires by conducting repeated RTA processes. The Ge channel length shrank from 2.33 μm to 1.96 μm after five cycles of RTA, as shown in Fig. 6(a)–(e). *I*/*V* measurements were performed after each annealing treatment, illustrated in Fig. 6(f). It shows that the ohmic behavior presented after the Cu_3Ge/Ge heterojunction formed. The length of RTA for 1st, 2nd and 3rd treatments at 150 °C and 4th and 5th treatments at 170 °C were 2, 4, 10, 4 and 8 min, respectively. Confirmed with SEM images, the growth length of Cu_3Ge nanowires corresponding to annealing time could be expressed, as shown in Fig. 6(g). It seems that the growth length of Cu_3Ge nanowires for first three steps was not proportional to the annealing time until the 4th and 5th annealing at 170 °C. According to Fig. 6(f), the calculated resistivity of Cu_3Ge/Ge heterostructured nanowires of each annealing step as a function of the Ge channel length were plotted in Fig. 6(h). Obviously, the resistivity of the 2nd, 3rd, 4th and 5th annealing exhibited a linear relationship due to the shrinkage of the Ge channel length. However, the resistivity of 1st annealing at the channel length of 2.33 μm appeared four times larger than the estimated resistivity (the red line in Fig. 6(h)). Compared with Fig. 6(g), the growth length of Cu_3Ge nanowires at 1st annealing also shows four times larger than that at 2nd annealing. At the same annealing temperature, Cu_3Ge nanowires should have had the same growth rate. We speculate that the diffusion of Cu atoms was much faster on the Ge nanowire surface than at the inner region of Ge nanowires. As the result, copper germanide formed only partly on the surface of heterostructured nanowires. Owing to the incomplete formation of copper germanide, the charge carriers may be retarded at the injection interface of the heterostructures in the radial direction, reducing the electrical transportation.

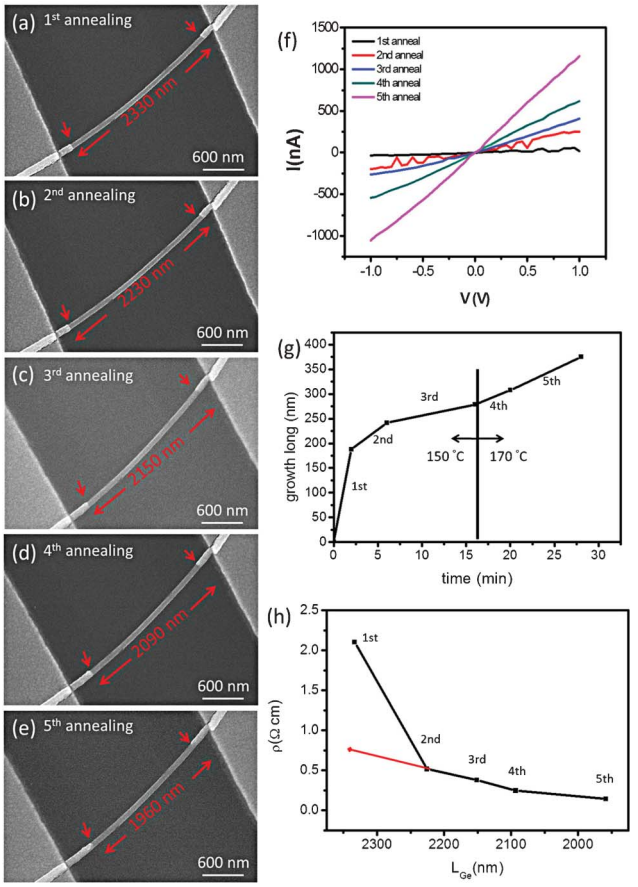

Fig. 6 Multiple RTA processes and electrical measurements of a single Ge nanowire. (a)–(e) SEM images of device structures after 1st, 2nd, 3rd, 4th and 5th RTA process, respectively. (f) Current–voltage curves after each RTA treatment. (g) Plot of growth lengths of Cu_3Ge as a function of annealing time. (h) Plot of resistivities of heterostructured nanowires as a function of the Ge channel length after each RTA treatment.

Conclusions

Single-crystalline Ge nanowires were synthesized *via* thermal evaporation and VLS growth method. The Ge nanowire FET was fabricated using EBL, metal deposition and the lift-off technique. Covered with copper contacts, the germanide/Ge/germanide heterostructured nanowires would be formed after the RTA process. Orthorhombic Cu_3Ge was identified by HRTEM and FFT diffraction patterns. The Ge nanowire FET devices demonstrated a p-type behavior for surface hole accumulation with hole mobility of 47.03 $cm^2\ V^{-1}\ s^{-1}$. The diameter-dependent electrical transport property of Ge nanowires shows that the resistivity of Ge nanowires decreased with decreasing diameter, retarded and even increased at diameters of less than 80 nm. The multiple annealing processes were utilized to control the Ge

channel length. The *I*/*V* measurements of each annealing show excellent enhancement of electrical transportation. Also, the gradual formation of germanide structures reduces Fermi level pinning effect and increases the Ohmic behavior of electrical transportation.

Acknowledgements

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