A Low Voltage All-Digital On-Chip Oscillator Using Relative Reference Modeling

Chien-Ying Yu, Jui-Yuan Yu, and Chen-Yi Lee, *Member, IEEE*

***Abstract*—This paper presents a low voltage on-chip oscillator which can compensate process, voltage, and temperature (PVT) variation in an all-digital manner. The relative reference modeling applies a pair of ring oscillators as relative references and estimates period of the internal ring oscillator. The period estimation is parameterized by a second-order polynomial. Accordingly, the oscillator compensates frequency variations in a frequency division fashion. A 1–20 MHz adjustable oscillator is implemented in a 90-nm CMOS technology with 0.04 mm^2 area. The fabricated chips are robust to variations of supply voltage from 0.9 to 1.1 V and temperature range from 0 °C to 75 °C. The low supply voltage and the small area make it suitable for low-cost and low-power systems.**

***Index Terms*—Digitally controlled oscillator (DCO), frequency compensation, low voltage, oscillators, process, voltage, and temperature (PVT) variations.**

I. Introduction

CLOCKING is an essential part in a digital system. The conventional clock source, a quartz crystal oscillator, is incompatible with the CMOS process. The incompatibility not only results in extra cost in the board-level integration but also wastes power on the peripheral capacitive elements when passing the oscillation signal. In applications such as microcontrollers [1] and wireless sensor nodes [2], the cost and power consumption of the overall system are the most concerned for mass distribution and long lifetime. The frequency accuracy can be loosed for the low-cost and low-power integration of the CMOS on-chip oscillators.

However, maintaining the frequency accuracy is still a challenging issue of the CMOS on-chip oscillator design due to the process, voltage, and temperature (PVT) variations. Taking a 21-stage ring oscillator in a 90-nm CMOS process as an example, the free-run frequency varies widely from a few hundred MHz to several GHz with PVT variations. Process variation is generally calibrated by trimming passive components like resistors and capacitors during post-fabrication test. Voltage and temperature variations are dealt with by separate approaches to maintain the frequency stability. Bandgap references in [3]–[6] are applied to mitigate voltage variation. Power averaging feedback in [7] cancels the voltage variation. Adaptive biasing scheme [3] is developed for a ring oscillator to maintain a constant frequency over process and temperature variations. A varactor array and feedback loops in [4] compensate temperature variation. Proportional to absolute temperature (PTAT) circuits [5] are designed to compensate temperature variation of the reference current and the electron mobility. The resistive elements in [6] and [7] are either chosen or sized for less temperature dependence. These techniques perform excellent capabilities to overcome PVT variations. However, these designs are customized with diagnostic structures and might be dedicated to specific techniques or properties (e.g., bipolar, MIM capacitor, low temperature dependent resistor, etc.). Some are not necessarily available in the fabrication process.

In addition, conventional bandgap references are inapplicable with sub-1 V supply [8]. The standard supply voltage for the core devices is scaled down to 1 V in deep-submicrometer processes. Circuits operating at low supply voltage have finite voltage headroom for biasing. The existing on-chip oscillators are, therefore, infeasible as the process and the voltage scale shrinks. On the other hand, fully digital implementation can operate at low supply voltage and is easy to be adopted in existing systems. Thus, this work proposes an all-digital solution for a low cost, low voltage on-chip oscillator while maintaining moderate frequency accuracy. The relative reference modeling uses a unified approach to estimate the present oscillation period of a ring oscillator regardless of the individual effects from PVT variations.

The implementation is carried out in a 90-nm CMOS process with the standard supply voltage of 1 V. Two additional contributions are further satisfied for various application requirements: 1) standard logic cell synthesizability, which can be directly combined into existing systems and design flows with negligibly extra effort; 2) frequency adjustability, which can be applied to dynamic frequency scaling applications for power reduction. The previous work [9] demonstrates a 40 MHz on-chip oscillator where the parallel comparison architecture occupies considerable area. This paper analyzes the frequency accuracy against PVT variations and improves the circuit architecture for area reduction. Section II shows the basic concept of the relative reference modeling. The system architecture and detailed circuits are shown in Section III. Section IV demonstrates the chip implementation and the experimental results. Finally, Section V concludes this work.

Manuscript received March 03, 2011; revised May 30, 2011; accepted June 10, 2011. Date of publication August 18, 2011; date of current version July 05, 2012. This work was supported in part by MOEA of Taiwan, under Grant 96-EC-17-A-03-S1-0005, and UMC University Shuttle Program, respectively.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: cyyu@si2lab.org; jyyu@si2lab.org; cylee@si2lab.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2011.2160301

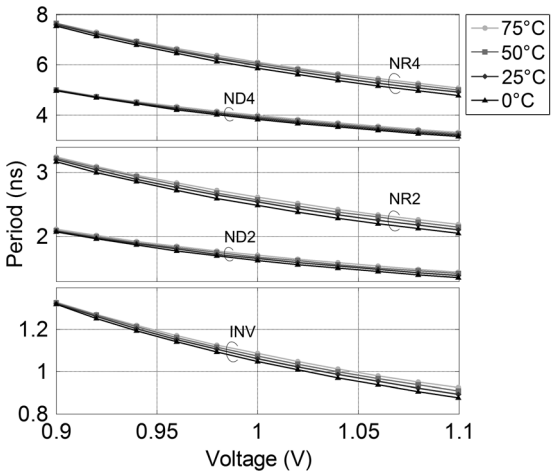

Fig. 1. Periods of the ring oscillators composed of different logic gates with voltage and temperature variations. INV: inverter gate, ND: NAND gate; NR: NOR gate; the number attached after the gate name indicates the number of inputs.

II. Relative Reference Modeling

The simplest implementation of a fully digital oscillator is the ring architecture composed of odd number of inverting delay cells (IDCs). The basic IDC is an inverter (INV) gate. Some common logic gates, like NAND, NOR gates, can also be configured as the IDCs by connecting inputs together. Fig. 1 shows the periods of ring oscillators composed of several types of the IDCs. The cell delays spread widely with voltage and temperature variations. Besides, the degrees of the delay variations differ according to the types of the IDCs. Based on the relative delay variations, the relative reference modeling estimates the absolute value of the gate delay. Denoting the IDC to be modeled as the reference delay cell (RDC) and the IDC to be compared as the compared delay cell (CDC), the delay ratio is expressed as

$$R(P,V,T) = \frac{D_{\mathrm{CDC}}(P,V,T)}{D_{\mathrm{RDC}}(P,V,T)} \tag{1}$$

where $D_{\mathrm{CDC}}(P,V,T)$ and $D_{\mathrm{RDC}}(P,V,T)$ are the delays of the CDC and the RDC, respectively. Symbols are expressed as functions of P, V, and T to describe the PVT effects where P represents the combined set of plural process parameters. The upper part of Fig. 2 shows the relation between the INV gate delay and the delay ratio of the NR2 gate to the INV gate derived from Fig. 1. The INV gate delay is highly correlated to the delay ratio. The delay of the RDC can then be modeled as

$$\begin{aligned}\widetilde{D}_{\mathrm{RDC}}(P,V,T) &= \mathrm{coef}_0 + \mathrm{coef}_1 R(P,V,T) \\ &\quad + \mathrm{coef}_2 R^2(P,V,T) + \cdots + \mathrm{coef}_n R^n(P,V,T)\end{aligned} \tag{2}$$

where coef_n is the nth-order modeling coefficient. An approximated second-order polynomial, $\tilde{D}_{\mathrm{INV}}$, is set to model the INV gate delay.

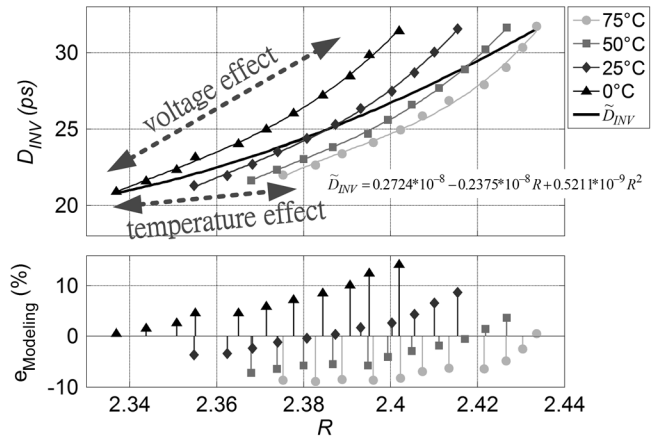

Fig. 2. Upper part shows the simulated points of the INV gate delay to the delay ratio with a second-order model; the lower part shows the modeling error.

In the upper part of Fig. 2, the displacements of the ratio-delay relation caused by voltage and temperature effects are not identical. The two effects span a region that does not coincide on the modeling curve. To evaluate the accuracy of the model, the modeling error is defined as

$$e_{\mathrm{modeling}}(P,V,T) = \frac{D_{\mathrm{RDC}}(P,V,T) - \widetilde{D}_{\mathrm{RDC}}(P,V,T)}{D_{\mathrm{RDC}}(P,V,T)}. \tag{3}$$

The $e_{\mathrm{modeling}}(P,V,T)$ of the $\tilde{D}_{\mathrm{INV}}$ is shown in the lower part of Fig. 2 where the absolute maximum value is 14.2%. The modeling accuracy depends on the type of the relative references and the operating range including the supply voltage and the temperature. Two principles should be satisfied for high modeling accuracy when selecting the relative reference pairs. First, large relative delay variations exist between the RDC and the CDC so that the absolute delay value can be reflected by the delay ratio. If the delay variations are similar, the delay ratio remains unchanged in different voltage and temperature conditions. Second, the displacements of the ratio-delay relation caused by voltage and temperature effects need to be identical. The delay is perfectly modeled if a displacement of the delay ratio, ΔR, caused from the voltage or the temperature effect always results in a displacement of the delay, ΔD_{RDC}, according to the modeling polynomial.

To get more insights about the selection of the relative references, the absolute maximum modeling errors of some common logic gates with 0.9 to 1.1 V supply voltage and 0 °C to 75 °C temperature range are listed in Table I. The model fits better with the relative references of the INV-NAND pairs and the INV-NOR pairs for the large relative delay variations. The NAND/NOR gates are more voltage and temperature sensitive than the INV gate due to the higher equivalent RC delay [10]. When the number of the gate inputs increases, the stacked transistors have higher threshold voltage due to the body effect and become more sensitive to the supply voltage. Therefore, the slope of the displacement caused by voltage effect gets close to that caused by temperature effect. The absolute maximum modeling errors decrease as the number of the gate inputs increases. For the relative references of the rest pairs, the above two principles are not

TABLE I
ABSOLUTE MAXIMUM MODELING ERROR MATRIX OF COMMON LOGIC GATES

		CDC						
		INV	ND2	ND3	ND4	NR2	NR3	NR4
RDC	INV		0.191	0.046	0.019	0.142	0.048	0.028
	ND2	0.191		0.093	0.117	0.151	0.079	0.103
	ND3	0.046	0.094		0.143	0.343	0.184	0.168
	ND4	0.019	0.117	0.143		0.269	0.351	0.371
	NR2	0.142	0.150	0.343	0.269		0.125	0.163
	NR3	0.048	0.079	0.184	0.350	0.125		0.241
	NR4	0.027	0.103	0.168	0.371	0.163	0.241	

ND: NAND gate; NR: NOR gate; the number attached after the gate name indicates the number of inputs.

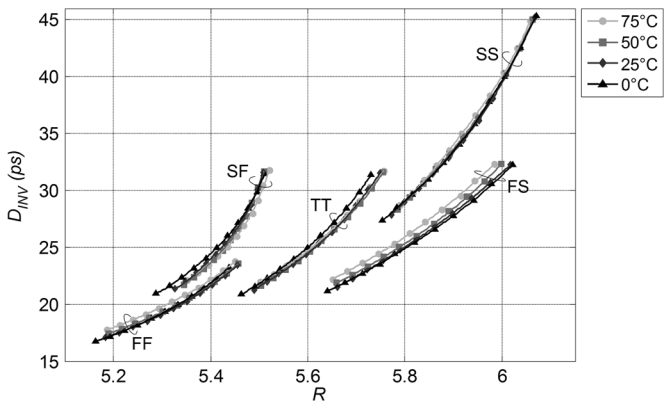

Fig. 3. Ratio-delay relation of the INV-NR4 pairs in five process corners. The first letter denotes the speed of the nMOS. The second letter denotes the speed of the pMOS.

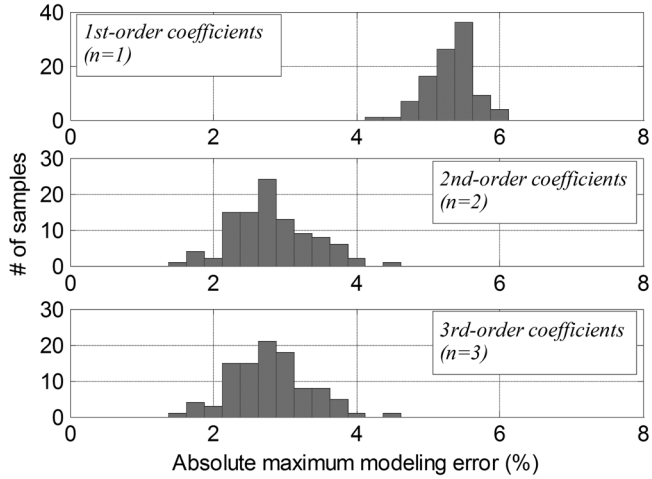

Fig. 4. Collections of the absolute maximum modeling errors with different modeling polynomial orders.

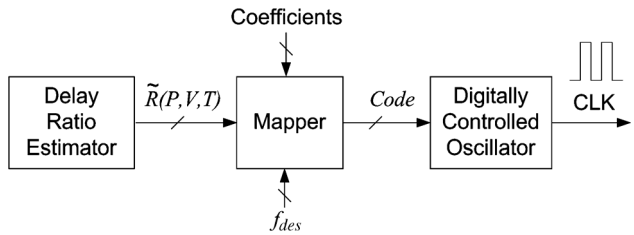

Fig. 5. System architecture of the on-chip oscillator.

well satisfied. The modeling accuracy is inferior and might not be adoptable in applications.

The modeling polynomial can be first-order, second-order, or even higher order depending on the required accuracy. The process variation of the design is implicitly contained in the modeling coefficients, which can be obtained in chip testing procedures. Fig. 3 shows the ratio-delay relations of the INV-NR4 pairs in five process corners. The coefficients alter as the process variations are taken into account, and the Monte Carlo simulation[1] shows the model is still representative. Fig. 4 shows the collections of 100 Monte Carlo simulations with model of different polynomial orders. The absolute maximum modeling errors are lower when applying higher polynomial orders. However, the improvement of the modeling errors with the polynomial order is limited on the order higher than third. It comes to the suggestion that second or third order polynomial is enough for the delay model.

III. SYSTEM ARCHITECTURE

A system architecture based on the relative reference modeling is proposed as shown in Fig. 5. The delay ratio estimator first estimates the delay ratio of the relative references, $\tilde{R}(P,V,T)$. With the estimated delay ratio and the coefficients, the mapper is able to obtain the delay information in the present PVT condition. The control code is then calculated for a digitally controlled oscillator (DCO) to generate the compensated clock. One implementation has been carried out in [9] where the parallel-delay-line comparison in the delay ratio estimator occupies considerable area. In this section, we introduce the area-efficient circuit architecture with the period comparisons of two ring oscillators and the frequency compensation based on frequency division.

A. Delay Ratio Estimator

Since the period of a ring oscillator is proportional to the delay of the composite IDCs, the delay ratio of two types of gates can be estimated by the architecture of two ring oscillators shown in Fig. 6. The delay ratio can be estimated with extendable accuracy requirement by cycle counting. Denoting the ring oscillator with the RDC as RRO and the other with the CDC as CRO, the RRO and the CRO generate oscillation signals which are directly connected to two counters. The estimated delay ratio will be demonstrated as the fractional value

$$\widetilde{R}(P,V,T) = \frac{N_{\mathrm{RRO}}}{N_{\mathrm{CRO}}} \tag{4}$$

where N_{CRO} and N_{RRO} are the counted numbers of the CRO and the RRO, respectively. If the counting time is enlarged, the values of N_{CRO} and N_{RRO} will be bigger and result in a finer estimation resolution. Setting the counting time as N_{TIME} cycles of the oscillation period of the CRO, the estimation error to the actual period ratio, $R(P,V,T)$, is guaranteed to be less than $1/N_{\mathrm{TIME}}$. Setting N_{TIME} to the value of power of two,

[1]The UMC 90-nm LOGIC/MIXED_MODE Monte Carlo Mismatch Spice Model is applied with 3 sigma distributions in the process simulations.

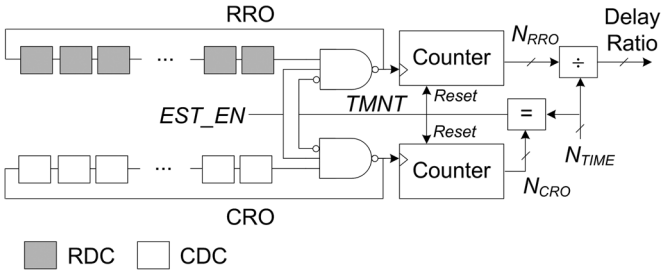

Fig. 6. Circuit of the delay ratio estimator.

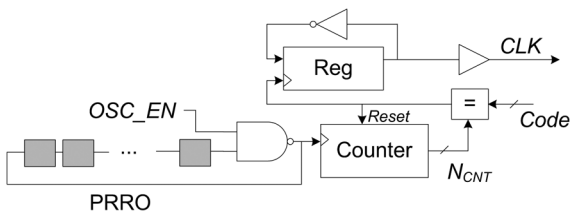

Fig. 7. Circuit of the DCO.

the division by N_{TIME} needs no divider. Comparing to the parallel-delay-line comparison approach [9], the cycle counting approach reduces most of the area which also relieves the effects from the on-die variations.

B. Mapper

Code for the DCO can be calculated in the mapper once the delay ratio is estimated. The second-ordered estimated period of the PRRO is

$$\hat{T}_{\mathrm{PRRO}}(P,V,T) = c_0 + c_1\widetilde{R}(P,V,T) + c_2\widetilde{R}^2(P,V,T) \quad (5)$$

where c_j is the jth order coefficients. The control code is derived for a desired frequency, f_{des}, as

$$\mathrm{Code} = \mathrm{round}\left(\frac{1}{2\cdot f_{\mathrm{des}}\cdot\left[c_0+c_1\widetilde{R}(P,V,T)+c_2\widetilde{R}^2(P,V,T)\right]}\right). \quad (6)$$

It is rounded to the nearest integer due to the finite resolution of the DCO.

C. Digitally Controlled Oscillator

Fig. 7 shows the DCO architecture. The output frequency is an integer fraction of the frequency generated by a pre-output RRO (PRRO). The control code, Code, is compared with the cycle counter. The value of the output register is inverted in every trigger from the comparator output. Therefore, the duty cycle of the output clock is guaranteed to be 50%, and the corresponding frequency is generated as

$$f_{\mathrm{DCO}} = \frac{\hat{f}_{\mathrm{PRRO}}(P,V,T)}{2\cdot \mathrm{Code}} \quad (7)$$

where $\hat{f}_{\mathrm{PRRO}}(P,V,T)$ is the frequency of the PRRO. The PRRO adopts the same IDCs as the RRO in the delay path and has the same timing performance as estimated to PVT variations. It also eliminates the possible inaccuracy from the path selector of the DCO in [9].

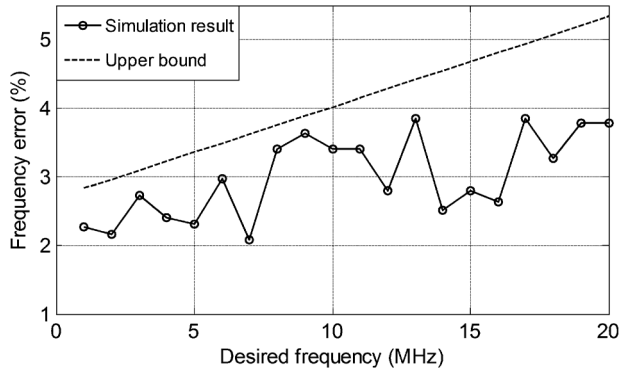

Fig. 8. Simulated output frequency error versus different desired output frequency.

IV. Implementation and Experimental Result

An all-digital on-chip oscillator is implemented in a 90-nm CMOS process based on the above circuit architecture. The INV gate and the NR4 gate are chosen to be the relative references. The supported frequency range with the DCO of 10-bit control code can be as low as 1 MHz. The frequency error versus the desired frequency is shown in Fig. 8. The frequency error is defined as the absolute maximum difference between the output frequency and the desired value over the supply voltage from 0.9 to 1.1 V and the temperature range from 0 °C to 75 °C. The frequency error is presented randomly because of the quantization effect in the implementation. A theoretical upper bound for the frequency error can be derived from the absolute maximum modeling error, the worst quantization error, and the worst DCO resolution in the operating range, as

$$\begin{aligned}\mathrm{UpperBound} &= \mathrm{Max}(e_{\mathrm{Modeling}}) + \mathrm{Max}(\mathrm{quantization\_error}) \\ &\quad + \mathrm{Max}(\mathrm{DCO\_resolution}) \\ &= 2.7\% + 0.1\% + \frac{1.32\ \mathrm{ns}}{T_{\mathrm{des}}}\end{aligned} \quad (8)$$

where the implemented quantization error is about 0.1% and T_{des} represented for the desired output period.

The frequency error is about two to three percent at lower desired frequency. The DCO output frequency resolution might introduce considerable frequency error at higher desired frequency. Therefore, the high desired frequency should be constrained for different application requirements. The simulation result confirms the frequency error is generally larger at higher desired frequency and never exceeds the upper bound. In practice, the upper bound is seldom touched because the probability when the worst modeling error, quantization error, and the DCO resolution happen at the same instant is low.

Fig. 9 shows the die photo with the layout view. It is mounted in the Side Braze ceramic package. The active area is 305 μm $\times$ 130 μm including an extra testing part. The area is mainly occupied by the mapper, which handles most of the digital value calculations. The rest parts are regular structures as shown in

TABLE II
COMPARISONS OF ON-CHIP OSCILLATORS

Design	[3]	[4]	[5]	[6]	[7]	[9]	This work
Technology	0.25μm CMOS	0.13μm CMOS	0.5μm CMOS	0.18μm CMOS	0.18μm CMOS	90nm CMOS	90nm CMOS
Supply voltage (V)	2.4 - 2.75	1.8 - 3.3	3 - 5	1.2 - 3	1.7 - 1.9	0.9 - 1.1	0.9 - 1.1
Frequency (MHz)	7	6*	11.6	10	14	40	5*
Area (mm^2)	1.6	0.81	0.19	0.22	0.04	0.4	0.04
Power (mW)	1.5	3.6	0.4	0.08	0.04	0.24	0.65
Accuracy (%)	2.64	0.008	2.5	0.45	0.91	3.5	2.3

* Adjustable output frequency.

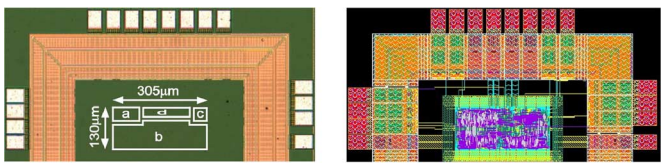

Fig. 9. Die photo of the on-chip oscillator and the layout view. The floorplan representations are: (a) delay ratio estimator, (b) mapper, (c) DCO, and (d) testing circuit.

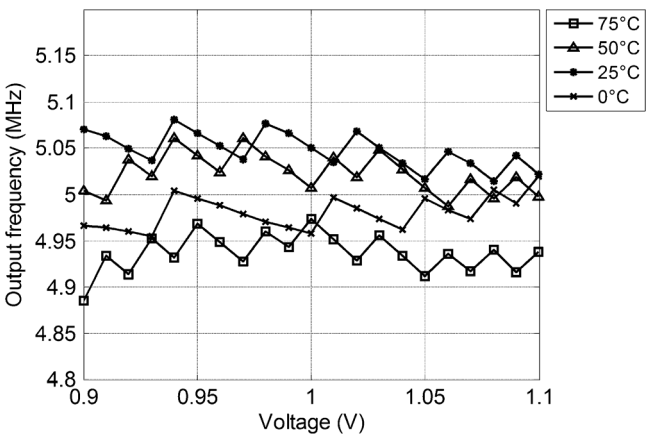

Fig. 10. Measured output frequency of the proposed oscillator when the desired frequency is set as 5 MHz.

the previous section and occupy only a little area. The modeling coefficients are first calculated by minimum mean square error fitting from the measurements of the R and the T_{PRRO} in the operating range of the supply voltage from 0.9 to 1.1 V and the temperature from 0 °C to 75 °C. Fig. 10 shows the measured output frequency for a single sample targeting on 5 MHz. The output frequency is compensated to 5 MHz with -2.3% and $+1.6\%$ variations. The start-up time of the output clock is 10.06 μs which includes the delay ratio estimation time, the combinational circuit delay in the mapper and the DCO delay. The rms jitter and current consumption measured at 5 MHz are 0.24 ns and 650 μA, respectively, at 1 V supply and 25 °C. A batch test of five chips is executed, and Fig. 11 shows the frequency error versus different output frequency which well corresponds to the simulation results in Fig. 8.

Comparing to the previous work [9], this work reduces the area by more than 10 times. The implementation of the period comparison can also improve the frequency accuracy with a longer calibration time due to the cycle counting. The frequency division based compensation occupies smaller area, and

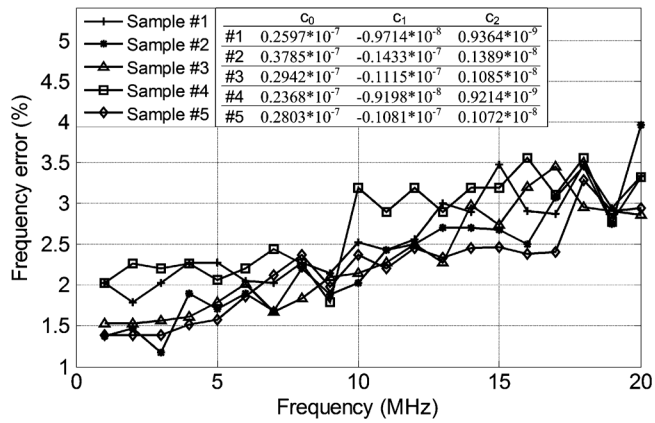

Fig. 11. Measured output frequency error of 5 samples at different output frequency.

the output matches the delay model without extra error in the delay path. As to the existing on-chip oscillators, the performance comparison is listed in Table II. In this work, the architecture with the relative reference modeling is the first all-digital approach to compensate the output frequency to PVT variations. The advantages of the lowest supply voltage and the smallest area are achieved with moderate frequency accuracy. The proposed on-chip oscillator can be directly integrated in the deep-submicrometer design with the standard supply voltage of 1 V. In addition, the utilization of the standard logic and the frequency adjustability make it more applicable to various system requirements.

V. CONCLUSION

A relative reference modeling method has been proposed to estimate the period of the internal ring oscillator affected by PVT variations. The architecture of the period comparison based delay ratio estimation and the frequency division based compensation is implemented in a 90-nm CMOS process. Targeting on 5 MHz, the measurement shows the maximum frequency error of 2.3%. The proposed on-chip oscillator works at lower supply voltage in standard CMOS process and can be fully integrated in existing systems for low-cost and low-power applications.

ACKNOWLEDGMENT

The authors would like to thank their colleagues within the SI2 Group, National Chiao Tung University, Taiwan, for many fruitful discussions in test chip design and implementation.

REFERENCES

[1] E. D. Marsman, R. M. Senger, M. S. McCorquodale, M. R. Guthaus, R. A. Ravindran, G. S. Dasika, S. A. Mahlke, and R. B. Brown, "A 16-bit low-power microcontroller with monolithic MEMS-LC clocking," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2005, pp. 624–627.

[2] M. Patel and J. Wang, "Applications, challenges, and prospective in emerging body area networking technologies," *IEEE Wirel. Commun.*, vol. 17, no. 1, pp. 80–88, Feb. 2010.

[3] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 433–442, Feb. 2006.

[4] M. S. McCorquodale, B. Gupta, W. E. Armstrong, R. Beaudouin, G. Carichner, P. Chaudhari, N. Fayyaz, N. Gaskin, J. Kuhn, D. Linebarger, E. Marsman, J. O'Day, S. Pernia, and D. Senderowicz, "A silicon die as a frequency source," in *Proc. IEEE Int. Freq. Control Symp.*, 2010, pp. 103–108.

[5] A. V. Boas and A. Olmos, "A temperature compensated digitally trimmable on-chip IC oscillator with low voltage inhibit capability," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, pp. 501–504.

[6] J. Lee and S. Cho, "A 10 MHz 80 μW 67 ppm/°C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18 μm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, 2009, pp. 226–227.

[7] Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho, "An on-chip CMOS relaxation oscillator with power averaging feedback using a reference proportional to supply voltage," in *IEEE Int. Solid-State Circuit Conf. Dig. Tech. Papers*, 2009, pp. 404–405.

[8] M. D. Ker and J. S. Chen, "New curvature-compensation technique for CMOS bandgap reference with sub-1-V operation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 667–671, Aug. 2006.

[9] C. Y. Yu, J. Y. Yu, and C. Y. Lee, "An eCrystal oscillator with self-calibration capability," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 237–240.

[10] T. Sakurai and A. R. Newton, "Delay analysis of series-connected MOSFET circuits," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 122–131, Feb. 1991.

Chien-Ying Yu was born in Hsinchu City, Taiwan, in 1984. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2006, where he is currently pursuing the Ph.D. degree in electronics engineering.

His research interests include VLSI architecture, low-power SoC, and wireless communication systems, especially in OFDM-based baseband transceiver for low-power WBAN systems and on-chip oscillator design.

Jui-Yuan Yu was born in Taipei City, Taiwan, in 1979. He received the B.S. and Ph.D. degrees in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2002 and 2008, respectively.

He is currently serving as a Postdoctoral Researcher with National Chiao-Tung University. His research interests include VLSI architecture, low-power SoC, and wireless communication systems, especially in OFDM-based baseband transceiver for high-speed WLAN, ultra-wideband (UWB) systems, and low-power WBAN systems.

Chen-Yi Lee (M'01) received the B.S. degree from National Chiao Tung University, Hsinchu, Taiwan, in 1982, and the M.S. and Ph.D. degrees from Katholieke University Leuven (KUL), Leuven, Belgium, in 1986 and 1990, respectively, all in electrical engineering.

From 1986 to 1990, he was with IMEC/VSDM, working in the area of architecture synthesis for DSP. In February 1991, he joined the faculty of the Electronics Engineering Department, National Chiao Tung University, Hsinchu, Taiwan, where he is currently a Professor and Dean of the Research and Development Office. His research interests mainly include VLSI algorithms and architectures for high-throughput DSP applications. He is also active in various aspects of high-speed networking, system-on-chip design technology, very low power designs, and multimedia signal processing. In these areas, he has authored or coauthored more than 180 papers and holds decades of patents.

Dr. Lee served as the Director of Chip Implementation Center (CIC), an organization for IC design promotion in Taiwan (2000/2008–2003/2012), and the microelectronics program coordinator of the Engineering Division under the National Science Council of Taiwan (2003/2001–2005/2012). Dr. Lee was the former IEEE Circuits and Systems Society Taipei Chapter Chair.