# In-Plane Gate Transistors With a 40-$\mu$m-Wide Channel Width

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***Abstract*—An in-plane gate transistor with a GaAs/AlGaAs 2-D electron-gas channel about 40 $\mu$m in width is investigated. The saturation region and the drain current modulation at different gate bias voltages are observed despite the wide channel. The surface-induced channel depletion is suggested as the main mechanism for the turn-off of the drain current at −10 V gate bias.**

***Index Terms*—In-plane gate transistors (IPGTs), 2-D electron gas (2DEG).**

## I. Introduction

THE in-plane gate transistor (IPGT) is one implementation of high-electron-mobility transistors (HEMTs) [1]–[3] in addition to the conventional scheme with gates above channels. Although simplified fabrication procedures for IPGTs are available, it is generally believed that nanometer-sized channels are necessary to avoid high threshold voltages. From this viewpoint, nanofabrication techniques such as the e-beam lithography seem inevitable for such devices [1]–[3]. For example, room-temperature transistor behaviors of IPGTs fabricated with repeated atomic-force-microscopy anode oxidation for electrical isolations were demonstrated [4]. The result revealed the potential of IPGTs in practical applications despite the expensive fabrication cost and high precision required. However, adoptions of nanofabrication techniques would limit further applications of IPGTs. Therefore, the development of IPGTs with micrometer channel widths based on the standard photolithography is appealing. The concern is whether clear transistor behaviors are attainable for such devices within a reasonable range of bias voltages.

In this letter, we investigate IPGTs with a standard but broad GaAs/AlGaAs 2-D electron-gas (2DEG) channel about 40 $\mu$m in width. Despite the broad channel of the device, generic transistor behaviors including flat saturation regions and drain–source current modulations are still observed at room temperature with the gate voltage ranging from −10 to 5 V. At temperatures lower than 100 K, the device cannot be turned off, although the gate terminals are significantly reverse biased. The phenomena are attributed to the effect of surface states on the trench and will be addressed later.

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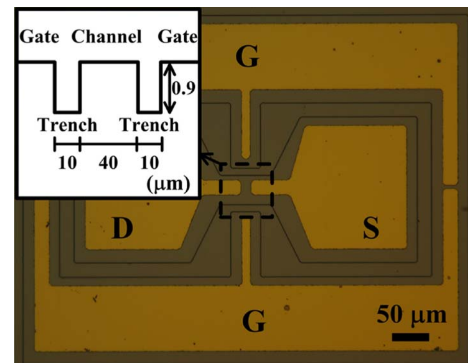


Fig. 1. Top-view picture of the IPGT taken under an optical microscope. (Inset) Schematic cross section of the device at the middle of the channel. The channel width and the trench depth/width in micrometers are labeled in the figure.

## II. Experiments

The wafer with a GaAs/AlGaAs 2DEG channel is prepared by a RIBER C21 solid-state molecular-beam-epitaxy system. The structure consists of a 30-nm Si-doped GaAs capping layer, a 15-nm Si-doped $Al_{0.3}Ga_{0.7}As$ donor layer, a 15-nm undoped $Al_{0.3}Ga_{0.7}As$ spacing layer, and a 200-nm buffer layer grown on the semi-insulating GaAs substrate. The doping densities of the n-type GaAs and $Al_{0.3}Ga_{0.7}As$ layers are $1.67 \times 10^{18}$ and $1.15 \times 10^{18}$ cm$^{-3}$, respectively. The Hall measurement indicates that the room-temperature sheet carrier density and electron mobility in the 2DEG channel at the undoped GaAs/$Al_{0.3}Ga_{0.7}As$ interface are $5.3 \times 10^{11}$ cm$^{-2}$ and $5.7 \times 10^{3}$ cm$^2/(\mathrm{V \cdot s})$, respectively. The device is fabricated under standard processing procedures including photolithography, wet etching, and metal evaporation. The top view of the device is shown in Fig. 1. The 40-$\mu$m channel is separated from gate terminals by trenches about 10 $\mu$m in width. The channel length is 15 $\mu$m. The isolation trench is 900 nm in depth and penetrates through the layer of 2DEG.

## III. Results and Discussions

The curves of drain currents $I_D$ versus drain–source voltage $V_{DS}$ of the device at $V_{GS} = 5, 0,$ and $-10$ V are shown

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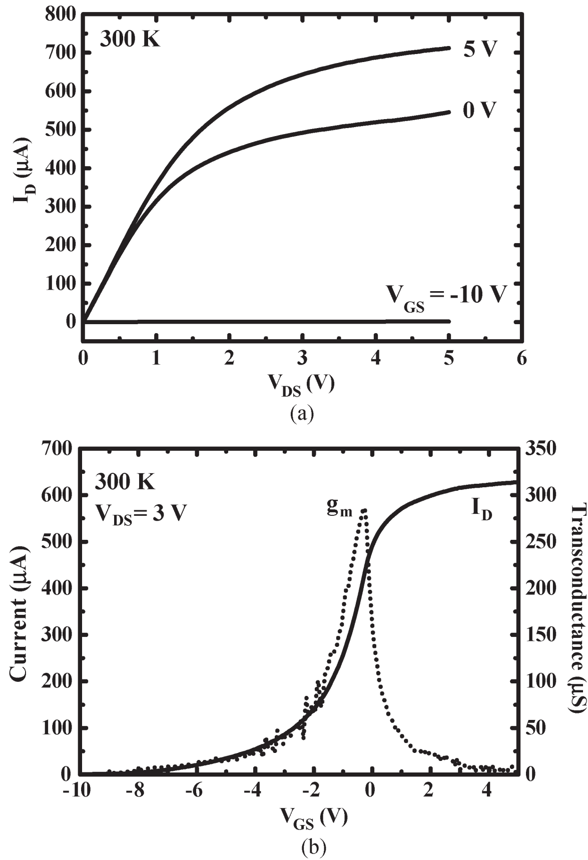


Fig. 2. (a) $I_D$–$V_{DS}$ curves of the IPGT at $V_{GS} = 5, 0,$ and $-10$ V. (b) $I_D$–$V_{GS}$ curve at $V_{DS} = 3$ V.

in Fig. 2(a). Saturation regions are present in the ON-state at $V_{GS} = 5$ and 0 V. The device is turned off at $V_{GS} = -10$ V. Unlike conventional top-gated HEMTs, the working principle of the IPGT is the lateral modulation of the depletion width through the bias control across in-plane gates and source/drain terminals. However, in view of the huge device with a 40-$\mu$m channel and 10-$\mu$m isolation trenches, it is surprising that a gate–source voltage of merely $-10$ V is sufficient to turn the device off. In Fig. 2(b), we show the curve of $I_D$ versus $V_{GS}$ at $V_{DS} = 3$ V. The corresponding transconductance $g_m$ of the device is also indicated in the figure. The maxima of $I_D$ and $g_m$ are 628 $\mu$A at $V_{GS} = 5$ V and 286 $\mu$S, respectively. Compared with the 40-$\mu$A $I_D$ and 20-$\mu$S $g_m$ of the IPGT with a 650-nm channel width in [4], much higher values are observed for the current device. These values are also larger than those of the device with multiple IPGT channels but shorter channel widths [5]. On the other hand, nonideal behaviors such as the increment of $I_D$ in the saturation region and the early saturation of $I_D$ versus $V_{GS}$ [see Fig. 2(a) and (b), respectively] are observable. Due to the large device size, typical short-channel effects in small devices should not be the cause to these phenomena. We suggest that the depletion related to the surface states, which may significantly alter the effective channel width under working bias conditions, leads to these nonideal behaviors. The estimation of the density of surface states described in the next paragraph indicates that the depletion related to the surface states could be quite possible.

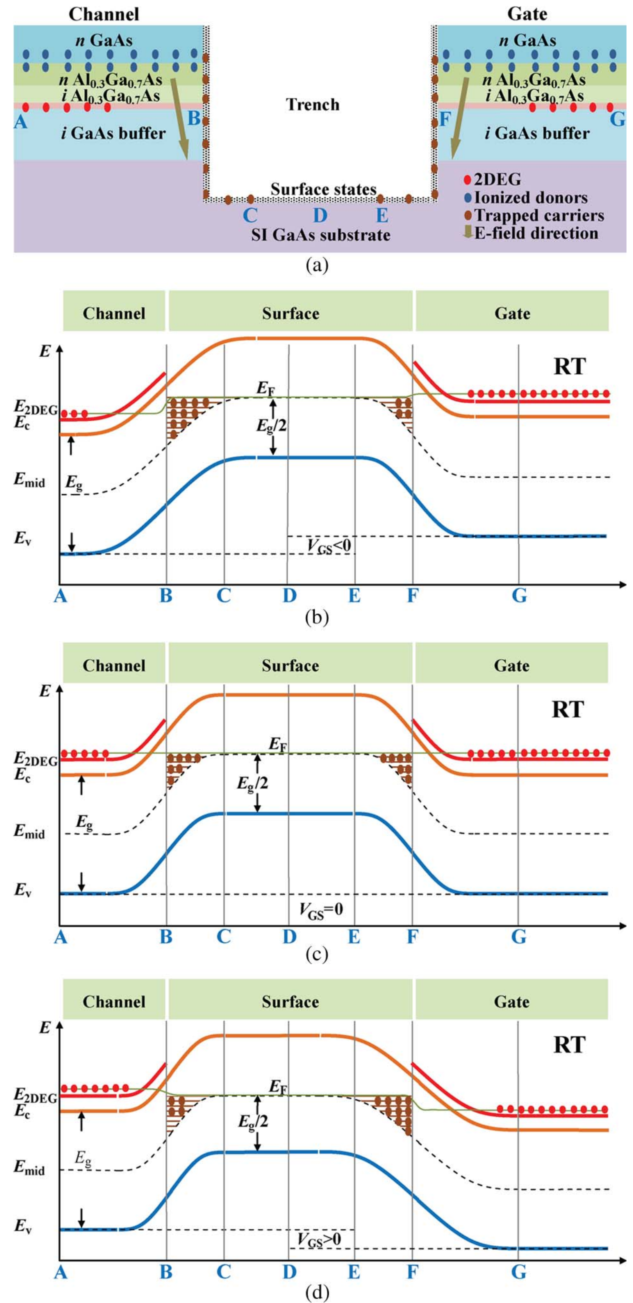


Fig. 3. (a) Cross-sectional view of the channel, the trench, and the gate. (Red) Carriers in 2DEG, (blue) ionized donors, and (brown) trapped carriers on the trench surface. (b)–(d) Room-temperature band diagrams from points A to G at $V_{GS} < 0$, $V_{GS} = 0$, and $V_{GS} > 0$, respectively. Due to the charge migration on the trench surface, the sizes of the depletion region and the charged surface area near the channel (gate) can be increased at $V_{GS} < 0$ (>0).

The unpassivated surface states on the trench may be the cause to the unexpected but desired features of the IPGT. The half-band-gap energy $E_g/2 = 0.712$ eV and surface density states $5 \times 10^{12}$ cm$^{-2} \cdot$ eV$^{-1}$ (native oxide) [6], [7] of GaAs indicate a density of about $3.56 \times 10^{12}$ cm$^{-2}$ for acceptor-like surface states. With a trench/channel area ratio of $2 \times 10/40 = 0.5$, the much lower carrier density of $5.3 \times 10^{11}$ cm$^{-2}$ in 2DEG could be significantly altered by the nearby surface. To understand the underlying working principle of the IPGT, let us consider the cross-sectional view of the device in Fig. 3(a).

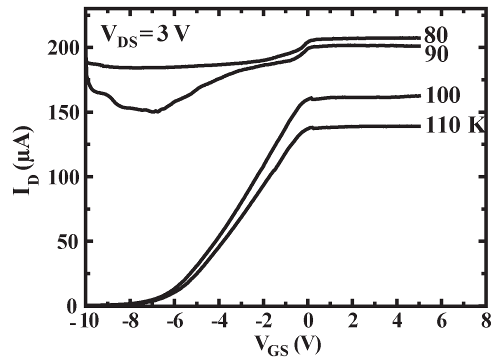


Fig. 4. $I_D$–$V_{GS}$ curves of the device at 80, 90, 100, and 110 K when $V_{DS} =$ 3 V.

The surface states on the trench trap the carriers in 2DEG. The negatively charged trench surface and ionized donors result in a built-in electric field pointing toward/along the surface, as indicated by the arrow in Fig. 3(a). The device physics will be more clearly grasped with the band diagram along the path from A to G in the figure. Point B (F) marks the entrance into the trench surface from the channel (gate), and C and E represent boundaries of charged regions on the trench surface.

The weak electric field directly penetrating through the thick air region in the trench (about $10^4$ V/cm at $V_{GS} = -10$ V, which is two orders of magnitude smaller than that in typical metal–oxide–semiconductor field-effect transistors) cannot effectively modulate the channel. While some part of $V_{GS}$ is taken up by the air region in the trench or surface region on the trench bottom, the portion in the form of barrier variations near the channel (gate)/trench surface should have higher impact on the channel modulation. The room-temperature band diagrams at $V_{GS} < 0$, $V_{GS} = 0$, and $V_{GS} > 0$ are shown in Fig. 3(b)–(d), respectively. Surface states are distributed within the GaAs band gap in interval BF. The Fermi level $E_F$ is close to the middle of the GaAs band gap in the inner of interval CE. Most of the charged surface states (acceptor-like) in interval BC $(E_F)$ are distributed between $E_F$ and the midband gap. The surface charge and ionized donors around the channel (gate) induce two potential barriers in intervals AC and EG, respectively. The sizes of the depletion region and charged surface area near the channel are broadened when $V_{GS} < 0$. While the depletion of 2DEG in the channel is due to the bias-induced repelling of the carriers into the source or drain terminals, the broadening of the charged surface area is caused by the surface electrons accumulated near the channel region. The inefficient carrier exchange maintains the Fermi level difference at two sides of point B (nonequilibrium). With a high density of surface states, it becomes possible to deplete the channel completely with an achievable bias voltage. In other words, depending on the sign and the magnitude of the gate bias, electrons may accumulate near the channel region (BC) or the gate region (FE). In this case, the 2DEG channel can be gradually turned off with a negative $V_{GS}$ value. When a positive $V_{GS}$ value is applied, the surface electrons are attracted and accumulated near the gate region, as shown in Fig. 3(d). In this case, the drain current increases with $V_{GS}$, as shown in Fig. 2(b). We note that the complete repelling of the surface charge near the channel might also cause the saturation of $I_D$ for $V_{GS} > 1$ V.

The migration capability of the surface charge plays an important role in the physical picture illustrated in Fig. 3(a)–(d). Based on this idea, if the charged carriers on the trench surface are all frozen out and immovable, the modulation characteristics of the IPGT should vanish. The curves of $I_D$ versus $V_{GS}$ with a fixed $V_{DS}$ of 3 V at 80, 90, 100, and 110 K are shown in Fig. 4. Although minor modulations of $I_D$ are still achievable when varying $V_{GS}$ below 100 K, the device cannot be switched off. We also note that, from Figs. 2(a) and 4, $I_D$ first drops as the temperature decreases. This drop is possibly caused by the more surface-state occupations, which deplete the channel. On the other hand, the increasing $I_D$ with decreasing temperature from 110 to 80 K is due to the higher electron mobility, which dominates at lower temperatures.

The possible application of this device architecture may be the high-speed phototransistors for light detections. It is possible to deplete the "dark current" of the device with a negative $V_{GS}$ value. With light irradiated on the channel region, which is not covered by oxides or metals, the photon-excited electrons can be collected with a positive $V_{DS}$ value and form photocurrents. Since there is no space charge such as the case of diodes and fixed $V_{GS}$ and $V_{DS}$ values are always applied to the device during operation, the channel mobility would be the sole parameter determining the response time of the phototransistor. By replacing the GaAs channel with InGaAs channels, extended detection wavelengths to the near-infrared range may be easily achieved with this device architecture.

## IV. Conclusion

In conclusion, IPGTs with a standard GaAs/AlGaAs 2DEG channel about 40 $\mu$m in width have been investigated. Surface-induced channel depletion has been suggested as the main mechanism responsible for the turn-off of the drain current at $V_{GS} = -10$ V. The incapability of turning off the channel below 100 K indicates that surface states play an important role for the IPGT. This demonstration of IPGTs with wide channels indicates an alternative scheme of dielectric-free transistors. The device architecture can be useful for high-speed phototransistors.

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