Reliability Analysis of Symmetric Vertical-Channel Nickel-Salicided Poly-Si Thin-Film Transistors

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***Abstract*—In this paper, a reliability analysis of symmetric Vertical-channel Ni-SAlicided poly-Si thin-film transistors (VSA-TFTs) is performed for the first time. First, we compare the drain-induced barrier-lowering effect (DIBL) of VSA-TFTs. The VSA-TFTs with thinner gate oxide thickness, an offset structure, and a longer floating n^+ region have better immunity to DIBL. Second, VSA-TFTs with a longer floating n^+ region also have better immunity under hot-carrier (HC) stress and self-heating (SH) stress. However, VSA-TFTs with a shorter floating n^+ region also have better immunity to positive gate bias (PGB) stress. Consequently, in order to optimize reliability characteristics, including SH stress, HC stress, and PGB stress, it is necessary to modulate the length of the floating n^+ region. Third, the PGB stress, rather than SH stress or HC stress, becomes a major issue for VSA-TFTs under the stress bias below 4 V. In other words, PGB stress will dominate the degradation behaviors when the stress bias is not high enough to achieve SH stress and HC stress. Finally, the worst degradation condition of VSA-TFTs under HC stress, similar to that of most TFT devices, occurs when the stress of V_G is less than half of V_D.**

***Index Terms*—Hot-carrier (HC) stress, polycrystalline silicon thin-film transistors (poly-Si TFTs), positive gate bias (PGB) stress, self-heating (SH) stress, symmetric S/D, vertical channel.**

I. Introduction

In THE LAST few decades, polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted considerable attention because of their high field-effect mobility and potential applications, including active-matrix liquid crystal displays (AMLCDs), system on panel, nonvolatile memory, and 3-D circuit integration [1]–[5].

In order to obtain high-performance poly-Si TFTs for more high-level applications in the future, several studies for the enhancement of the devices' structure and characteristics have explored, such as high-k materials, double-channel structures, nanowire-channel devices, and sequential lateral solidification–crystallization processes [6]–[9]. We also propose a novel structure poly-Si TFT device to improve device characteristics, which is called the symmetric Vertical-channel Ni-SAlicided poly-Si TFT (VSA-TFT) [10], [11]. It has the advantages of simple fabrication process, great potential for 3-D circuit integration, and easy scaling down of channel length without advanced photolithographic equipment.

The reliability of TFT devices is an important issue. Hence, before the practical application of such devices in AMLCDs or other high-level applications, their reliability characteristics must be clearly identified. Given this need, in this paper, we investigate the reliability characteristics of symmetric VSA-TFTs.

Several stress methods are generally used to understand the reliability characteristics of TFT devices, such as self-heating (SH) stress [12]–[15], hot-carrier (HC) stress [15]–[18], and bias temperature instability (BTI) stress [19]–[22]. In this paper, we compare the drain-induced barrier-lowering (DIBL) effect in Overlap, Offset, and GO-15-nm VSA-TFTs [11]. In addition, we investigate the reliability characteristics of VSA-TFTs, including SH stress, HC stress, and positive gate bias (PGB) stress.

II. Experiment

The key processes of VSA-TFTs were discussed in detail in our previous work [10], [11]. Fig. 1 displays the schematic cross section and top view of VSA-TFTs. The length of the floating n^+ region is defined by the mask channel length L_{mask}, where the mask channel width W_{mask} is equal to the effective channel width. The actual channel length of VSA-TFTs is defined as $2\times$ the total thickness of the poly-Si gate, which is equal to 0.4 μm. The length of the floating n^+ region is defined by the mask channel length. Therefore, the length of the floating n^+ region is designated as "L_{mask}" in our previous work [10], [11]. In order to avoid confusing L_{mask} with the actual channel length, we redesignate L_{mask} as L_f in this paper.

In this paper, we compare three kinds of VSA-TFTs, namely, Overlap, Offset, and GO-15-nm VSA-TFTs. The gate oxide thickness of the Overlap VSA-TFTs is 30 nm, and the overlap region between the gate and S/D edges is about 40 nm. The gate oxide thickness of the Offset VSA-TFTs is also 30 nm, but there is an offset region between the gate and S/D edges of about 40 nm instead of an overlap region. Fig. 2 shows the cross-sectional transmission electron microscope (TEM) microphotograph of the GO-15-nm VSA-TFTs [along the A$-$A$'$ direction in Fig. 1(b)]. The gate oxide thickness of the GO-15-nm VSA-TFTs is 15 nm, and the offset region between the gate and S/D edges is about 15 nm. Finally, all the devices were fabricated with 10-min NH_3 plasma treatment to passivate the defects in the poly-Si channel film [23].

Manuscript received February 3, 2012; revised April 30, 2012 and May 3, 2012; accepted May 7, 2012. Date of publication June 11, 2012; date of current version July 19, 2012. This work was supported by the National Science Council of Taiwan under Contract NSC-100-2221-E-009-012-MY3. The review of this paper was arranged by Editor B. Kaczer.

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Digital Object Identifier 10.1109/TED.2012.2199498

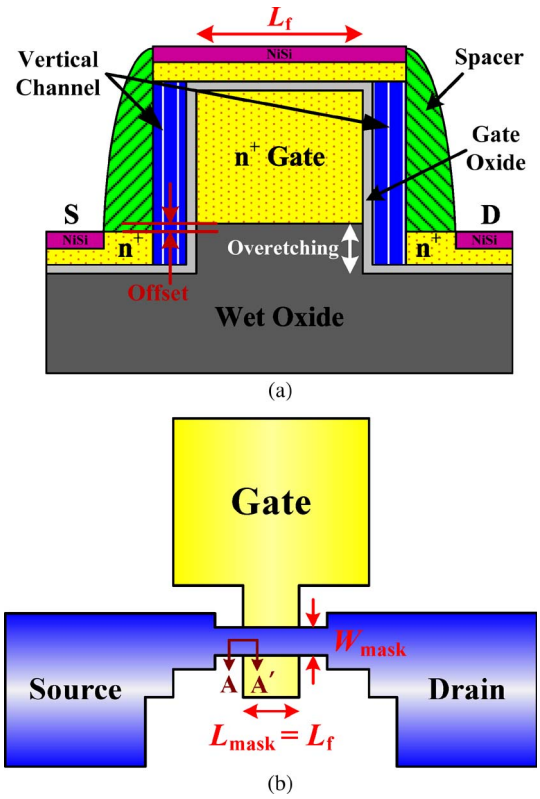

Fig. 1. (a) Schematic cross section and (b) top view of VSA-TFTs.

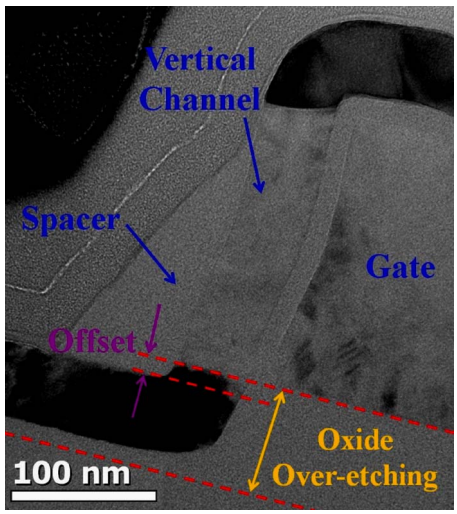

Fig. 2. Cross-sectional TEM microphotograph of GO-15-nm VSA-TFTs.

III. Results and Discussion

A. Device Performance and DIBL Effect

Several important parameters of Overlap, Offset, and GO-15-nm VSA-TFTs with 10-min NH_3 plasma treatment and $L_f = 3$ μm are listed in Table I. On-state current I_{on} is defined as the drain current at $V_G = 5$ V and $V_D = 0.1$ V, and off-state current I_{off} is defined as the minimum drain current at $V_D = 0.1$ V. The GO-15-nm VSA-TFTs have better subthreshold swing (S.S.) and higher on/off current ratio than the other devices. More detailed discussions of the VSA-TFTs' performance are reported in our previous work [10], [11]. Fig. 3 exhibits the DIBL effects of Overlap, Offset, and GO-15-nm

TABLE I
Important Parameters of Overlap, Offset, and GO-15-nm VSA-TFTs With 10-min NH_3 Plasma Treatment and $L_f = 3$ μm

	S.S. (mV/dec)	Mobility ($cm^2/V \cdot s$)	I_{off} (pA)	I_{on} (uA)	on/off ratio
Overlap VSA-TFTs	315	70	0.46	9.93	$> 10^7$
Offset VSA-TFTs	269	67	0.04	5.59	$> 10^8$
GO-15-nm VSA-TFTs	127	50	0.05	5.76	$> 10^8$

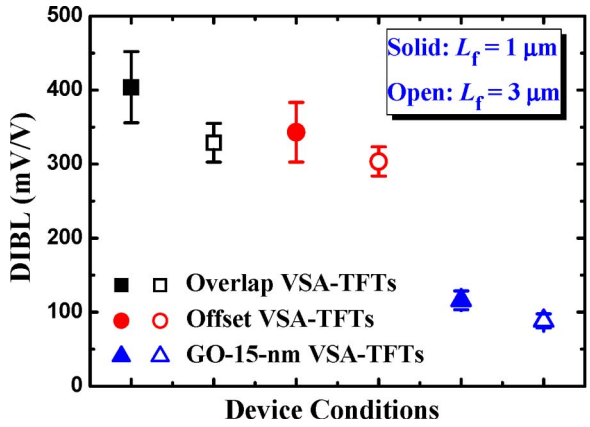

Fig. 3. DIBL effects of Overlap, Offset, and GO-15-nm VSA-TFTs with different L_f.

VSA-TFTs with different L_f. The GO-15-nm VSA-TFTs with $L_f = 3$ μm have the lowest DIBL value (88 mV/V) among the devices studied. The gate oxide thickness of the GO-15-nm VSA-TFTs is thinner than that of the other VSA-TFTs, resulting in better gate-to-channel control ability. Additionally, VSA-TFTs with $L_f = 3$ μm also have better immunity to DIBL effect due to the increased effective channel length resulting from the longer floating n^+ region. Therefore, the GO-15-nm VSA-TFTs with $L_f = 3$ μm have better immunity to DIBL effect. By the same token, the Offset VSA-TFTs have better immunity to DIBL effect than the Overlap VSA-TFTs due to the longer effective channel length resulting from the offset region.

In order to understand the reliability characteristics of TFT devices, the SH stress, HC stress, and PGB stress are used to understand the degradation behaviors (more than 30 devices were used to compare).

B. SH and HC Stressing

Fig. 4 shows the time dependence of the transfer characteristics of the GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under SH stress of $V_G = 5$ V, $V_D = 5$ V. It is obvious that I_{on}, S.S., and V_{th} are degraded after a long period of SH stressing. In addition, the device with $L_f = 1$ μm exhibits more serious degradation behavior than the device with $L_f = 3$ μm. The degradation behavior of SH stress is due to Joule heating and the damage generated along the entire channel [15]. Hence, the positive ΔV_{th} trends result from the degradation of S.S. and I_{on} after SH stress.

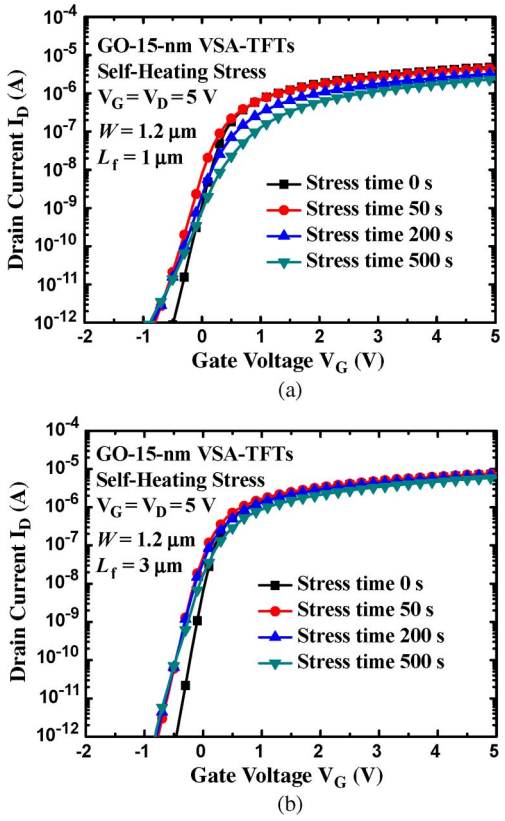

Fig. 4. Time dependence of transfer characteristics of GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under SH stress of $V_G = 5$ V, $V_D = 5$ V.

The threshold voltage shifts $\Delta V_{\rm th}$ and ON-state current change $\Delta I_{\rm on}$ percentage as a function of stress time for GO-15-nm VSA-TFTs with different L_f under different SH stress biases are extracted, as shown in Fig. 5. In general, $V_{\rm th}$ is defined as the applied gate voltage when the drain current achieves a normalized value. However, all the GO-15-nm VSA-TFTs have the same W/L. Therefore, $V_{\rm th}$ is directly defined as the applied gate voltage when the drain current $I_D = 20$ nA at $V_D = 0.1$ V. $I_{\rm on0}$ is the initial value of $I_{\rm on}$, and $\Delta I_{\rm on}$ is the changes in $I_{\rm on}$ after stress. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ become significant when the stress biases are raised. The degradation behaviors are also more serious when L_f is decreased from 3 to 1 μm. This is due to that the device with $L_f = 3$ μm has a longer electrical effective channel length, resulting in a slight reduction of drain currents under SH stress. The electrical effective channel length can be regarded as $2\times$ the total thickness of the poly-Si gate $+L_f$. Thus, the device with $L_f = 3$ μm has a longer electrical effective channel length than the device with $L_f = 1$ μm. Hence, GO-15-nm VSA-TFTs with $L_f = 3$ μm have better immunity to SH degradation. Fig. 6 shows the time dependence of the transfer characteristics of GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under HC stress of $V_G = 2.5$ V, $V_D = 5$ V. The S.S. characteristics and $V_{\rm th}$ are almost identical after stressing. However, negative $\Delta I_{\rm on}$ is obvious after HC stress. The degradation behavior of HC stress is different from that of SH stress. This is due to the energetic HCs generated near the drain side under a high drain electric field, causing damage in the grain boundaries and poly-Si/SiO_2 interfaces [15], [24].

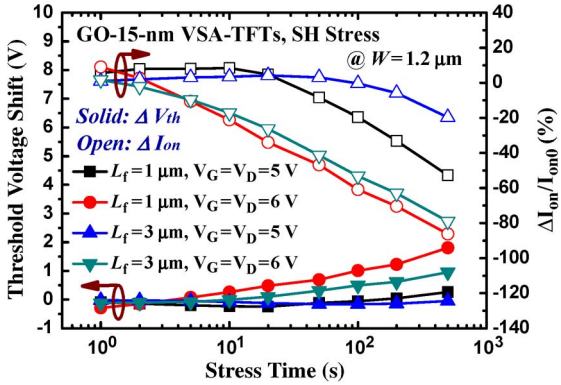

Fig. 5. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs with different L_f under different SH stress biases.

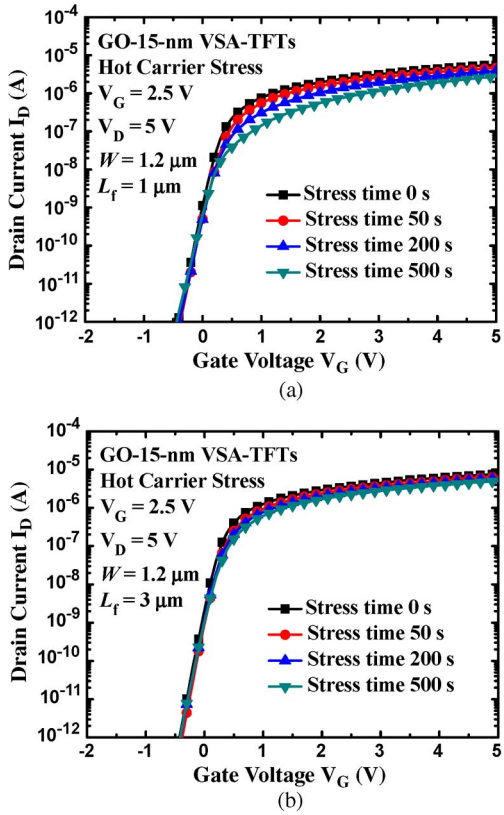

Fig. 6. Time dependence of transfer characteristics of GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under HC stress of $V_G = 2.5$ V, $V_D = 5$ V.

The damage to the grain boundaries and poly-Si/SiO_2 interfaces near the drain side strongly affects the ON-state carrier transport, leading to $I_{\rm on}$ degradation. Because HC stress results in local damage near the drain side, there is less damage in the channel region under lower gate bias than with SH stress. Therefore, degradation of S.S. and $\Delta V_{\rm th}$ is marginal under HC stressing. This SH and HC degradation phenomenon is consistent with the reported literature [12], [15], [16].

The $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs with different L_f under SH stress of $V_G = 6$ V, $V_D = 6$ V and HC stress of $V_G = 2.5$ V, $V_D = 5$ V are extracted, as shown in Fig. 7. Positive $\Delta V_{\rm th}$ and negative $\Delta I_{\rm on}$ after a long period of SH stressing are more serious

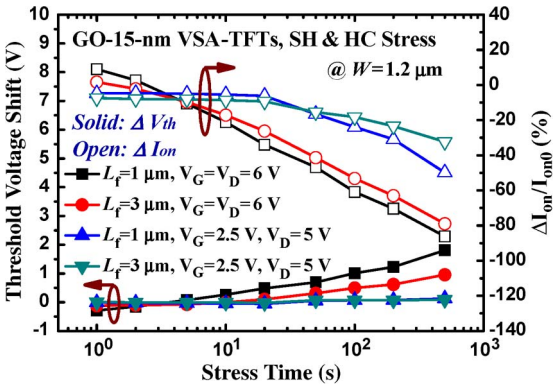

Fig. 7. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs with different L_f under SH stress of $V_G = 6$ V, $V_D = 6$ V and HC stress of $V_G = 2.5$ V, $V_D = 5$ V.

than those after a long period of HC stressing. Furthermore, GO-15-nm VSA-TFTs with longer $L_f = 3$ μm not only have better immunity to SH degradation but also have better immunity to HC degradation due to the reduced drain currents [15] and suppressed electrical field near the drain, respectively [10]. Hence, Joule heating and the HC impact ionization rate may be mitigated by increasing L_f, leading to better immunity to SH and HC degradation.

C. PGB Stressing

Fig. 8 shows the time dependence of the transfer characteristics of GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under PGB stress of $V_G = 5$ V, $V_D = 0$ V. Generally speaking, the devices will produce positive $\Delta V_{\rm th}$ and negative $\Delta I_{\rm on}$ after PGB stress. This indicates that electrons are trapped in the gate oxide under PGB stress. However, the trends of $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ in GO-15-nm VSA-TFTs under PGB stress conflict with reported results on the planar device [20]–[22]. In Fig. 8, it is evident that S.S. degradation, negative $\Delta V_{\rm th}$, and positive $\Delta I_{\rm on}$ occur at the same time. These measured results indicate that the degradation mechanism of GO-15-nm VSA-TFTs under PGB stress of $V_G = 5$ V, $V_D = 0$ V was not consistent with electrons being trapped in the gate oxide.

In our VSA-TFTs, the actual channel length is defined as $2\times$ the total thickness of the poly-Si gate. However, the electrical effective channel length can be regarded as $2\times$ the total thickness of the poly-Si gate $+L_f$. The floating n^+ region above the n^+ gate also suffers PGB stress. Apparently, another mechanism dominates the degradation behavior. Ma *et al.* proposed that the accelerated electrons would collide with the weak bond of the grain boundaries and damage the poly-Si channel film, generate the trap states, increase S.S., and reduce $I_{\rm on}$ under PBTI stress [20]. Cheng *et al.* and Lee *et al.* demonstrated that the TFT devices not only have Si–H bonds but also exhibit Si–N bond formation to terminate the dangling bonds in the grains and grain boundaries in the channel region after NH_3 plasma passivation [25], [26]. Many studies report that Si–H bonds are broken by HC stress and gate bias stress more easily than Si–N bonds [23], [26]–[30]. Liao *et al.* proposed that hydrogen may diffuse into the gate oxide and decrease the threshold voltage subsequently after the Si–H bond has been broken [22]. Furthermore, the stress bias of $V_G = 5$ V is not high enough to

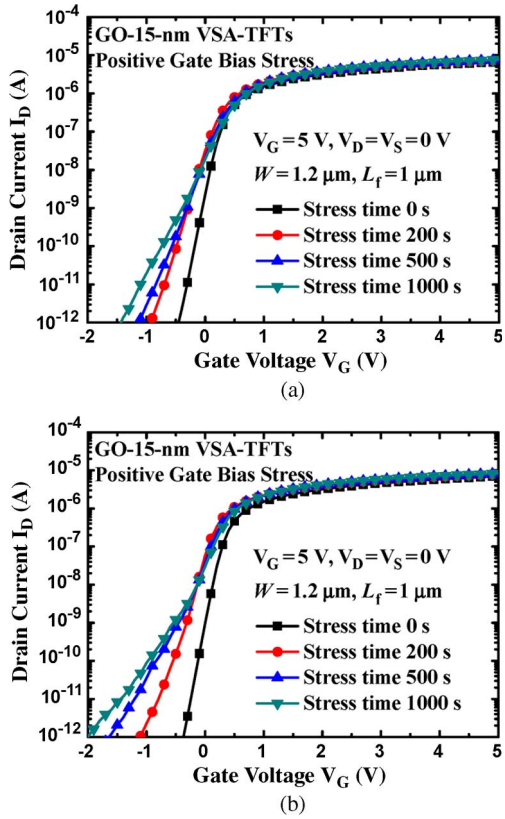

Fig. 8. Time dependence of transfer characteristics of GO-15-nm VSA-TFTs with (a) $L_f = 1$ μm and (b) $L_f = 3$ μm at $V_D = 0.1$ V under PGB stress of $V_G = 5$ V, $V_D = 0$ V.

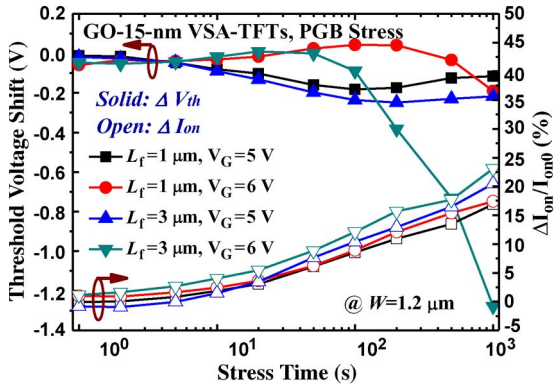

Fig. 9. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs with different L_f under different PGB stress.

cause Fowler–Nordheim (F–N) tunneling, leading to electrons being trapped in the gate oxide. Therefore, we believe that one of the reasons for negative $\Delta V_{\rm th}$ is due to the break in the weak Si–H bonds and the diffusion of hydrogen into the gate oxide and channel film. Another reason for negative $\Delta V_{\rm th}$ can be attributed to the degradation of S.S.

The $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs with different L_f under different PGB stress are extracted, as shown in Fig. 9. Fig. 9 shows that the negative $\Delta V_{\rm th}$ of GO-15-nm VSA-TFTs with $L_f = 3$ μm is more serious than that of GO-15-nm VSA-TFTs with $L_f = 1$ μm. We posit that the GO-15-nm VSA-TFTs with $L_f = 3$ μm have more hydrogen diffused into the gate oxide than the GO-15-nm VSA-TFTs with $L_f = 1$ μm.

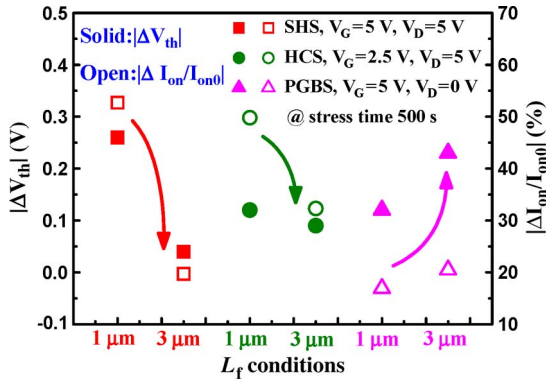

Fig. 10. Comparison the degradation behavior of SH stress, HC stress, and PGB stress of GO-15-nm VSA-TFTs with different L_f.

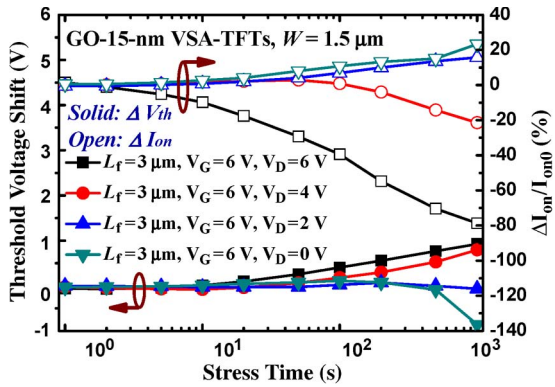

Fig. 11. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs under different stress biases with fixed $V_G = 6$ V and various V_D.

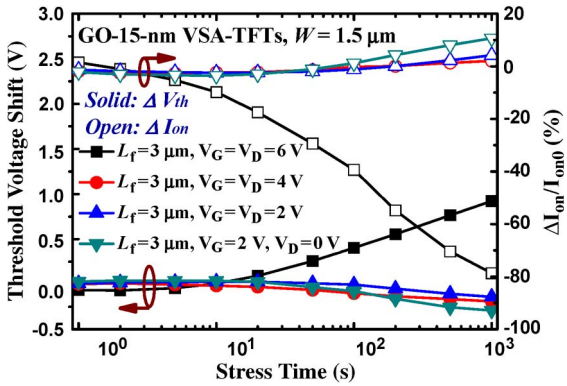

Fig. 12. $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs under different $V_G = V_D$ stress bias and PSG stress of $V_G = 2$ V, $V_D = 0$ V.

Because the GO-15-nm VSA-TFTs with $L_f = 3$ μm have a longer floating n^+ region and have more broken Si–H bonds after PGB stress, more hydrogen is diffused into the gate oxide, resulting in extra negative $\Delta V_{\rm th}$. Particularly, the negative $\Delta V_{\rm th}$ trend of the stress bias at $V_G = 6$ V for $L_f = 3$ μm and for $L_f = 1$ μm occurs after 50 and 200 s, respectively. The negative $\Delta V_{\rm th}$ of stress bias at $V_G = 6$ V for $L_f = 3$ μm after a long stress time is significant. This may be attributed to the greater number of broken Si–H bonds and more hydrogen diffusion into the gate oxide under higher gate stress bias. However, the negative $\Delta V_{\rm th}$ trend of stress bias at $V_G = 5$ V is more serious than when the stress bias at $V_G = 6$ V after 10 s, as shown in Fig. 9. According to the measured results, it appears that the stress bias of $V_G = 6$ V could generated more F–N and trap-assisted tunneling than the stress bias of $V_G = 5$ V. Under a stress bias of $V_G = 6$ V, the mechanism of broken Si–H bonds competes with F–N tunneling and trap-assisted tunneling. After a long stress time, the broken Si–H bonds are the main mechanisms in the more negative $\Delta V_{\rm th}$, particularly when $L_f = 3$ μm. Fig. 9 shows that GO-15-nm VSA-TFTs with $L_f = 3$ μm and stress bias at $V_G = 6$ V have more positive $\Delta I_{\rm on}$ than GO-15-nm VSA-TFTs with $L_f = 1$ μm and with a stress bias of $V_G = 5$ V. $I_{\rm on}$ after stress becomes higher than the initial state, probably due to negative $\Delta V_{\rm th}$. However, the degradation behavior of PGB stress for different L_f is opposite that of SH stress and HC stress, as shown in Fig. 10. Hence, in order to optimize reliability characteristics, including SH stress, HC stress, and PGB stress, it is important to trade off the length of the floating n^+ region. Here, we find the best condition to be $L_f = 2$ μm.

D. Bias Dependent on SH, HC, and PGB Stressing

Fig. 11 shows the $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs under different stress biases with fixed $V_G = 6$ V and various V_D. $\Delta V_{\rm th}$ changes from positive to negative as the V_D bias decreases due to reduced Joule heating rate. Furthermore, the V_G bias becomes increasingly important and dominates the degradation behaviors when the V_D bias is decreased. The $\Delta I_{\rm on}$ behavior also shows the same trends. $\Delta I_{\rm on}$ changes from negative to positive when the V_D bias is reduced. Hence, the degradation behavior is similar to that of PGB stress when the V_D bias is insufficiently high ($V_D \leqq 2$ V).

Fig. 12 shows the $\Delta V_{\rm th}$ and $\Delta I_{\rm on}$ percentages as a function of stress time for GO-15-nm VSA-TFTs under different $V_G = V_D$ stress biases and PSG stress of $V_G = 2$ V, $V_D = 0$ V. Except for the stress bias of $V_G = V_D = 6$ V, all show negative $\Delta V_{\rm th}$ and positive $\Delta I_{\rm on}$. Furthermore, the negative $\Delta V_{\rm th}$ and positive $\Delta I_{\rm on}$ of the stress bias of $V_G = 2$ V are more serious than those of the stress bias of $V_G = V_D = 4$ V and $V_G = V_D = 2$ V. This shows that PGB stress will dominate the degradation behavior when the stress bias is below 4 V (consistent with the results of Fig. 11). Hence, when the device completely operates at low voltage (below 4 V), the best condition for optimum reliability characteristics is $L_f = 1$ μm.

In both bulk silicon and single-crystal silicon, the worst HC degradation occurs when the stress bias of V_G is about half of V_D since it has the highest rate of impact ionization. This can be obtained from the substrate current $I_{\rm sub}$. When $I_{\rm sub}$ rises to the maximum value, the rate of impact ionization is highest [31]. However, the worst HC degradation in TFT devices always occurs when the stress bias of V_G is less than half of V_D [15], [22].

We sought to determine the worst HC degradation condition in our novel VSA-TFTs. Fig. 13 shows the (a) dependence of $\Delta V_{\rm th}$ on V_G stress at fixed $V_D = 6$ V with different constant I_D and (b) dependence of $\Delta I_{\rm on}$ on V_G stress at fixed $V_D = 6$ V with different stress times. Because S.S. is almost the same and negative $\Delta I_{\rm on}$ is obvious after HC stress, we use different

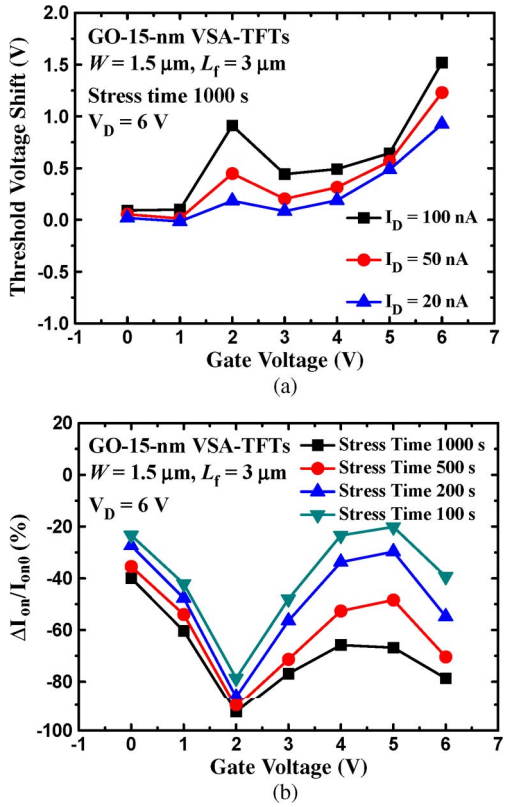

Fig. 13. (a) Dependence of $\Delta V_{\rm th}$ on V_G stress at fixed $V_D = 6$ V with different constant I_D and (b) dependence of $\Delta I_{\rm on}$ on V_G stress at fixed $V_D = 6$ V with different stress times.

constant I_D to extract $V_{\rm th}$. Results indicate that the largest $\Delta V_{\rm th}$ occurs when the stress bias of $V_G = 1/3$ V_D (except $V_G = 5$ and 6 V) under all constant I_D. It also indicates that the largest negative $\Delta I_{\rm on}$ occurs when the stress bias of $V_G = 1/3$ V_D for all stress times. Thus, the worst HC degradation condition is $V_G = 1/3$ V_D for novel VSA-TFTs.

IV. Conclusion

In this paper, we have investigated the DIBL effect and the reliability issues, including SH stress, HC stress, and PGB stress, for VSA-TFTs. The GO-15-nm VSA-TFTs have better immunity to DIBL effect than the Overlap and Offset VSA-TFTs. Additionally, VSA-TFTs with a longer floating n^+ region have better immunity to DIBL effect. In HC stress and SH stress, VSA-TFTs with a longer floating n^+ region also have better immunity. However, VSA-TFTs with a shorter floating n^+ region have better immunity to PGB stress. PGB stress will dominate the degradation behaviors when the stress bias is below 4 V. Consequently, the length of the floating n^+ region is the key parameter for reliability characteristics. Finally, the worst HC degradation condition of VSA-TFTs, which is similar to that of most TFT devices, occurs when the stress of V_G is less than half of V_D.

Acknowledgment

The authors would like to thank the Nano Facility Center of National Chiao Tung University and the National Nano Device Laboratory for providing process equipment.

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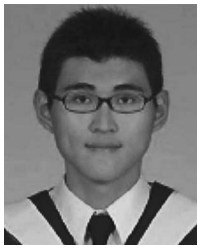

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