An Embedded Dynamic Voltage Scaling (DVS) System Through 55 nm Single-Inductor Dual-Output (SIDO) Switching Converter for 12-Bit Video Digital-to-Analog Converter

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Abstract—This paper proposes a 55 nm CMOS 12-bit current-steering video digital-to-analog converter (DAC) directly powered by the single-inductor dual-output (SIDO) switching converter to compose a dynamic voltage scaling (DVS) system and improve the power efficiency. Dual-DVS control in both digital and analog circuits can effectively reduce power consumption. With various supply voltages, the video DAC can meet several different specifications in the power optimized (PO) mode. Furthermore, for DAC, the proposed 3S method, including finger separating, splitting and shifting, achieves good differential non-linearity (DNL) performance to 0.78/0.4 least significant bit (LSB) and integral nonlinearity (INL) 1.3/1.0 LSB (with/without SIDO converter) without additional calibration. It also suppresses the switching noise interference from the SIDO converter. Moreover, for SIDO converter, the cross-regulation performance is greatly improved in both transient and steady state to achieve lowest interference for the analog supply. The total power efficiency can be improved up to 11.5% and 28% in the DVS and the PO mode. The SIDO supplied DAC with the dual-DVS function achieves 69.88 dB spurious free dynamic range (SFDR) at the 1 V output swing and 1 MHz input. The proposed intrinsic 12-bit DAC and SIDO converter achieve high definition video DAC performance with the benefit of area and energy efficiency.

Index Terms—Single-inductor dual-output (SIDO), digital to analog converter (DAC), DC-DC converter, dynamic voltage scaling (DVS), least significant bit (LSB), differential nonlinearity (DNL), integral nonlinearity (INL), spurious free dynamic range (SFDR).

I. INTRODUCTION

IN RECENT years, the integrated circuits in nanometer technology have tailored for very high density digital and mixed-signal integration applications. The trends of system-on-a-chip (SoC) integration lead the progress of portable devices to combine all the multimedia, communication, storage and processing functions as shown in Fig. 1.
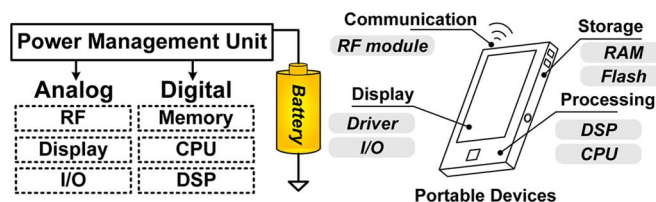
Fig. 1.   The system structure of a portable device.

Such a circuitry system can be roughly divided into digital and analog circuits. The digital circuits switch the voltage level up to supply voltage and down to the ground with high noise immunity. Remarkable improvements in the power consumption were achieved by the embedded power management unit (PMU), especially in nanometer technology SoC design with sub-1 V core devices. The PMU is often designed to fulfill different power requirements of each sub-circuit. Using input/output (I/O) devices with high-voltage tolerance can ensure the chip to be powered by the Li-Ion battery.

Low dropout regulators (LDRs) and switching regulators (SWRs) are two typical power modules in the design of embedded PMU [1] as shown in Fig. 2. LDRs possess the advantages of low noise and fast response, but suffer low efficiency once there is large dropout voltage. On the contrary, SWRs, which include the inductor-based and capacitor-based converters, have high conversion efficiency over a wide voltage range at the cost of output voltage ripple. Besides, the switching ripple will be coupled or fed into the circuits so as to influence the accuracy and quality of signals. As a result, the noise-sensitive analog circuit is often supplied by the LDRs, which behave as the post-regulators. There are different combinations of power modules as in Fig. 2(b), which depends on the system requirements. In Type I power module, the SWR is placed in front of the LDR to avoid large power loss caused by the dropout voltage in the LDR. For both analog and digital circuits with different supply voltage, two SWRs are needed at the cost of large number of external passive inductors or capacitors. Because digital circuit is not sensitive to noise, it can be directly supplied by the SWR as Type II with high efficiency. To improve the integration performance, only one SWR is used to simultaneously supply multiple outputs for further reducing the
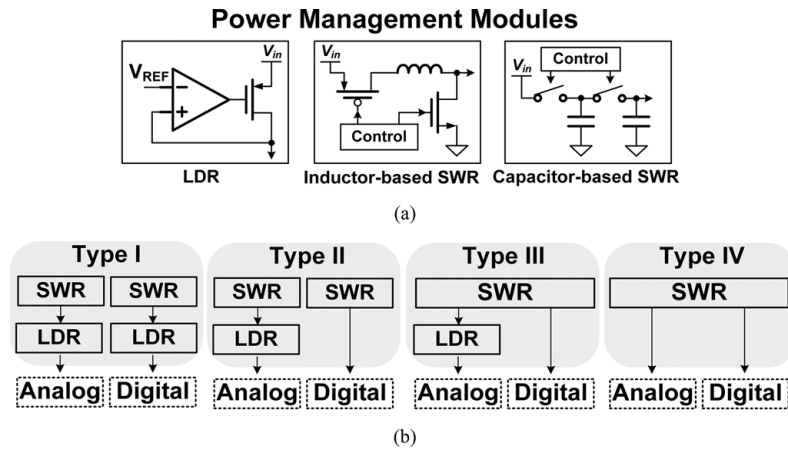
Fig. 2. (a) The structure of different power modules. (b) Combination of power modules.

number of external components and the area of printed-circuit board (PCB) as the Type III. The SWR can be single-inductor multiple-output (SIMO) converter [2]–[4] to replace the use of many different types of SWR for high integration. Specially, careful design in analog circuit and the SIMO converter can further remove the demand of the LDR as depicted in the Type IV design. In this paper, the Type IV design is proposed to show the possible PMU implementation in high integration of SoC without suffering large chip area, external components and low power efficiency. Furthermore, the analog blocks in the SoC can also be supplied by the SWR if the performance, like voltage ripple, line/load regulation, and driving capability, can be improved.

From above demands, the SIMO DC-DC converter [2]–[4], which uses only one inductor, is an appropriate PMU solution. Minimization of external components achieves compact size and simultaneously provides two output voltages to different circuit blocks. Besides, the benefit of high efficiency can be guaranteed due to the characteristics of switching converters. The noise immunity in the analog blocks and the cross-regulation in the SIMO converter need to be carefully enhanced to meet the power requirements.

Furthermore, owing to finite power supplies in portable devices, it is imperative to have an integrated PMU with the dynamic voltage scaling (DVS) [5], [6] methodology in digital circuits. Scaling the supply voltage can reduce the power consumption in different operation status. As we known, the DVS technique was seldom implemented in the analog blocks due to the deteriorated performance caused by the reduced voltage headroom. The analog circuits are sometimes more power-consuming than the digital blocks. Thus, the DVS technique can also be implemented in some specific analog circuits with a great power reduction for system sustainability. The battery life can be further extended due to the removal of the LDRs and the implementation of the analog DVS technique. Dual-DVS technique is implemented in the proposed DVS system which includes an embedded power module (SIDO converter) and a mixed-signal circuit to show the energy-efficient and area-efficient performance compared to the prior arts. In this paper, to prove the feasibility of dual-DVS on both digital and analog circuits, an application of high quality video digital-to-analog

converter (DAC) circuit [7], [8], is taken into the system design, which is composed of digital control circuits and high accuracy analog circuit. The proposed 55 nm CMOS intrinsic 12-bit video DAC directly powered by the SIDO converter can simultaneously achieve high performance and efficiency in various operation modes through the implementation of dual-DVS technique. That is, the dual-DVS technique can be fully implemented in the SoC with remarkable improvement on power efficiency to demonstrate its benefit in portable device applications.

The paper is organized as follows. The structure of DVS system is depicted in Section II. Section III illustrates the proposed 12-bit video DAC and the physical implementation. The proposed SIDO DC-DC converter and the DVS power optimization are described in Section IV. Experimental results are shown in Section V. Finally, a conclusion is drawn in Section VI.

II. STRUCTURE OF DYNAMIC VOLTAGE SCALING SYSTEM

Recently, with the progress of storage and signal processing, high definition (HD) video and audio formats have become more and more popular in home appliances. Meanwhile, the advanced display technology on liquid crystal display (LCD) also improves the color gradation and response time on panels. Thus, high quality multimedia entertainment leads the prosperity of appliance and media industry. Conventional interfaces such as "true color" [9] are defined as that at least 256 shades of red, green, and blue (RGB), for a total of at least 16,777,216 color variations. It has been upgraded to higher pixels and finer resolution formats beyond "true color" such as HD video. There is also other display formats such as Y′CbCr [10], which needs higher resolution than 8-bit in luminance(Y). The specifications of a video DAC should also be upgraded in both resolution and data rate. For example, the video DAC in blue-ray HD video players needs 12-bit resolution with the data rate of 150 MHz [7]. The portable devices also follow the trends of HD multimedia with more concerns on compact size and high power efficiency.

For a video DAC, there are many different component interfaces [11] as shown in Fig. 3. The output voltage varies in different ranges in different video interfaces. Such as in the Pb/Pr channel of Never The Same Color (NTSC) interface, the output

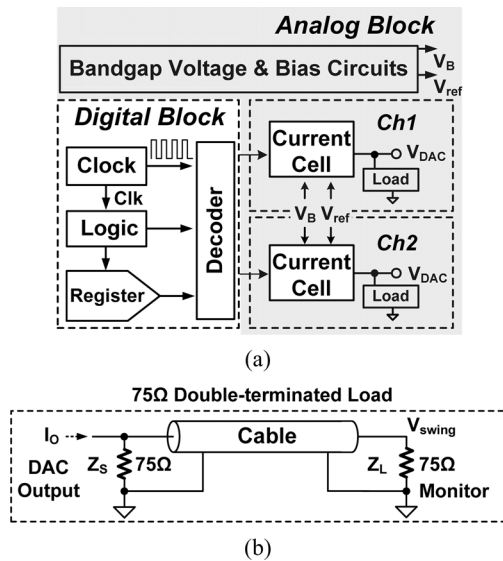Fig. 3. Different video interface applications and Signal range.

Fig. 4. (a) The structure of the video DAC. (b) Standard double terminal load of video DAC.

voltage difference is 0.7 V or 1 V. In the Y channel of Phase Alternating Line (PAL) interface, the output voltage difference is 0.5 V or 0.7 V. The synchronization voltage level can reset the pixel with an additional synchronization circuit. The video DAC needs the synchronization process in some applications. As a result, the total video DAC output voltage range may extend to 1.3 V [11]. The video DAC in Fig. 4(a) is designed to meet several different video interface specifications [10]. Each video DAC has several output channels depending on the application. The standard output loading is shown in Fig. 4(b) which is the double-terminated load of 75 Ω. The video DAC needs to have direct driving capability and large current delivering ability to generate large output swing on the load resistor. Thus the current-steering DAC architecture is chosen for benefiting both large current driving capability and high operation speed. The video DAC has both digital and analog circuits. Digital circuits include the clock generator, decoder and control logic. Analog circuits include the current cell array and the bandgap reference circuit which generates the bias voltage.
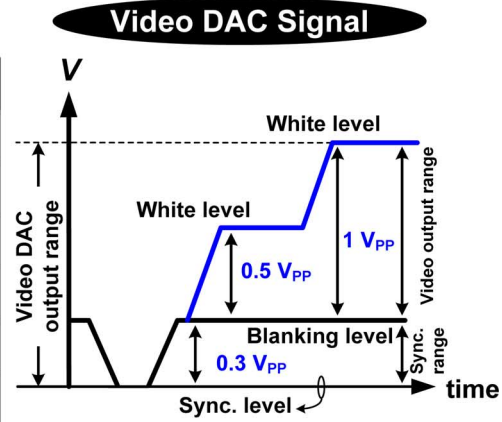
Fig. 5(a) shows the system architecture of the 12-bit video DAC with the DVS controller commanded by external control signals, V_{DVSA} and V_{DVSD}, which also control the SIDO converter. Here, the SIDO switching DC-DC converter, supplied by the Li-Ion battery, will generate two voltage levels: V_{OA} and V_{OB}. The V_{OA}, ranging from 1.75 V to 2.5 V, can supply the analog circuits. The V_{OB}, with the range from 0.8 V to 1.1 V, drives the digital circuits of the video DAC which is implemented by low-voltage core devices in nanometer (nm) process. The digital input code $D[0:11]$ will be transferred to the analog output voltage V_{DAC}. The DVS controller sends two two-bit signals V_{DVSA} and V_{DVSD} to determine dynamic analog and digital voltages, respectively. Through the DVS control, the V_{DAC} is selected from different full scale range from 500 mV to 1.3 V for various output requirements. Meanwhile, the SIDO converter will dynamically adjust the supply voltage V_{OA} to optimize the power consumption as shown in Fig. 5(b).

III. PROPOSED 12-BIT CURRENT STEERING VIDEO DAC WITH DVS SCHEME

A. Structure and Operating Principle

To successfully separate the 12-bit (4096) different color levels in high-definition video applications, the key performance index (KPI) of the video DAC is the linearity, especially for differential nonlinearity (DNL). The intrinsic 12-bit video DAC specifications include DNL < 1 LSB and integral nonlinearity (INL) < 2 LSB with the maximum clock frequency 150 MHz for 1080 pixels HD video display application. The current cell mismatch, including both global and local variation, will impact the video DAC performance. The proposed current cell with a cascode current mirror and switch logic is depicted in Fig. 6(a). By steering the output current to load resistor or GND, the DAC can generate output voltage level according to the digital input. The segmented architecture is commonly used to achieve high linearity current cell array, and the effects of unary and binary segmentation on the DNL and INL performances were studied in the literatures [8], [12]. The DNL is strongly affected by the segmentation scheme. Higher unary segmentation produces better DNL performance. On the other hand, the current cell array area will increase in the unary
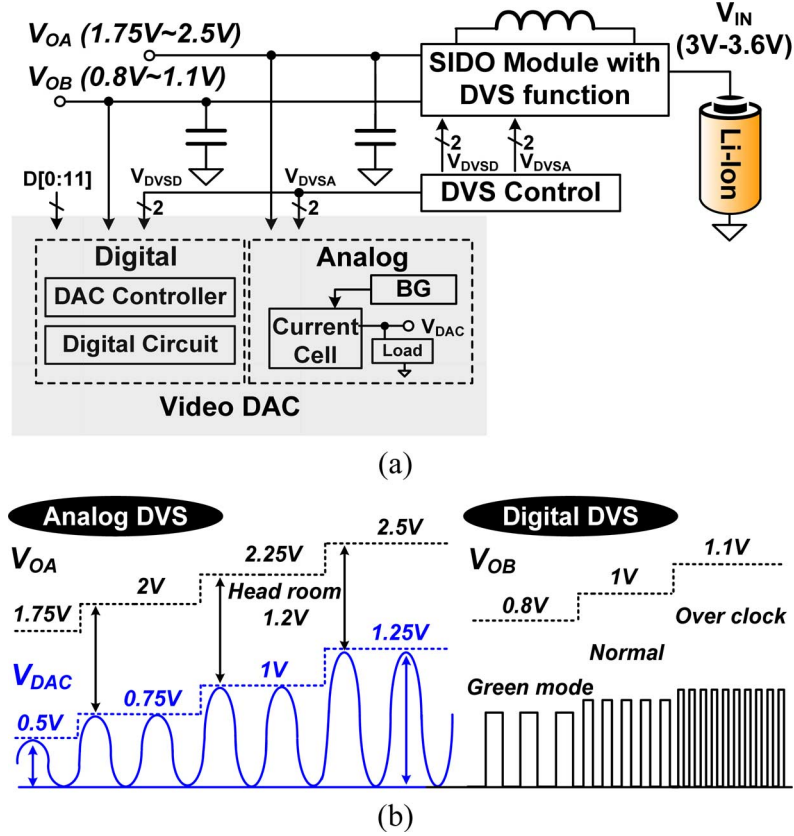
Fig. 5. (a) The structure of proposed DVS system. (b) The relationship of dual-DVS function.

segmentation. Higher binary segmentation achieves smaller DAC layout area.

To leverage the advantages of both unary and binary architectures, the segmentation of the 12-bit DAC is 6-bit thermometer code for the most-significant-bit (MSB) cells, 3-bit thermometer code for sub-MSB cells, and 3-bit binary LSB cells, as shown in Fig. 6(b). The 3-bit sub-MSB is adopted by thermometer decoding to avoid mismatches in higher sub-MSB bits. Comparing with 6-bit binary LSB decoding, the 3-bit binary LSB and 3-bit thermometer sub-MSB can achieve better linearity due to the unary sub-MSB cells. As illustrated in Fig. 7, the main area of the DAC layout is in the 6-bit MSB array. The 3 + 3 sub-MSB and LSB only occupy a small portion of the total area. As a result, the "6 + 3 + 3" structure successfully achieves better linearity, and is of comparable area with "6 + 6" architecture.

To improve the DAC's dynamic performance [13], the output impedance of the current cell must be large enough to function as a good Norton equivalent current source [14]. The current-steering DAC's spurious free dynamic range (SFDR) is approximated by (1). The R_{cell} is the output impedance of a single cascode current cell, the R_{load} represents the load resistance, and N is the resolution of the DAC. Through the standard double-terminated load and the SFDR requirements of 75 dB, the theoretical resistance value of R_{cell} is about 200 MΩ. The proposed R_{cell} in a single current cell is over 250 MΩ.

$$\text{SFDR} \approx 20\log\left(\frac{R_{cell}}{R_{load}}\right) - 6(N - 2) \qquad (1)$$

The wide-swing cascoded current-bias architecture improves the PSRR of the DAC. The use of noise coupling capacitor C_{C1} is to suppress the switching noise interference from the SIDO converter. In this design, the full-scale output current is 34 mA. At the equivalent resistive load of 37.5 Ω, the maximum output voltage is 1.3 V. Each MSB current cell will deliver 0.541 mA output current. The scalable current mirror can adjust the mirror current according to the DVS control signal, V_{DVSA}, and generate various output swings depends on the system applications. Controlling the dynamic scaling voltage provided by the DC-DC SIDO converter and the DAC output full-scale voltage, the voltage headroom of the video DAC can be optimized for better performance and less power dissipation.

B. Physical Implementation of the 3S Method and Noise Suppression

The physical implementation of the current cell array introduces the finger-split, shift and separate (3S) layout method. To reduce the steering current mismatch, the finger-split and shift technique, which is a two-dimensional matching layout as shown in Fig. 7(a). Compared with the conventional finger-split matching method, the proposed finger-split and shift method can further randomize the placement of the current cell to improve the linearity. In the physical implementation, the 12-bit control code is separated into two parts. The 3-bit least-significant-bit (LSB) current cell array and 3-bit sub-thermometer control array are placed in common centroid layout as in Fig. 7(b).
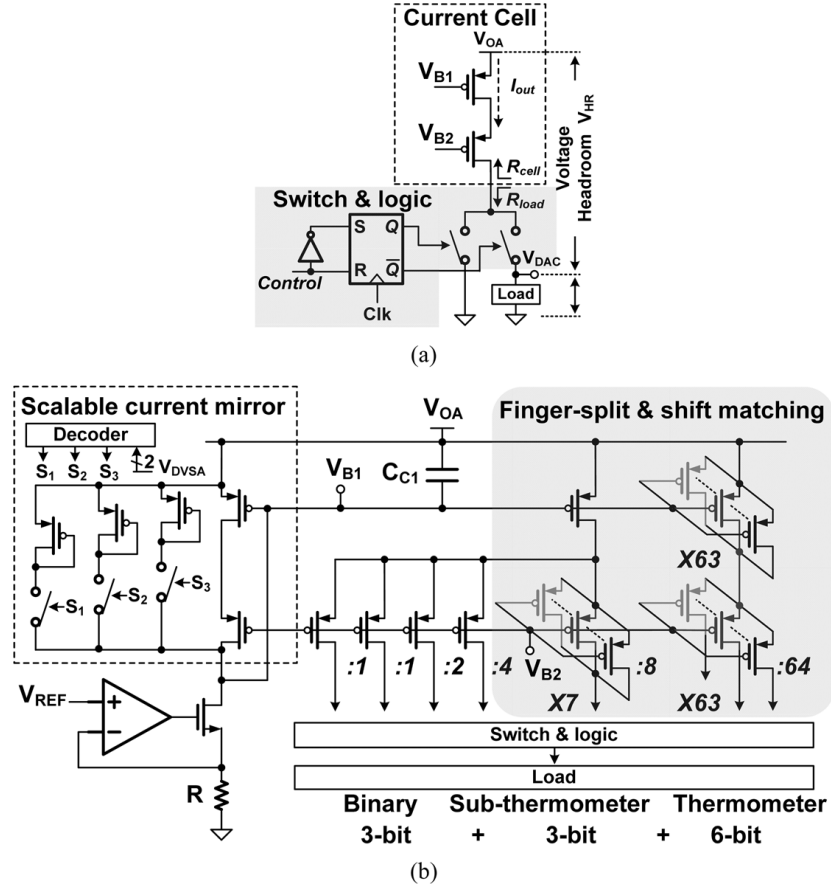
Fig. 6. (a) Single current cell and the switch. (b) Architecture of current cell in the 12-bit current steering DAC.

Fig. 7(c) shows the layout arrangement. The 6-bit MSB current cell array is placed by the finger-split and shift method. Each MSB current cell has 64 units of LSB current cell. The MSB array has been divided into 4 quadrants for the matching purpose, each quadrant has 16 fingers of each MSB cell as in Fig. 7(b). Sixteen fingers in a quadrant are separated in 8 groups by putting two cells together. The drain and source terminals of each cell can be shared to reduce large layout and routing area. The two-dimension finger-split and shift placement is extended as depicted in Fig. 7(a) into 64 cells and called as a group. Thus, each group has 128 unit cells ($16 \times 2 \times 4$), the row and the column will shift by each group as illustrated in Figs. 7(b) and (c). Since the finger-split and shift technique is implemented cyclically, by mirroring the layout of each quadrant in two dimensions, the layout complexity is reduced. As a result, it minimizes the area penalty layout complexity. The tail group and cascode group use the same layout matching method.

The size of current source constituted by P-type MOSFET is chosen by the tradeoff between the mismatch and the silicon area. According to the Pelgrom MOSFET mismatch model as (2) [15], the current variation is related to two process parameters, A_β and A_{VT}.

$$W \cdot L \geq \frac{\left[A_\beta^2 + \frac{4 \cdot A_{VT}^2}{(V_{GS} - V_T)^2}\right]}{\left[2 \cdot \left(\frac{\sigma(I)}{I}\right)^2\right]} \qquad (2)$$

Refer to process mismatch parameters, A_β is the process mismatch constant induced by MOSFET aspect ratio and other process parameters, e.g., mobility; A_{VT} is the threshold voltage variation constant. V_{GS} is the gate-source voltage and V_T is the threshold voltage. To achieve performance-optimized design, the overdrive voltages of the current cells and the unit current are designed carefully to meet the mismatch requirement at the largest output voltage swing of 1.3 V. According to Brownian-Bridge-Based statistical analysis, the 12-bit current-steering DAC should have relative standard deviation $\sigma(I)/I = 0.24\%$, which corresponds to the INL smaller than 0.5 LSB [16]. By putting in the process mismatch parameter and the bias voltage V_{GS}, the minimum device size can be derived as $(W \cdot L) = 4.9~\mu\text{m}^2$. For maximum output swing of 1.3 V, the LSB current is 8.3 μA. Thus the selected current cell device size is $W = 4.8~\mu$m and $L = 1.1~\mu$m.

In advanced CMOS technologies, there will be layout dependent effects (LDE), such as length of oxide-diffusion (LOD) and well proximity effects (WPE), which will impact the MOS array global variation performance. For large MSB array, the current cells will be more uniform at the center than at the corner. In the proposed 12-bit DAC layout, one surrounding ring of dummy current cells is added to prevent the layout-dependent effects. The more dummy cells were added, the smaller current mismatch between center and corner cells. However, it is at the cost of area overhead. The LDE (Layout Dependent Effect) will impact the current mismatch and result in worse DNL than those in

No matching

| 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 | 4 | 4 | 4 | 4 |

Finger-split

| 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 | 1 | 2 | 3 | 4 |

Finger-split & shift

| 1 | 2 | 3 | 4 | 4 | 1 | 2 | 3 | 3 | 4 | 1 | 2 | 2 | 3 | 4 | 1 |

Finger-split & shift in 2-dimension

1	2	3	4	16	13	14	15	11	12	9	10	6	7	8	5
5	6	7	8	4	1	2	3	15	16	13	14	10	11	12	9
9	10	11	12	8	5	6	7	3	4	1	2	14	15	16	13
13	14	15	16	12	9	10	11	7	8	5	6	2	3	4	1

(a)

Digital circuit

Q1 Q3

Q2 Q4

LSB array Cascode group Tail group

(b)

6-bit LSB Current Cell

8

84	85	86	87	87	86	85	84
85	84	83	82	82	83	84	85
86	83	4	81	81	4	83	86
87	82	81	1	2	81	82	87
87	82	81	2	1	81	82	87
86	83	4	81	81	4	83	86
85	84	83	82	82	83	84	85
84	85	86	87	87	86	85	84

8

Common centroid

MSB Current Cell (Q1)

16 x 2

1
2
3
4

Group 1
Group 2
Group 3
Group 4
Group 5
Group 6
Group 7
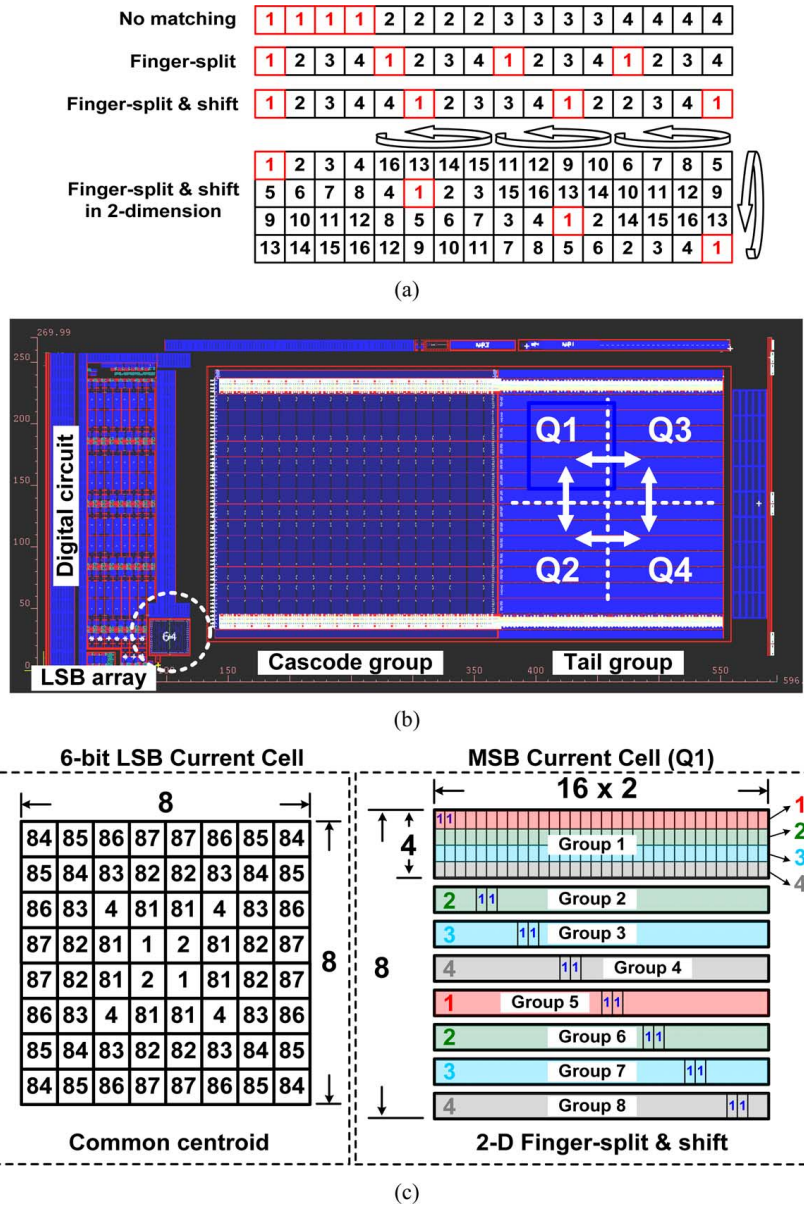Group 8

2-D Finger-split & shift

(c)

Fig. 7. (a) Finger-split and shift method. (b) Layout of the DAC. (c) Layout arrangement.

theoretical results. Assuming symmetrical linear, symmetrical square and directional linear global variation as in Fig. 8(a), the mismatch of each current cell can be modeled by setting the current mismatch percentage of the center cell versus the corner cell (2% in this example). After applying 3S layout style, it can be seen that the finger-split and shift method achieves good matching performance of MSB array with DNL $\sim$ 0.15 LSB under all three different global variations. Compared with prior arts [17], [18], it shows worse linearity at symmetrical square condition ($\sim$ 0.8 LSB) and better DNL at directional linear condition ($\sim$ 0.06 LSB) as shown in Fig. 8(b). For large MOS arrays in advanced technology, it is more likely to have bowl-shape-like global variations due to the layout dependent effect. Besides, due to the cyclic property of finger-split and shift methodology, the 3S decoding sequence will not introduce large area overhead or layout complexity. In this work, the 1-ch DAC layout area is only 0.12 mm^2 with 12-bit intrinsic linearity.

The optimized 3S decoding sequence can also minimize the surrounding dummy cell width because it can sustain larger center to corner current mismatch.

When the power source disturbances, it will impact the bias condition of the current cell and thus deteriorate the output current. As a result, the DNL and the INL will become worse when DVS is on and under power optimization mode. During the measurement, each current cell was turned on sequentially. If the power supply disturbed, the gate-source/drain-source voltage vary, the output current will also varies a little even under the power supply rejection. For high resolution and good signal quality, the power supply noise needs to be well handled not only from the circuit design, but also from the physical implementation. Fig. 9 shows three different matching manners of the 12-bit current-steering DAC architecture. To suppress the switching noise from the SIDO converter and current mismatch from the current steering control, the layout technique must
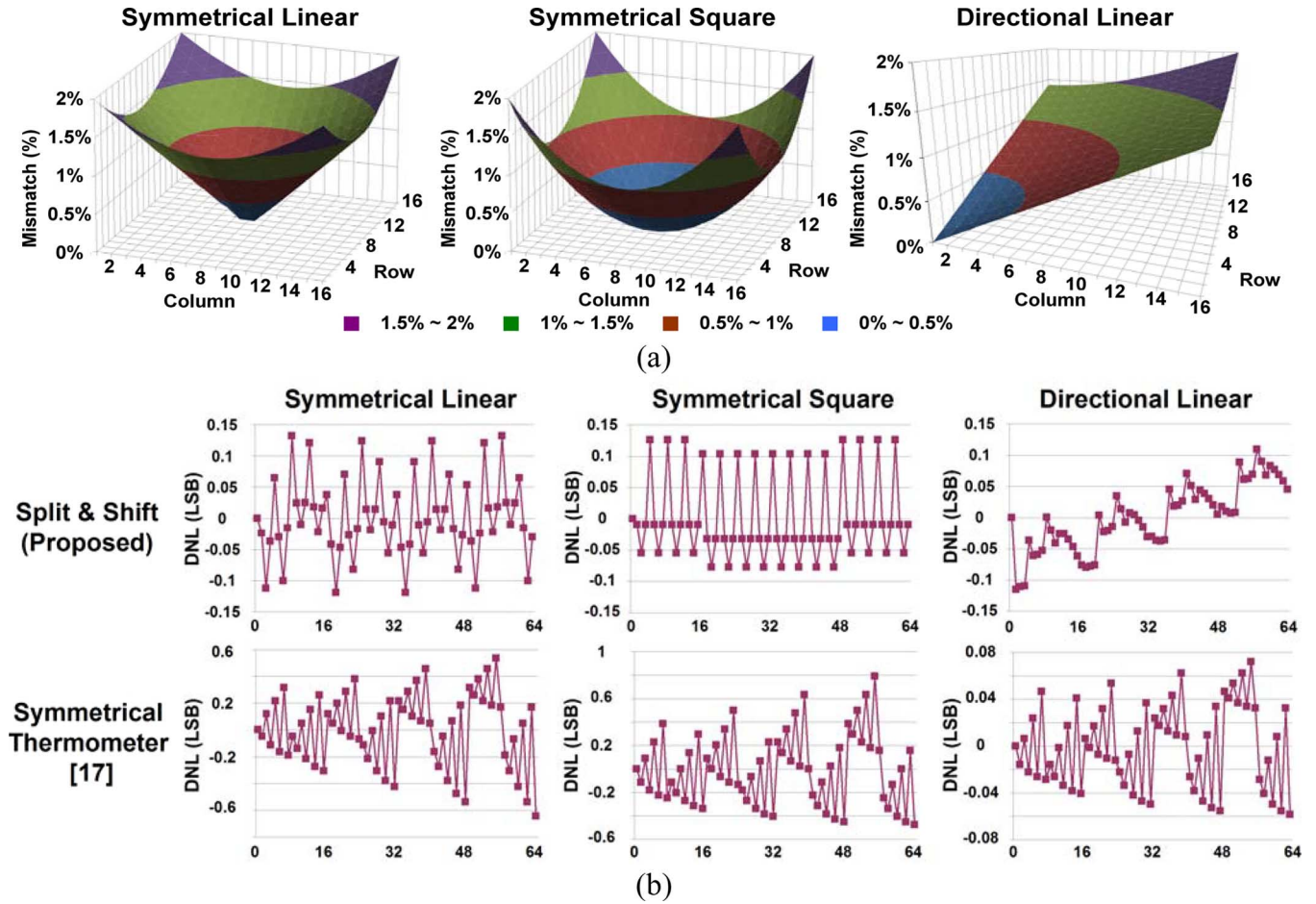
Fig. 8.　(a) Mismatch modeling. (b) Theoretical mismatch performance on current array.
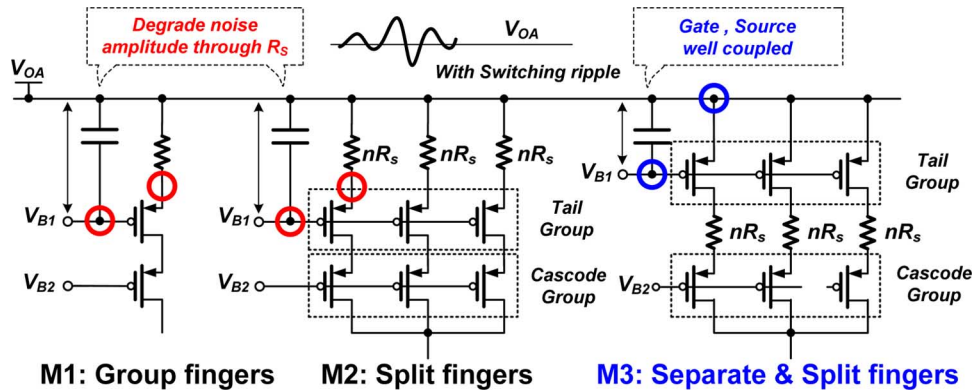

Fig. 9.　The finger-separate and split method.

be taken into consideration. In contrast to the original method M_1 which uses the group of finger, the prior method M_2 uses the splitting method to improve the current mismatching issue, while this kind of placement methods still suffers from switching noise interference due to the coupling effect on gate and source. The proposed method, M_3, which adopts the split and separate method, separates the placement of tail group and cascade group in layout. It has lower the parasitic resistance between the tail group and power supply. Meanwhile, the switching noise from the SIDO converter can be suppressed and the 12-bit DAC with SIDO converter has less impact from

switching noise effect. The 3S method achieves good matching and noise immunity performance compared with the previous methods.

IV. SIDO CONVERTER WITH DVS POWER OPTIMIZATION

A. Proposed SIDO Converter

The proposed SIDO DC-DC converter in Fig. 10 provides two well-regulated voltages to analog blocks and digital circuits separately. The embedded DVS control can accept the external control signals, V_{DVSA}, V_{DVSD}, to control the two feedback
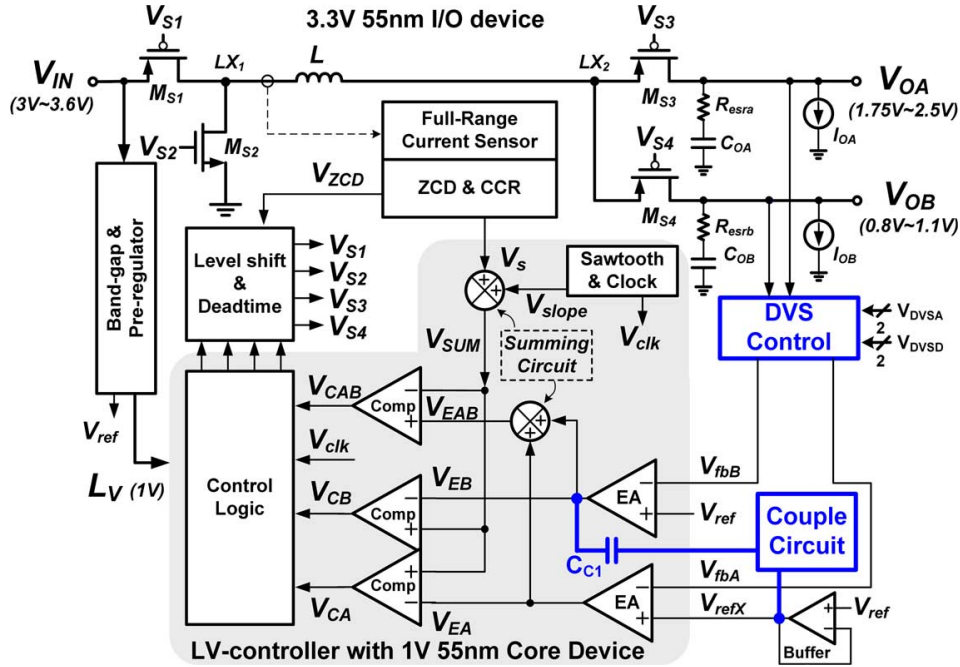
Fig. 10. The proposed SIDO converter with the couple circuit to reduce the cross-regulation for improving the SFDR of the 12-bit DAC.
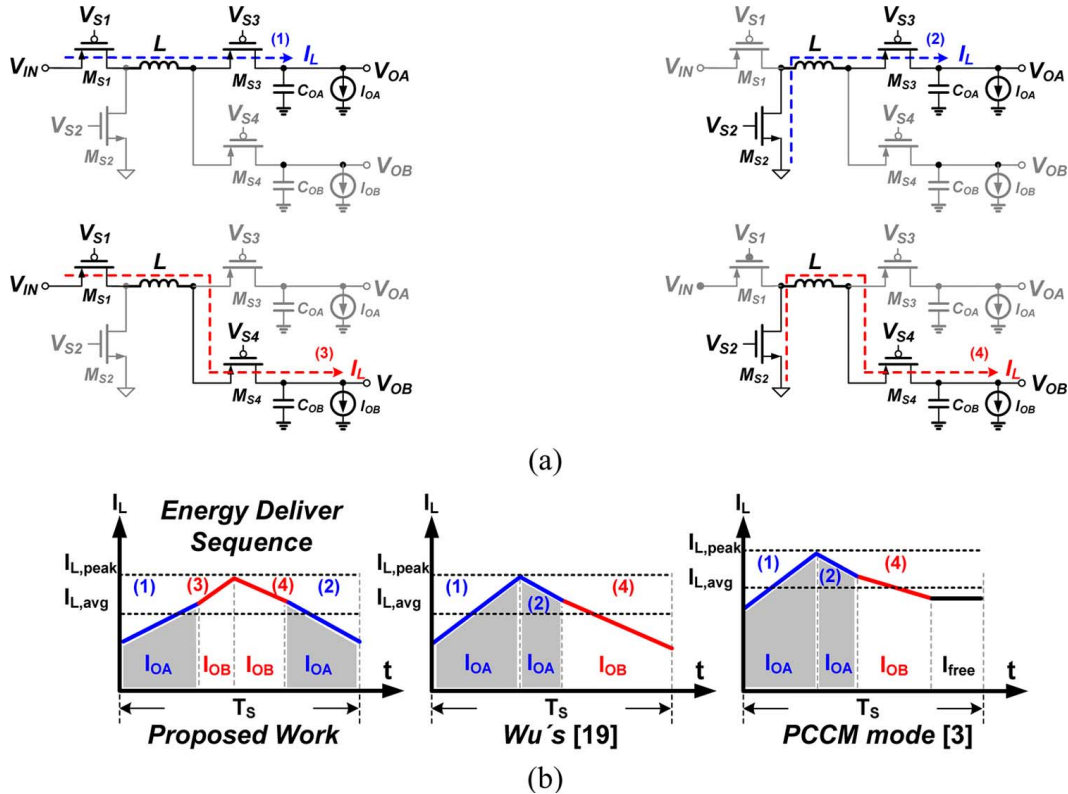

Fig. 11. (a) Energy delivering sequence of the proposed SIDO converter. (b) Various deliver sequences.

voltages, V_{fbA} and V_{fbB}. Thus, the two DVS output voltages for power optimization can be accurately decided.

Only four power switches (M_{S1}–M_{S4}) are used at the power stage which provides dual step-down outputs. The power switches, which are implemented by the thick oxide I/O devices in 55 nm CMOS technology, tolerate the voltage range

of battery-powered input up to 3.6 V. The voltage dividers are carried out by the DVS control to feed output voltage information back to the low-voltage (LV) controller for monitoring the two output loading conditions. Besides, the converter can operate both in the discontinuous conduction mode (DCM) and the continuous conduction mode (CCM) to improve the
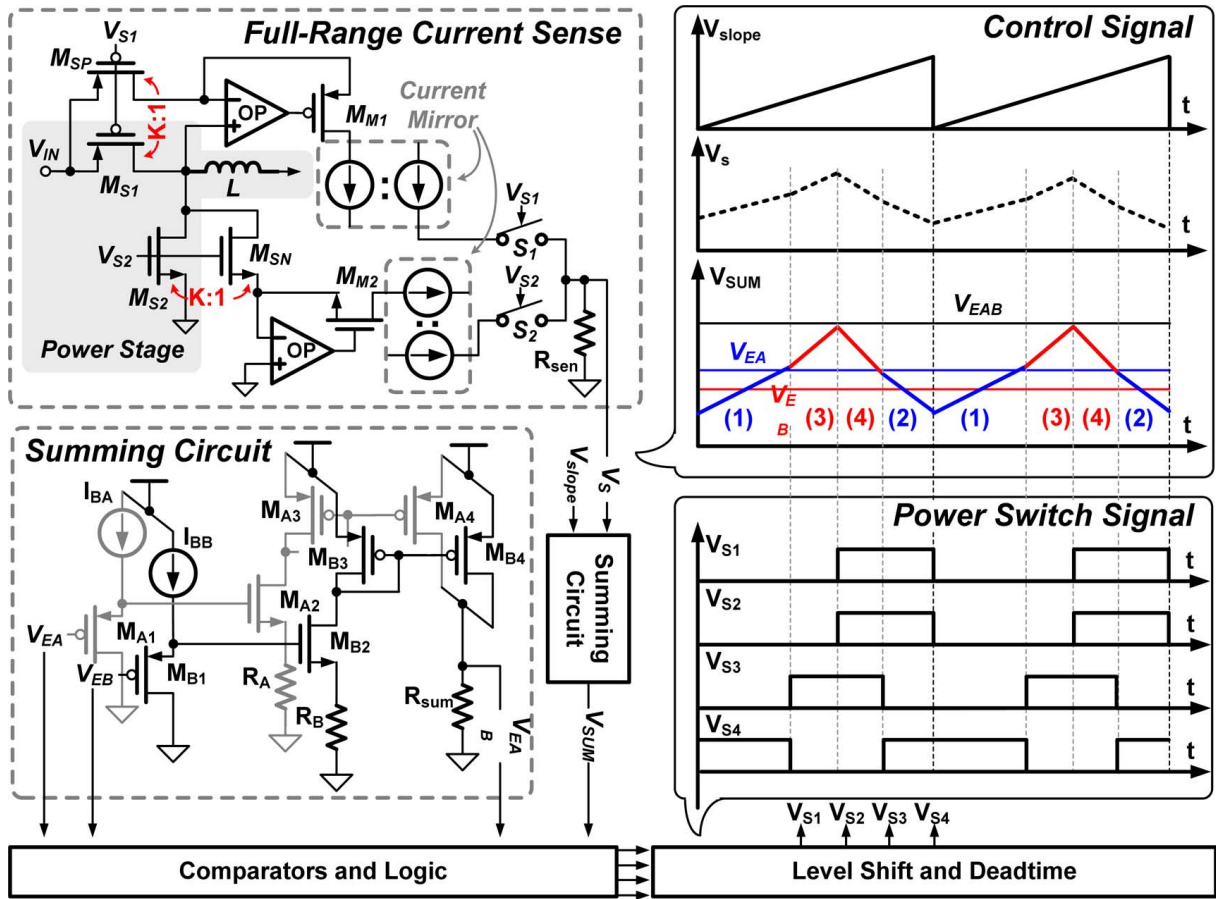
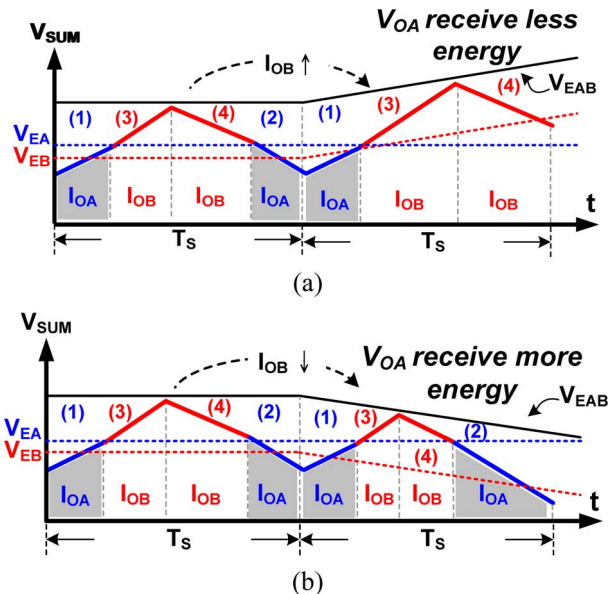Fig. 12.   The full-range current sense, summing circuit and timing diagrams.

Fig. 13.   The proposed SIDO module for suppressing the switching noise to improve the SFDR of the 12-bit DAC.

Fig. 14.   (a) Proposed couple circuit for suppressing the cross-regulation. (b) Couple effect of the V_{fbAB}.

power efficiency over a wide load range. The pre-regulator generates a 1 V supply voltage and the reference V_{ref} for the LV-controller. Hence, the power consumption from the LV-controller can be decreased. The energy deliver sequences of the dual step-down SIDO converter are shown in Fig. 11(a). In phase (1) and phase (2), the inductor is in the charging state,
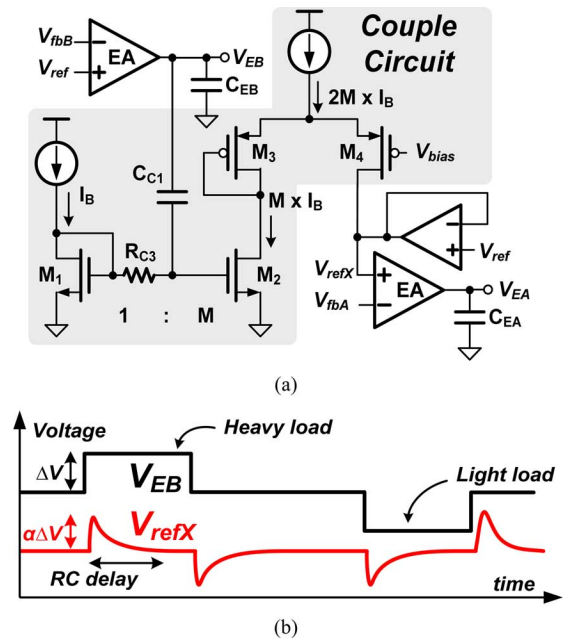
the SIDO converter delivers energy to both outputs and thus the inductor current rises. On the other hand, in phase (3) and phase (4), the inductor is in the discharging state and thus the inductor current falls. Compared to the prior arts as shown in
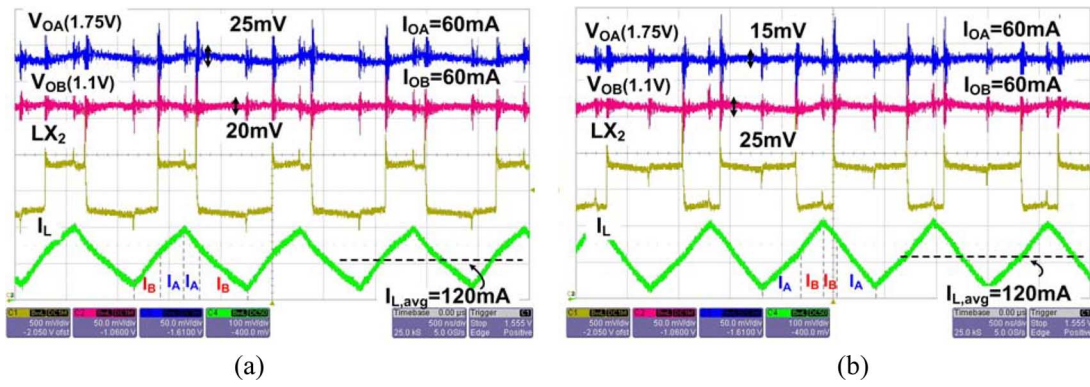
Fig. 15. The measured ripple performance under different energy delivering sequence.
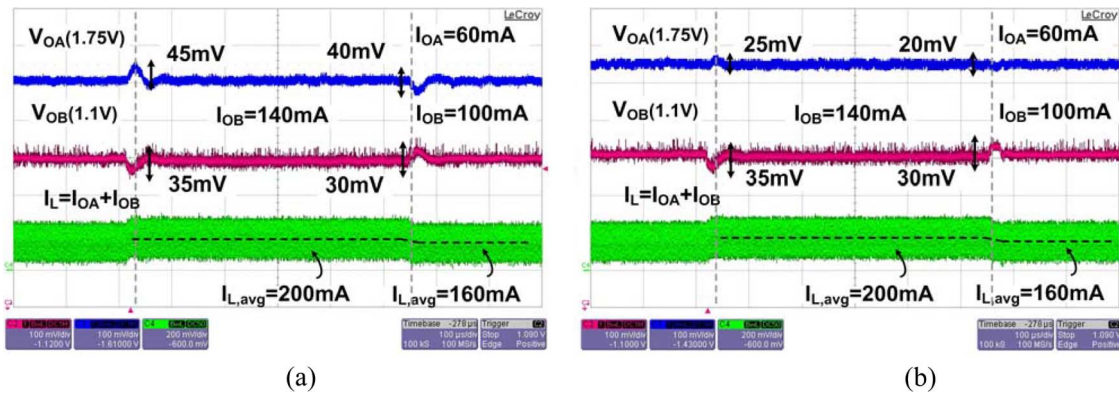

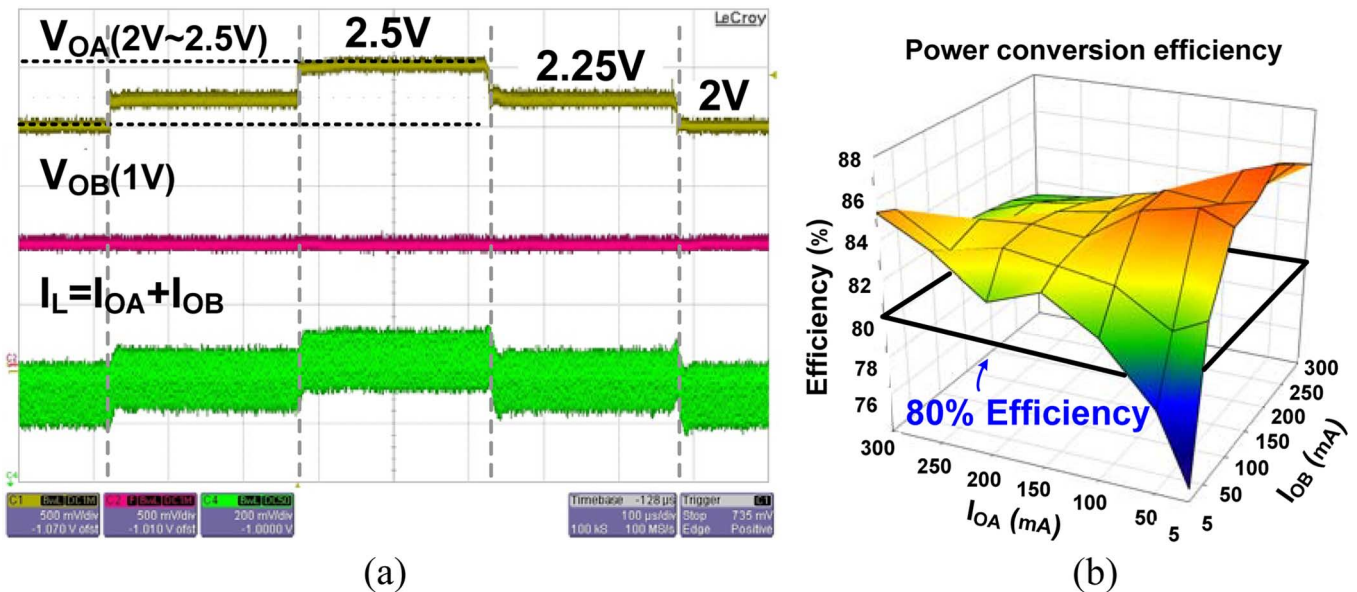Fig. 16. The measured cross regulation in transient response.

Fig. 17. (a) Measurement of the DVS function. (b) Power efficiency of the SIDO converter.

Fig. 11(b), the Wu's energy deliver sequence will limits the loading condition between the two outputs [19]. The freewheel stage in the pseudo-continuous conduction mode (PCCM) [2], [20], [21] occupies most of the switching period at light loads, and thereby resulting in low efficiency. In this work, to improve power conversion efficiency, the inductor current is effectively reduced by stacking the two inductor currents from the two outputs. Owing to the superposition, the overall inductor current is simply equal to the summation of the two outputs as shown in Fig. 11(b). The two outputs are separately charged, which means the loading condition between two loads are not limited, and the inductor current can always be kept lower than those in the prior arts with PCCM technique.

The control scheme and the detail circuits are shown in Fig. 12. The current mode control loop is composed of the current sensing circuit, the voltage feedback loop and the summing
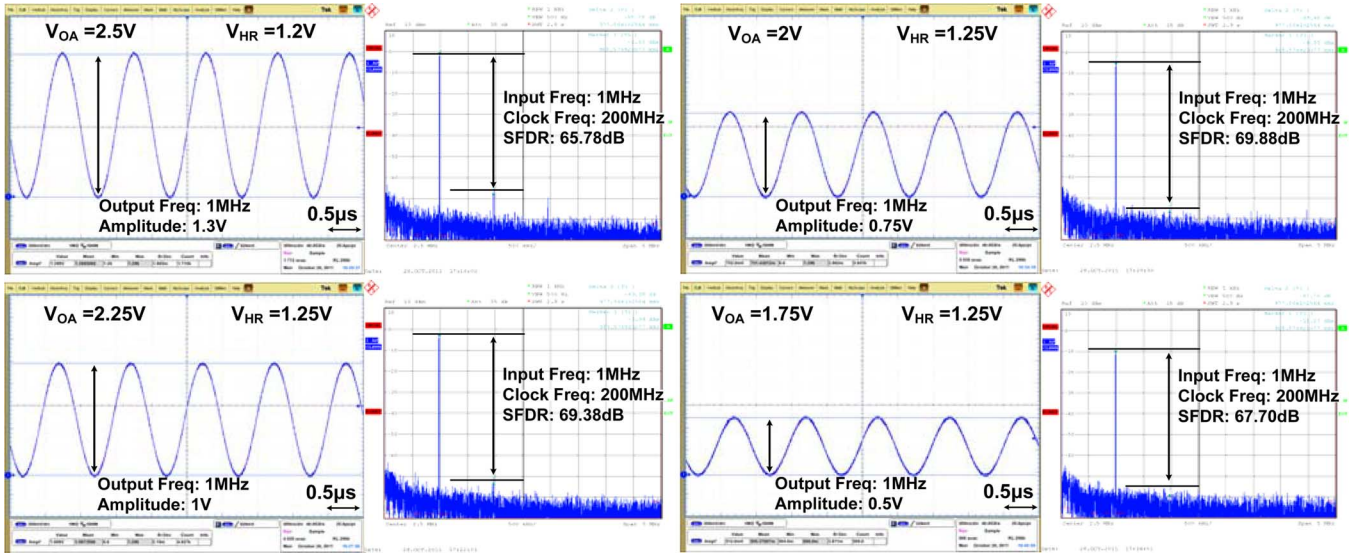
Fig. 18. Measured DAC output swing and SFDR in the DVS mode.
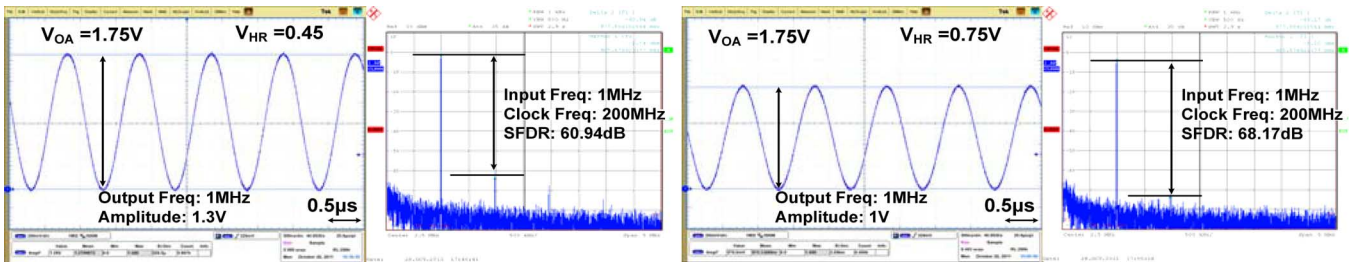
Fig. 19. Measured DAC output swing and the SFDR in the PO mode.
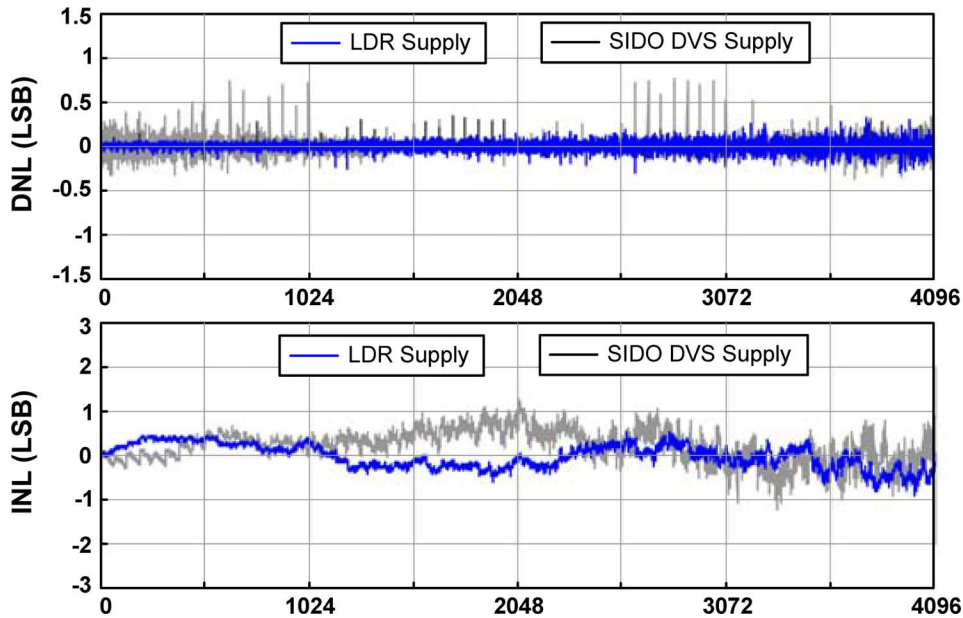
Fig. 20. INL/DNL with/without the SIDO DVS supply.

circuit. The full-range current sensor can generate the sensing signal V_S which is transformed from the inductor current in a certain ratio. The switches S_1 and S_2 will select the current signal according to the turn-on status of the power switches to achieve full-range current sense in each energy deliver path. The summing circuit will plus the V_S with the ramp signal

V_{slope}, which is used to avoid sub-harmonic oscillation, and to implement the current-mode control. The V_{EA} and the V_{EB} are the error signals feedback from the outputs of the two error amplifiers. Hence, the V_{EA} and the V_{EB} represent the requested energy from both loads. The summed up V_{EAB} represents the total energy requirements and should be compared with the

Fig. 21. Measured DAC SFDR in the STD mode.

Fig. 22. Measured DAC SFDR in the DVS mode.

V_{SUM}, which represents the energy in the inductor, to adjust the duty cycle for controlling the inductor current level. As the timing diagram depicted in Fig. 12, the energy will firstly deliver to the V_{OA}. When the V_{SUM} reaches the V_{EA}, the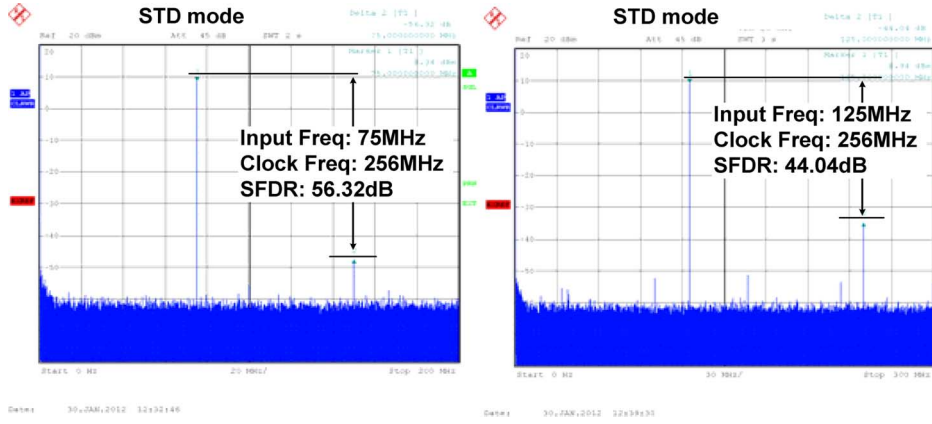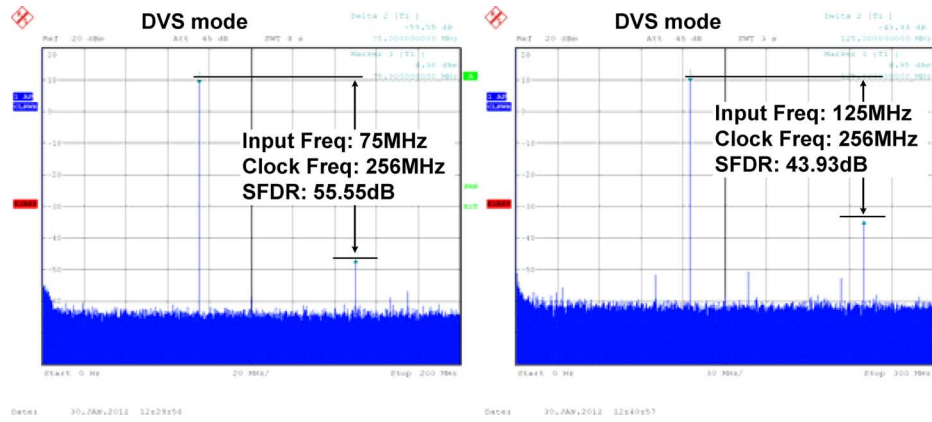 V_{OA} receives enough energy and the energy will deliver to the V_{OB} until the V_{SUM} reaches the V_{EAB}. In the DCM operation, the CMOS controlled rectifier (CCR) and the zero current detection (ZCD) circuit in Fig. 10 control power MOSFETs to avoid reverse inductor current for high power conversion efficiency.

Furthermore, the energy delivery paths must be well arranged [2], [22], [23] and the cross-regulation needs to be carefully considered at the same time. Cross-regulation is a well-known issue on the SIDO converters [19]–[25] and may take place in either transient or steady-state periods due to one-inductor utilization. To improve output quality on analog power supply, the SIDO converter operates in the analog ripple optimization condition. That is, the SIDO converter will deliver the energy to analog circuits with high priority regardless the loading condition at the other output. Thus the voltage ripple on the V_{OA} can be minimized through suppressing the influence of power supply noise and optimizing the steady-state cross regulation.

Transient cross regulation was resulted from the energy delivery scheme during the load transient response. If there is a sudden load change on the output V_{OB} as shown in Fig. 13(a), the V_{OB} needs more energy to cause the increase of the V_{EB}. As a result, the summed-up error signal V_{EAB} will rise to increase the inductor current level. While the loading at the V_{OA} remains

the same, the energy delivered to V_{OA} will decrease due to the change of the sensing signal V_S. Therefore, the voltage on V_{OA} will drop since less energy has been delivered to V_{OA}. On the contrary, the V_{OA} voltage will rise because receives more energy as shown in Fig. 13(b).

Furthermore, the proposed SIDO converter includes the couple circuit to suppress the cross-regulation. In other words, the instant disturbance caused by one of the two outputs can be coupled to control the energy for minimizing the cross-regulation. When the inductor current is firstly delivered to the analog output V_{OA}, a sudden load change on the V_{OB} will cause the V_{OA} to either drop or rise according to the polarity of load change [25]. The couple circuit as shown in Fig. 14(a) can couple the error signal generated from the error amplifier (EA) of the V_{OB}. Through the C_{C3} and the R_{C3}, the coupled signal will induce the discharging/charging effect and finely adjust the buffered reference voltage V_{refX}. The error signal V_{EA} will be influenced and change the duty cycle of the V_{OA} as shown in Fig. 14(b) to reduce the transient cross regulation of the V_{OA}. In other words, the cross-regulation can be effectively reduced.

B. DVS Power Optimization

For digital circuit, the supply voltage will influence the speed of the logic circuit. Thus the DVS function can adjust the supply voltage according to the operation frequency and achieve an optimized performance and power consumption. For analog circuit, voltage headroom and the bias voltage will be seriously

TABLE I
DAC OPERATION STATUS AND PERFORMANCE

Mode	Supply	Output Swing	SFDR	DAC Power Efficiency	Total Power Efficiency
STD1.3	2.5V LDR	1.3V	69.1	52%	36.1%
STD 1	2.5V LDR	1V	72.29	40%	27.7%
STD 0.75	2.5V LDR	0.75V	72.57	30%	20.8%
STD 0.5	2.5V LDR	0.5V	71.1	20%	13.8%
DVS 1.3	2.5V SIDO	1.3V	65.78	52%	44.7%
DVS 1	2.25V SIDO	1V	69.38	44.4%	38.2%
DVS 0.75	2V SIDO	0.75V	69.88	37.5%	32.3%
DVS 0.5	1.75V SIDO	0.5V	67.70	28.5%	24.5%
PO 1.3	1.75V SIDO	1.3V	60.94	74.5%	64.1%
PO 1	1.75V SIDO	1V	68.17	57.1%	49.1%
PO 0.75	1.75V SIDO	0.75	68.4	42.8%	36.8%
PO 0.5	1.75V SIDO	0.5	65.1	28.5%	24.5%
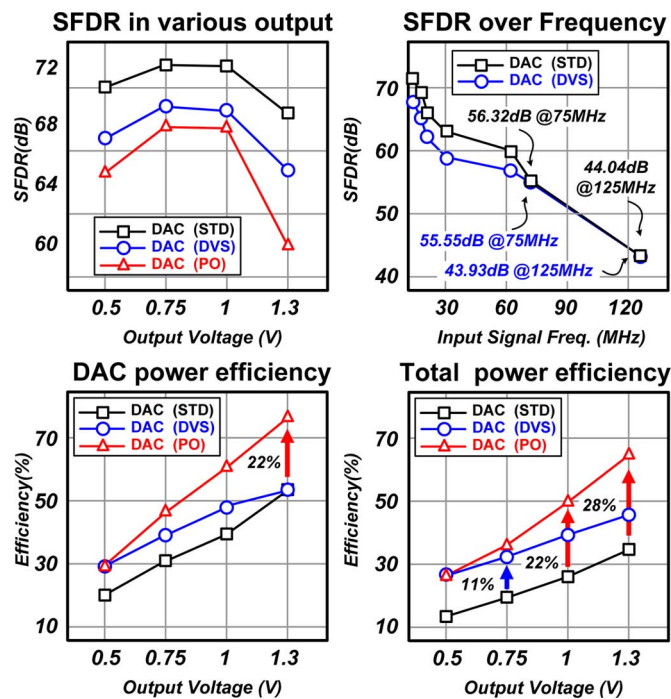
Fig. 23. SFDR and power efficiency in different modes.

Fig. 24. Chip micrograph.

TABLE II
PERFORMANCE SUMMARY

Technology	TSMC 55nm CMOS process
SIDO module with DVS	
Input Voltage	3V~3.6V
Inductor (off-chip)	4.7μH
Capacitor (off-chip)	4.7μF
Switching Frequency	1MHz
Output Voltage 1 (V_{OA})	1.75~2.5V
Output Voltage 2 (V_{OB})	0.8~1.1V
Maximum Load Current	300mA
Line Regulation (V_{OA})	18.75mV/V @ Load=200mA
Load Regulation (V_{OA})	30mV/A @ V_{IN}=3.3V
Output Ripple	<50mV
Power Efficiency	86.2%
Die Size	1500μm x 650μm
DAC module	
Input Voltage	1.75~3.3Analog 1V Digital
Output Dynamic Range	0.5V~1.3V
SFDR	72.29dB @1V output LDR
F_{clock}	250MHz
INL(max) / (min)	0.95/-1
DNL(max) / (min)	0.4 / -0.37
Die Size	300μm x 1200μm (3 channels)

affected by the supply voltage. The voltage headroom influences the resolution and linearity of the DAC [7], [8] and also dominates the power consumption of the whole system. Due to the various output swing and resolution requirements from different video formats, the video DAC has different output statuses. To provide various output swing and preserve the same signal quality of the analog blocks, the analog DVS control is introduced. Different display formats have to be defined by video processing unit or digital signal processor (DSP), and different supply voltage will be generated through SIDO converter once the DVS control circuits received the display information.

The DVS function is designed to save energy but also meet the requirement of the voltage headroom which guarantees the performance of the analog circuits. According to different output demands from 0.5 V to 1.3 V, the DVS controlled SIDO converter can provide appropriate supply voltage. For the bias and deep-saturation requirement of the cascode current cell, voltage headroom of 1.2 V is large enough to ensure good
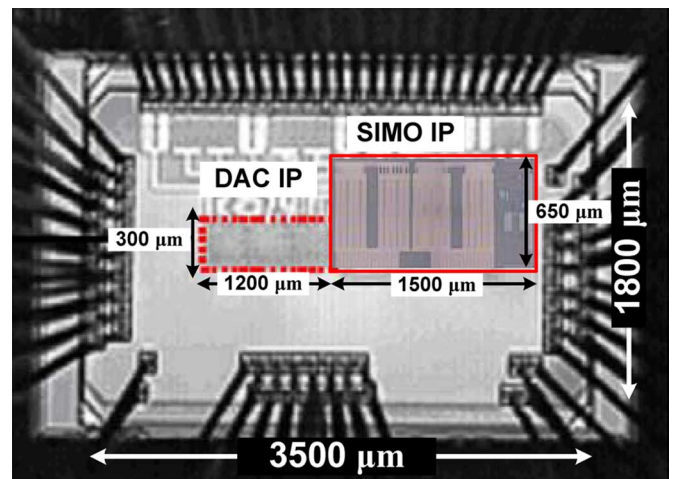
performance of the current cell. Thus the supply voltage is set to be 1.2 V higher than the voltage swing to minimize the unnecessary power loss caused by extra voltage headroom. The DVS function provides two different operation modes

TABLE III
COMPARISONS OF OTHER DAC SYSTEMS

	This work	TVLSI 2011 [26]	JSSC 2007 [27]	JSSC 2004 [28]
Technology	55 nm CMOS	90 nm CMOS	0.18μm	0.18μm
Resolution	12 bit	12 bit	14 bit	12 bit
Sampling Rate	250 MHz	400MHz	200MHz	320MHz
INL	1LSB LDR 1.3LSB SIDO	0.4LSB	1.37LSB	0.4LSB
DNL	0.4LSB LDR 0.78LSB SIDO	0.3LSB	0.76LSB	0.3LSB
Max. SFDR	72.29dB LDR 69.88dB SIDO	73.6dB	81.5dB	95dB
Full Scale Current	34.6mA	26.7mA	16mA	21mA
Full Scale Voltage Swing	1.3V	1V	N/A	1V
Embedded Power module	Yes	No	No	No
DAC Supply Voltage	Digital 1V Analog 2.5V	Digital 1.2V Analog 2.5V	Digital 1.8V Analog 1.8V	Digital 1.8V Analog 3.3V
Power Dissipation	95mW	92mW	130mW	82mW
Total Power Efficiency	38.2 % @ DVS Output = 1V	< 27.7%	<27.7%	< 27.7%
Active Area	1-chanel DAC 0.12mm^2 SIDO 0.975mm^2	0.18mm^2	3mm^2	0.44mm^2
*FOM$_{DAC}$	10046	8005	280	2936

● 1V output under 3.6V battery voltage with LDR as system power supply

$$^* FOM_{DAC} = \frac{N_{bit} \times F_{Sampling} \times P_{efficiency}}{Power \times Area_{DAC}} \text{ where } Power(mW), F_{Sampling}(MHz), Area(mm^2), P_{efficiency}(\%)$$

according to the video signal format. For low resolution requirements such as RGB outputs, the DVS module will enter the PO mode, which will keep the V_{OA} at the lowest output voltage of 1.75 V. Because the cascode current mirror, bandgap reference and OPAMP in the DAC circuits are designed by 2.5 V I/O devices, the supply voltage cannot be lower than 1.75 V to guarantee the correct operation of the DAC.

V. EXPERIMENTAL RESULTS

The proposed 12-bit DAC supplied by the SIDO converter was fabricated in 55 nm CMOS process [29]. The SIDO module operates with an inductor of 4.7 μH and two output capacitors of 4.7 μF at 1 MHz switching frequency. The output ripple is less than 50 mV and the quiescent power of SIDO module controller is 120 μW. The 12-bit DAC operates at 250 MHz clock frequency, with the input signal at 1 MHz.

Fig. 15(a) shows the energy deliver sequence of the SIDO converter in the analog optimized condition and Fig. 15(b) shows the contrary deliver sequence at the same loading. The ripple in analog supply V_{OA} can be reduced from 25 mV to 15 mV, which optimizes the steady state cross regulation. Fig. 16(a) shows the transient cross regulation without the couple circuit. As the couple circuit starts operation, a better transient cross regulation performance can be achieved as in Fig. 16(b). Through the analog optimized delivering path and couple circuit, the switching ripple and the cross regulation in both steady state and transient can be minimized. The measured DVS supply voltage is shown in Fig. 17(a). The power efficiency of the SIDO converter is shown in Fig. 17(b); the maximum power efficiency is 86%. Through the high efficiency

of SIDO converter with DVS control, the power efficiency can be optimized and extend the battery life of a portable device.

The SFDR of the 12-bit DAC and the power efficiency of the SIDO module via different full-scale output swing and supply voltage are shown in Fig. 18. The maximum SFDR is 69.88 dB at 1 V output. Here, a SFDR performance measurement result of the PO mode is provided for further power reduction but with the penalty of degrading some resolution as shown in Fig. 19. For large output swing up to 1.3 V, the headroom is not sufficiently large. Thus the output waveform suffers from some distortion resulting in degradation in the SFDR performance. Fig. 20 shows the INL and DNL performance with/without the SIDO DVS power supply. The switching noise of SIDO converter slightly degrades the DNL performance from 0.4 LSB to 0.78 LSB and the INL performance from 1 LSB to 1.3 LSB. The performance of DNL is smaller than 1 LSB. It demonstrates the correctness of intrinsic 12-bit video DAC with the DVS technique and supplied by the SIDO converter. The SFDR of the DAC in STD mode and DVS mode under 75 MHz and 125 MHz are shown in Figs. 21 and 22, respectively.

The mode selection and the performance overview of the video DAC with/without SIDO module are in Fig. 23. The details are also listed in Table I. The 12-bit video DAC supplied by LDR is called the standard (STD) condition. When supplied by SIDO converter, it presents the performance of both the DVS and the PO mode. We define the DAC power efficiency as the DAC output swing voltage divided by supply voltage, which represents the power wasting on the headroom requirement in analog circuits. The total power efficiency is defined as the DAC power efficiency multiplied by the power module's efficiency. We assume a battery with 3.6 V output voltage as the system

power supply in order to compare the differences between traditional LDR and the proposed SIDO converter, as shown in Table I. It is observed that with the DVS control, the power efficiency can be promoted. In the PO mode, it also provides at least 60 dB of SFDR, which is capable for the traditional DVD quality video. Comparing with the tradition LDR solution, the DAC supplied by the SIDO converter can save up to 11.5% and 28% of total power consumption in the DVS mode and the PO mode respectively. The chip micrograph is shown in Fig. 24. The total occupied silicon area is 1.335 mm^2 (excluding I/O cells and bond pads). The detailed design specifications of both the SIDO converter and the video DAC are listed in Table II. Comparisons with other DAC methodologies are shown in Table III.

VI. Conclusion

In this paper, a 12-bit video DAC and the power supply SIDO converter module are proposed. The test chip was fabricated in 55 nm CMOS process. The SIDO DC-DC converter generates two high efficiency power outputs for different circuit blocks with only one power module which saves the PCB area and the quantity of external component. At 1 MHz input, without linear regulator, SIDO DC-DC converter with dual-DVS technique improves the DAC's total power efficiency up 11.5% and achieves maximum 69.88 dB SFDR in the DVS mode. The PO mode provides a solution for low power operation and still maintains the acceptable SFDR up to 60.94 dB and 68.4 dB at 1.3 V and 0.75 V output swing respectively. Through the measurement result, it is clear that the 3S method exhibits not only a better performance in matching issues but also in the noise reduction theme. This combination is an area and energy efficient solution and will be valuable for many video applications such as the driver or controller of a monitor screen, which also includes digital control circuits, DAC and I/O circuits.

Acknowledgment

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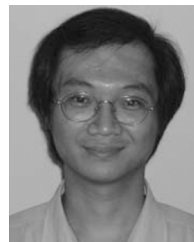
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