High Definition Image Pre-Processing System for Multi-Stripe Satellites' Image Sensors

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***Abstract*— High-resolution image sensors play an important role in today's satellites' remote sensing applications. This paper presents an image recombination and processing system for one-dimensional multi-strip complementary metal-oxide semiconductor image sensors (CISs.) The proposed system takes advantage of the satellites' linear moving property to control the exposure time of CIS and provides the real-time ability to generate 11 200 × N high-resolution images for satellites' remote sensing. Using hardware accelerators coupled with versatile microprocessors, the architecture is able to offer processing capability as well as long-term maintainability for space-borne platforms. The details of hardware design to meet real-time requirement are presented. The prototype, which contains four strip CISs and field programmable gate array-based prototyping, was implemented to verify functionality and capability of real-time image acquisition and combination. The implementation results show that it is feasible to integrate the proposed system into a single chip.**

***Index Terms*— Complementary metal-oxide semiconductor (CMOS) image sensor, field programmable gate array (FPGA), microprocessor, remote sensing, space-borne platform.**

I. Introduction

IMAGE sensors play an important role in today's satellites' remote sensing applications, such as forest monitoring, disaster area evaluations, environment monitoring, climate monitoring, etc. Traditionally, charge-coupled devices (CCDs) are adopted in satellite's applications. Recently, the improvement of CMOS image sensors (CISs) have been used in space applications [1], owing to the lower cost, lower power consumption and compatibility to nowadays well-developed CMOS integrated circuit compared to CCD's technology. Several satellites have adopted both one-dimensional and two-dimensional CISs as their components. Satellites' linear moving property [2], [3] to control the exposure time of line CISs provide real-time ability to generate 11,200 × N high-resolution image for satellites' remote sensing.

Line sensor array possessing high-resolution as well as high line-rate properties imposes difficulties on CMOS semiconductor fabrication. Recently, wafer-level stitching technique has been developed for high-resolution large-scale image sensors; however, it highly relied on foundries to improve yield [4]. Therefore, multiple CIS dies aligned in single package to form a high-resolution image are proposed in this study. In order to avoid the spatial discontinuity, these strip CISs are arranged in an interlaced and overlapped fashion. Thus, multi-pixel vertical gaps and horizontal overlaps are between top line sensors and bottom ones. A real-time calibration scheme is required for satellite image remote sensing.

The proposed architecture of the real-time image pre-processing system for satellites' remote sensing is shown in Fig. 1. The system integrated sixteen strip CISs [5], four image combiner and acquisition interfaces (ICAIs) [6], an I^{2}C controller, two microprocessors and external memories

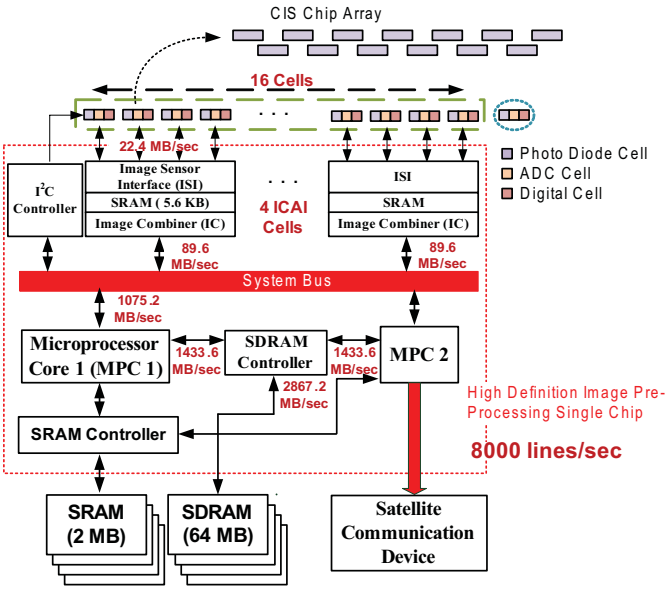

Fig. 1. Architecture of the proposed real-time image pre-processing system for satellites' remote sensing.

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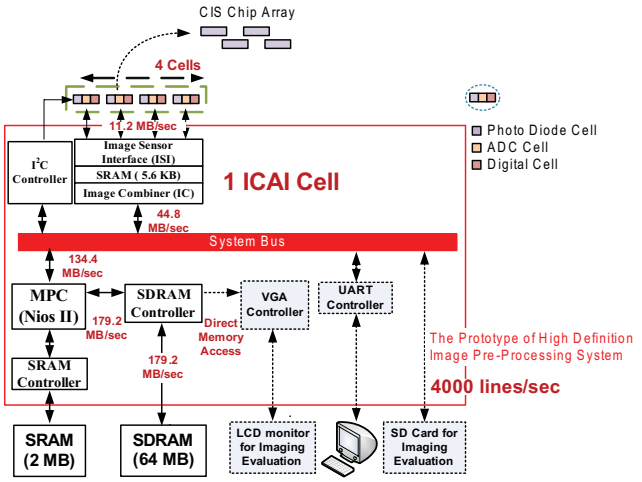


Fig. 2. Architecture of the system prototype for satellites' remote sensing.

to build a high-resolution multiple-aspect two-dimensional images. ICAI cooperated with microprocessors are proposed to calibrate gaps and overlaps in real-time. Multiple static random access memories (SRAMs) and synchronous dynamic random access memories (SDRAMs) are utilized to improve reliability. Except for CISs and external memories, the reset of system is supposed to be integrated in a single chip because of high data bandwidth demand for image throughput. Based on the above setup, the proposed system provides the real-time capability to acquire images for the satellites' remote sensing applications.

In this paper, a prototype of real-time image pre-processing system for satellites' remote sensing is implemented to verify functionality and evaluate real-time performance. The architecture of the prototype is shown in Fig. 2. The prototype is composed of four strip CISs, an ICAI, a custom Nios II/fast processor system [7], an SDRAM and a PC performing satellite server. The main difference between the prototype and the final system is data bandwidth demand. The final system will demand eight times larger throughput than the prototype; however, the bandwidth demand can be achieved by the proposed single chip.

The rest of this paper is organized as following. In Section II, the system architecture and performance evaluation of the prototype are described. Section III discusses hardware designs. In Section IV, implementation result is presented. Following is the conclusions in this paper (Section V.)

II. Architecture and Performance Evaluation of the Prototype

The system prototype is shown in Fig. 2. In the hardware, it consists of four strip CISs, a custom Nios processor system, which is the proposed chip prototype, and personal computer (PC.) The Nios processor family [7] is 32-bit embedded-processor architecture designed specifically for the field-programmable gate array (FPGA.) The simplicity, flexibility and fixed instruction format of RISC [8] provides implementation feasibility for high processing performance. Nios II/fast processor core is adopted in the prototype. With performance over 300 DMIPS (Dhrystones 2.1 benchmark), it is optimal for applications with large amounts of code and data. In our Nios processor system [9], [10], it implements typical bus architecture. All the transfers among peripherals (slaves) and Nios processor (master) must be passed through system bus. SRAM and SDRAM are adopted as instruction and data memory, respectively. Two additional features, video graphics array (VGA) display and secure digital (SD) card storage are applied to verify sensor performance, which will not be in the final system. To cooperate with designed hardware, functions including sensor gaps calibration and image stream out are implemented. A host computer links to the image pre-processing system via universal asynchronous receiver/transmitter (UART). In this study, the host computer plays the role of satellite control center and the image source. The satellites' linear moving image and on-the-fly configuration are provided by a custom integrated graphic user interface (GUI) running on the host computer.

In the system prototype, only four strip CISs are adopted, which contains 2,800 pixels. The total data bandwidth of microprocessor is 400 MB/sec at 100 MHz operating rate. The front-end image bandwidth is evaluated about 11.2 MB/sec at exposure time of 250 microseconds (four sensors generate 4,000 $\times$ 2,800 bytes per second, 8 bits per pixel.) Because the 8-bit pixel is required to align 32-bit data stream, 44.8 MB/sec bandwidth is consumed for bus transfer. MPC require three clock to access one pixel stream from ICAI and four clocks to access SDRAM, therefore, 134.4 MB/sec and 179.2 MB/sec is required for ICAI and SDRAM access, respectively. Therefore, a total of 313.6 MB/sec data bandwidth is required on MPC. That is feasible in 90-nm FPGA-based platform at 100 MHz clock rate; however, if sixteen strip CISs are applied in 8000 line rate, the data bandwidth demand on MPC will become a critical problem. In this study, the pre-processing architecture of line scan image sensor based on microprocessors with hardware accelerator (ICAI) is utilized. Although application-specific integrated circuit (ASIC) can provide highly processing capability and be efficient on data transfer, it is lack of flexibility. The specific hardware with a versatile microprocessor provides processing capability and flexibility. Furthermore, online configuration and programmability features of microprocessor provide long-term maintainability for space-borne application. Therefore, microprocessors-based architecture is utilized in this research.

In the final system, sixteen strip CISs provide 11,200 pixels. The front-end image bandwidth as well as on-chip system bus is evaluated about 358.4 MB/sec at exposure time of 125 microseconds (sixteen sensors generate 8,000 $\times$ 11,200 bytes per second.) One microprocessor does the basic pre-processing on image line by line and store results into SDRAM. The other microprocessor takes charge of block processing, such as lossless image compression, on combined image in SDRAM. The most critical bandwidth demand locates on SDRAM, which is about 2870 MB/sec. The data bandwidth can be readily achieved if the system runs at 800 MHz in nowadays chip implementation [11], [12].

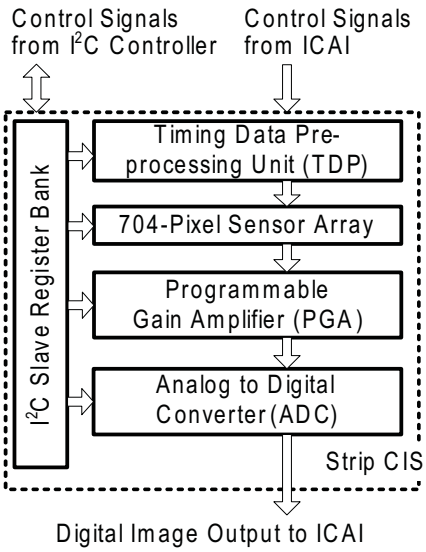


Fig. 3. Block diagram of the strip CIS.

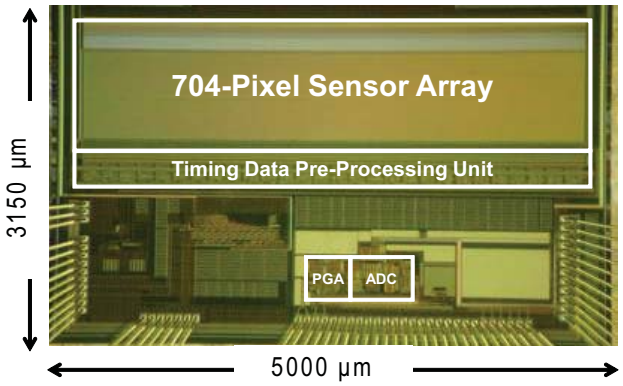


Fig. 4. Die photograph of the CIS for satellites' remote sensing.

III. Hardware Designs

In addition to the system architecture, dedicated hardware components are also key factors in real-time performance. In this section, hardware designs to meet real-time requirements for satellites' remote sensing are presented.

A. Satellites' Image Sensors

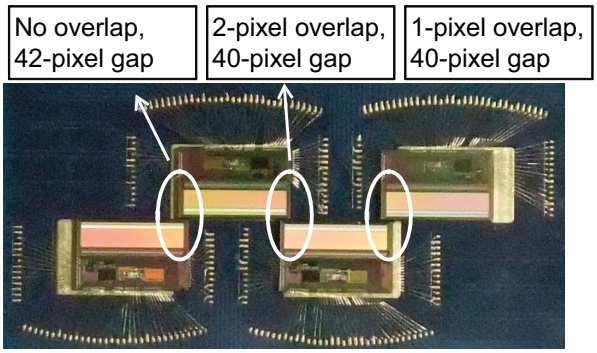
The architecture of strip CIS is shown in Fig. 3. The timing data pre-processing (TDP) unit is designed to control photodiode array to store image and output data serially. Four excess photodiodes are designed for die overlapping. The analog image signal is fed into a power-efficient programmable gain amplifier (PGA) for common-mode voltage level shifting and signal amplifying. The analog output of the PGA is then digitized by a 10-bit cyclic analog-to-digital converter (ADC) [13]. All configurations of circuit blocks are stored in an I^2C slave register bank. A one-shot power-on configuration is processed by the host.

The strip CIS has been fabricated with TSMC 0.18 μm triple-well CIS 1P3M technology. In order to reduce the light reflection and interference, only three metal layers were used in the whole chip. The die photograph is shown in Fig. 4.

TABLE I
Specification of the Satellites' Image Sensor

Technology	TSMC 0.18 mm 1P3M CMOS Image Sensor Process
Total Sensing Number (4 dies)	2,800
Total Sensing Number (1 die)	704
Resolution per Pixel	10 bits
Pixel Size	6.5μm × 6.5 μm
Saturation Output Voltage	1.312 V
Responsibility	3.64 V/Lux-s
Line Rate (Frame Rate)	8000 lines/s
Integration Time	125 μs
Fix Pattern Noise	(+2.73% / −2.7%)

(a)



(b)

Fig. 5. Photograph of four strip CISs. (a) Wire bond on PGA 370 package. (b) Different amount of vertical gaps and horizontal overlaps among sensors.

The sensor array per die has 704 pixel cells with a pixel size of 6.5 × 6.5 μm^2. The responsibility of sensor is 3.64 V/Lux.s; the fix pattern noise (FPN) ranged from +2.73% to −2.7%. The saturation output voltage of pixel front-end is 1.312V with 3.3V supply operation. The line rate and the required integration time are 8000 lines/s and 125 μs, respectively. The specification of the sensor is listed in Table I.

In order to evaluate the functionality, four strip CISs are bonded on PGA 370 package, which is shown in Fig. 5. The system package is fabricated by Integrated Service Technology, Inc. (website: http://www.isti.com.tw). One line is composed of 2,800 pixels (The resolution range of one line is 2,800 to 2,816 pixels depending on the assembling variation; 2,800 is the minimum guarantee value.) The interlaced placement is proposed to avoid the spatial discontinuity. Top strips

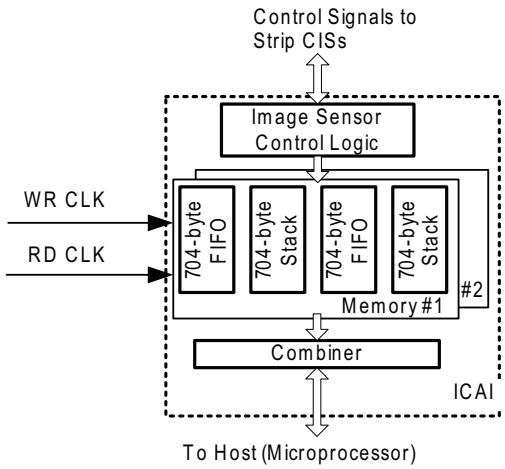


Fig. 6. Block diagram of the proposed ICAI.

CISs are placed in reverse order and closed to bottom ones to minimize the vertical gaps. Due to the alignment variation, there are different amount of vertical gaps and horizontal overlaps among sensors, which is shown in Fig. 5(b).

The proposed ICAI consists of three blocks–Dimage sensor control logic, memory blocks and combiner. The architecture of the proposed ICAI is shown in Fig. 6. Exposure time and other sensor configurations are sent to image sensor control logic from the host. Image sensor control logic takes charge of real-time acquisition and horizontal overlaps calibration. Acquired images are stored into first-in-first-out (FIFO) memory and stack, which are components in memory blocks, but overlap pixels are discarded. The last pixel is read out first without any computation in stacks so that's the most efficient way to reverse the images from top strip CISs. The write clock, WR CLK, of FIFOs and stacks is the same rate as image sensor's pixel rate. The read clock, RD CLK, of FIFOs and stacks is the same rate as microcontroller. Two memory blocks construct the double-buffering architecture [14]. At any one time, one memory block is actively being read out by the host, while the other block is being written acquired images from strip CISs. When drawing is complete, the roles of the two are switched with a few of switching overhead. Therefore, ICAI can continuously acquire and combine images. The processing capability of the proposed ICAI is 8,000 lines per second while operating at 32 MHz.

The space and time relationship of active pixels is illustrated in Fig. 7. Note that the reorder pixel sequence and the overlap elimination are accomplished by ICAI. The horizontal overlaps between CIS_K to CIS_{K+1}, are denoted as OV_K, where K is CIS index. Because CIS_4 is the last sensor in the prototype, OV_4 is 1. The pixel index after calibration is denoted as C_K, which can be defined as

$$
\begin{aligned}
&if(K\ is\ odd)\\
&\quad C_K = last\ pixel\ index\ in\ each\ sensor - OV_K\\
&else\\
&\quad C_K = OV_K
\end{aligned}
\tag{1}
$$

where the last pixel index in each sensor is 704. Because OV_K is known after assembling, C_K can be evaluated once while the system power on. Thus, continuous overlap elimination can be achieved.

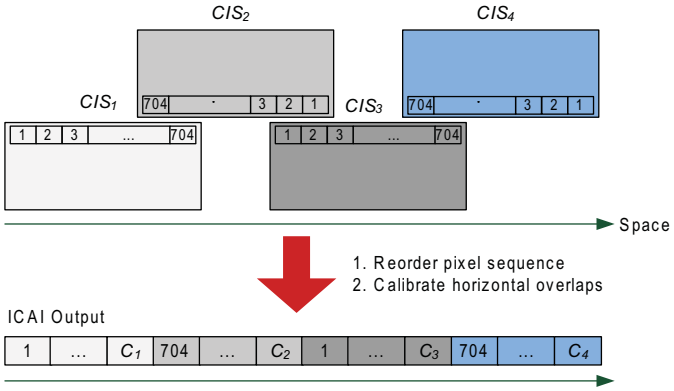


Fig. 7. Concept of pixel sequence reorder and horizontal overlaps elimination processed by ICAI.

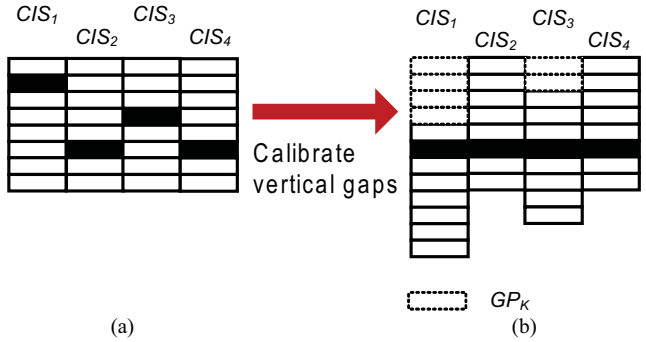


Fig. 8. Memory allocation of images. (a) Without any calibration. (b) Images are written into memory in an interleaved fashion.

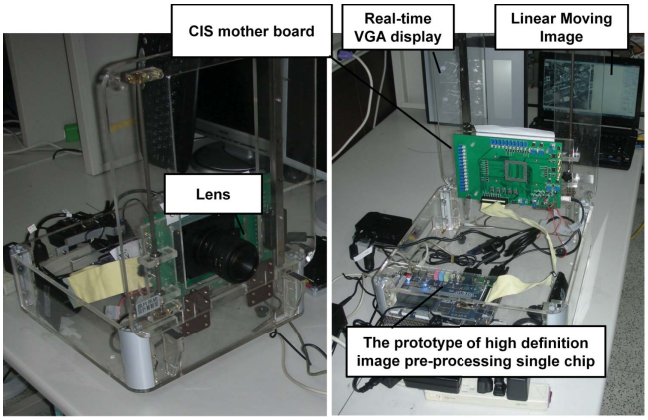


Fig. 9. Setup overview of the proposed system prototype.

B. Microprocessor

The microprocessor takes in charge of sensor gaps calibration and image stream out. If one line acquisition is complete, the microprocessor will be notified to read out images from ICAI. Readout of images will be written into external SDRAM in an interleaved fashion to calibrate vertical gap. The concept is shown in Fig. 8. If no calibration is applied, a straight line captured by the strip CISs will become

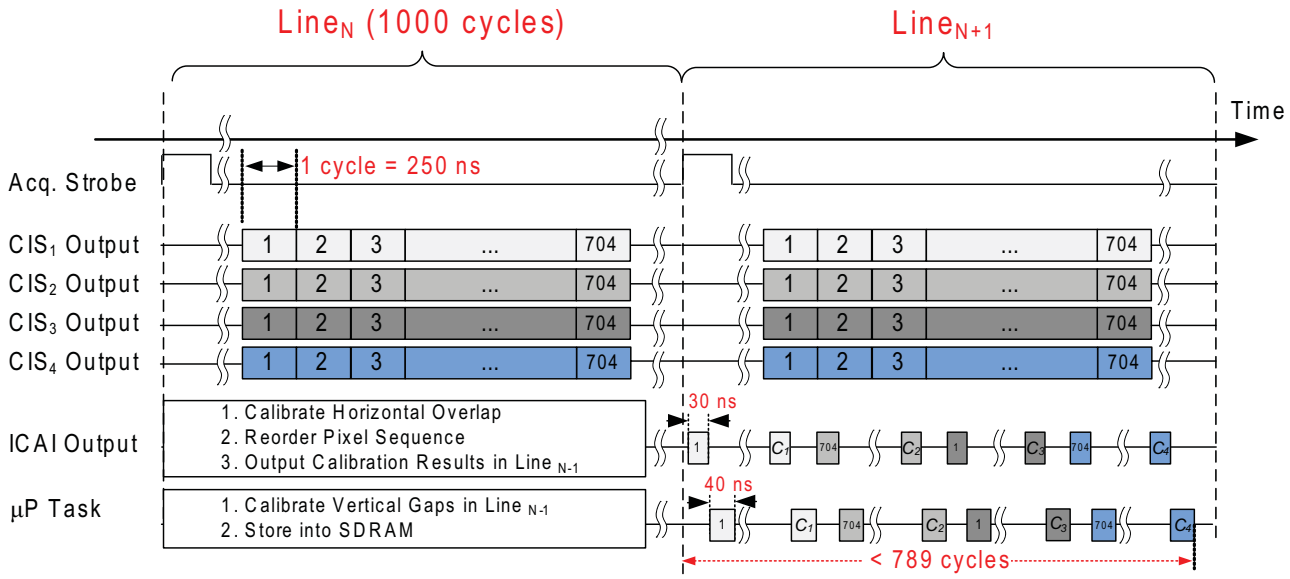


Fig. 10. Timing diagram of the implemented prototype.

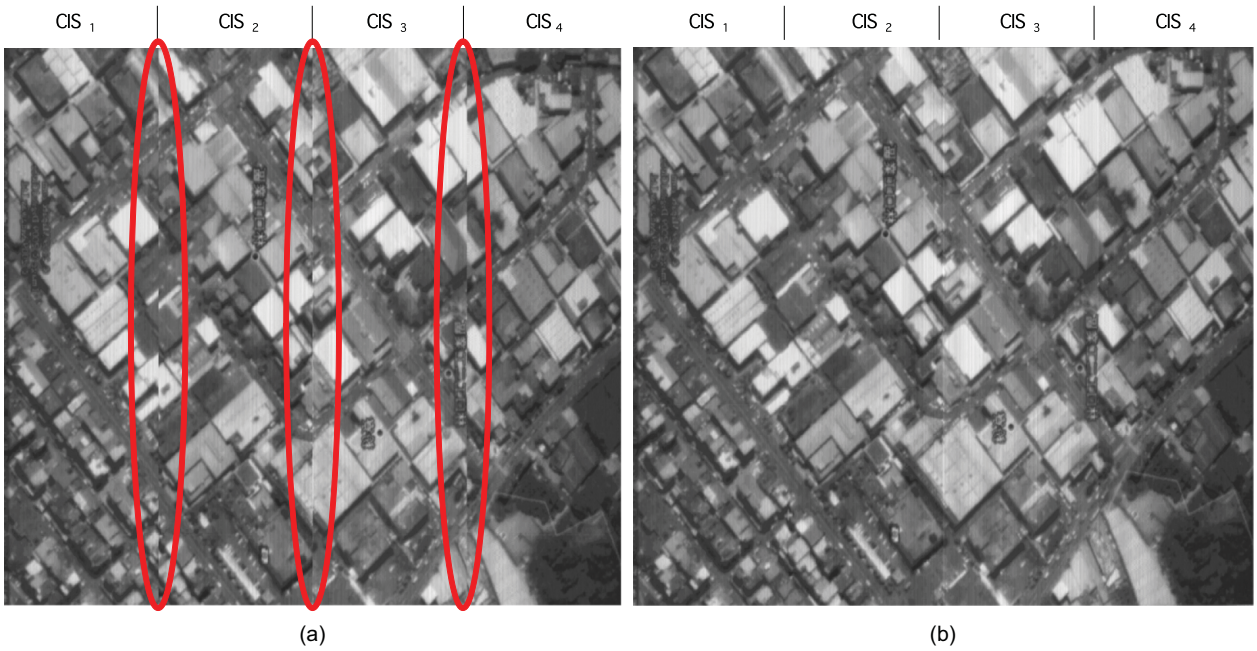


Fig. 11. Satellite's image on industrial district. (a) Without any calibration. (b) Pre-processed by the chip prototype.

a stagger, which is shown in Fig. 8(a). Calibration can be done by shifting the write addresses of images with slight processing overhead, which is shown in Fig. 8(b). The start write pointer of each line image, $WPtr_K$, can be defined as

$$\begin{aligned} &if(N == 1)\\ &\quad WPtr_K = Init\_WPtr_K\\ &else\\ &\quad WPtr_{K,N} = WPtr_{K,N-1} + Comb\_Pixels \end{aligned} \tag{2}$$

where N is the N'th scanned line. The pointer is computed every line image access (700 pixels). The successive pixels access is incremental and no computation is required. The initial memory write pointer, $Init\_WPtr_K$, can be defined as

$$\begin{aligned} &if(K == 1)\\ &\quad Init\_WPtr_K = GP_K \times Comb\_Pixels\\ &else\\ &\quad Init\_WPtr_K = \left(\sum_{l=1}^{K} Pixels - OV_K - 1\right)\\ &\qquad\qquad + GP_K \times Comb\_Pixels \end{aligned} \tag{3}$$

where GP_K is pixels of vertical gaps between CIS_K to CIS_{K+1}. Non-overlapping pixels in each CIS are denoted as *Pixels*, which ranges from 700 to 704. Combined pixels of multi-strip CISs are denoted as *Comb_Pixels,* which ranges

TABLE II
SPECIFICATION OF THE PROPOSED IMAGE PRE-PROCESSING SYSTEM

Total Sensing Number (16 dies)	11,200 pixels
Vertical Gaps Calibration Capability	0-64 pixels
Horizontal Overlaps Calibration Capability	0-8 pixels
Line Rate (32-bit Microprocessor @ 800 MHz ICAI @ 32 MHz)	8000/second

from 2,800 to 2,816 in the prototype, and 11,200 to 11,264 in the final system. The horizontal overlaps pixels between CIS_K to CIS_{K+1}, are denoted as OV_K. Because *Pixels,* OV_K, GP_K, *Comb_Pixels* can be obtained after assembling, $Init\_WPtr_K$ is evaluated once while the system power on; $WPtr_K$ is also required slight computational resource. Therefore, continuous gaps calibration can be achieved by the proposed method.

IV. IMPLEMENTATION RESULTS

The setup of the system prototype is shown in Fig. 9. Manual-focus lenses and CIS mother board was on the fixture. Lenses and CIS mother board were connected with the chip prototype via 80-wire ATA cable. The front LCD monitor showed a satellites' linear moving image. The strip CISs captured the satellites' image line by line and then transferred it to the chip prototype for image combination. The combination result showed on another monitor. As the system prototype powered on, initializations began and then it started continuously image acquiring and combining. In the meantime, the image quality of CIS and real-time performance of system prototype was evaluated by observing VGA display. Further image analysis, such as aspect ratio rectification [1], has been done offline on the host computer by storing image into SD card.

The timing diagram of the implemented prototype is shown in Fig. 10. The clock cycle time is 250 ns, which is 1/2000 of CIS minimum integration time. A time stage is defined as 1000 cycles, that is, 250 μs. After exposure completion, a strobe will trigger CISs to output image pixels concurrently. In the meanwhile, ICAI will acquire the image pixels by using time-division multiplexing method for horizontal overlaps calibration as well as outputting the calibrated line image in the previous time stage to the microprocessor. ICAI FIFOs and stacks readout clock is synchronous with microprocessor to meet data bandwidth demand. As long as one pixel is fetched by microprocessor, it is pushed into SDRAM for gaps calibration. Then, recurrence of fetch and push is continuous until ICAI FIFOs and stacks are empty. Gaps calibration is accomplished implicitly by SDRAM access. Every line image processing time is less than one time stage, which is 250 μs. The timing diagram proves that the proposed real-time and highly-efficient processing hardware can execute continuously.

The specification of the proposed system is listed in Table II. The proposed system can generate 112,00 $\times$ N in 8000 line rate while the microprocessor and ICAI run at 800 MHz and 32 MHz, respectively. 64-pixel gap and 8-pixel overlap calibration capability is accomplished. Gaps calibration capability cannot be limited to 64 pixels; however, the more gaps need to calibrate, the more memory cells are required. In the experimental results, vertical gaps including misalignment error are guarantee to less than 50 pixels. Acquired and combined images are shown in Fig. 11. If no calibration was applied, discontinuity could be seen on the image [Fig. 11(a)]. Fig. 11(b) is the real-time calibration result, which demonstrates functionality of the proposed image pre-processing system.

V. CONCLUSION

The Design and implementation of image pre-processing system were demonstrated to overcome the challenge of real-time high-resolution image acquisition and combination for satellites' remote sensing. The proposed chip integrating sixteen strip CISs, four ICAIs, and two microprocessors has been proved to be able to generate 11,200 $\times$ N high-resolution image. The prototype with four strip CISs has been implemented to verify the real-time performance of final system. Calibrated images were shown to demonstrate the functionality. The implementation result on FPGA shows the proposed system is feasible to integrate into a single chip. This research provides not only a satellites' remote sensing platform but also a solution for high-definition line scan.

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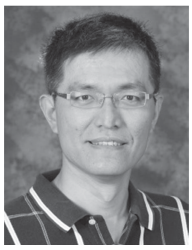

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Dr. Chiu has served as the Technical Program Committee Member and Session Chair in many conferences, such as the VLSI Design/CAD Symposium, VLSI-DAT, AP-ASIC, APCAS, ASPDAC, ISNE, and TESDC. He also served as a Technical Program Committee Chair on the 5th Taiwan ESD Conference, Taiwan, in 2006, and a General Chair on the 6th Taiwan ESD Conference, Taiwan, in 2007. Since 2003, he has been on the advisory committee of the Mixed-Signal and RF Consortium, Heterogeneous Integration Consortium, and Bio-Medical Electronics Consortium, Ministry of Education, Taiwan. He has served as the President of the Taiwan Electrostatic Discharge Association and a Supervisor of Nanotechnology and Micro System Association, in 2010 and 2008, respectively. He also served as a member of MEMS Committee in SEMI Taiwan, since 2010. He was the recipient of the Prof. Wen-Zen Shen Memorial Award for his outstanding contribution to the integrated circuits and system design fields from Taiwan IC Design Society in 2008. He also received the Outstanding Achievement Award in Science and Technology from the National Applied Research Laboratories in 2010.