AIP Applied Physics Letters

Analysis of an anomalous hump in gate current after dynamic negative bias stress in HfxZr1-xO2/metal gate p-channel metal-oxide-semiconductor field-effect transistors

Szu-Han Ho, Ting-Chang Chang, Chi-Wei Wu, Wen-Hung Lo, Ching-En Chen, Jyun-Yu Tsai, Hung-Ping Luo, Tseung-Yuen Tseng, Osbert Cheng, Cheng-Tung Huang, and Simon M. Sze

Citation: Applied Physics Letters **101**, 052105 (2012); doi: 10.1063/1.4739525
View online: http://dx.doi.org/10.1063/1.4739525
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/101/5?ver=pdfcov
Published by the AIP Publishing

Analysis of an anomalous hump in gate current after dynamic negative bias stress in $Hf_xZr_{1-x}O_2$/metal gate p-channel metal-oxide-semiconductor field-effect transistors

Szu-Han Ho,[1] Ting-Chang Chang,[1,2,a)] Chi-Wei Wu,[1] Wen-Hung Lo,[2] Ching-En Chen,[1] Jyun-Yu Tsai,[2] Hung-Ping Luo,[1] Tseung-Yuen Tseng,[1] Osbert Cheng,[3] Cheng-Tung Huang,[3] and Simon M. Sze[1,2,4]
[1]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan*
[2]*Department of Physics, National Sun Yat-Sen University, Kaohsiung 804, Taiwan*
[3]*Device Department, United Microelectronics Corporation, Tainan Science Park, Taiwan*
[4]*Department of Electronics Engineering, Stanford University, Stanford, California 94305, USA*

(Received 15 June 2012; accepted 13 July 2012; published online 30 July 2012)

This letter investigates a hump in gate current after dynamic negative bias stress (NBS) in $Hf_xZr_{1-x}O_2$/metal gate p-channel metal-oxide-semiconductor field-effect transistors. By measuring gate current under initial through body floating and source/drain floating, it shows that hole current flows from source/drain. The fitting of gate current-gate voltage characteristic curve demonstrates that Frenkel-Poole mechanism dominates the conduction. Next, by fitting the gate current after dynamic NBS, in the order of Frenkel-Poole then tunneling, the Frenkel-Poole mechanism can be confirmed. These phenomena can be attributed to hole trapping in high-k bulk and the electric field formula $E_{high\text{-}k}\ \varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2}$. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4739525]

With the scaling down of metal-oxide semiconductor field-effect transistors (MOSFETs), gate current changes from Fowler-Nordheim tunneling current to direct tunneling current, causing power dissipation to increase and performance to degrade. In addition, conventional SiO_2-based dielectrics have approached their physical limits. Hence, replacing SiO_2-based dielectric with high-k based dielectric is a valid way to solve these problems. Furthermore, high-k/metal gate can be integrated with the techniques of silicon on insulator (SOI),[1–3] strained-silicon,[4,5] and multi-gate to improve device characteristic. As recommended in the International Technology Roadmap for Semiconductors, Hf-based dielectrics have been heavily studied to replace SiO_2-based dielectrics in recent years.[6,7] However, HfO_2 suffers from charge trapping,[8–10] mobility degradation, threshold voltage (V_t) instability, and positive bias temperature instability (PBTI) issues. Recently, the $Hf_xZr_{1-x}O_2$ dielectrics have been shown to be a superior gate dielectric to Hf-based dielectric.[11–13] In terms of material characteristics, Zr-doping in HfO_2 transforms the monoclinic crystal structure into a tetragonal crystal structure, leading to a rise in the value of dielectric constant and a decrease in grain size. For electrical characteristics, the increasing value of dielectric constant leads to a decrease in V_t. Diminishing grain size makes $Hf_xZr_{1-x}O_2$ dielectric oxidize more completely during annealing, causing a reduction in charge trapping, an increase in mobility, and a decrease in PBTI.[14] Thus, this study focuses mainly on gate current fitting for $Hf_xZr_{1-x}O_2$ dielectrics p-MOSFETs in dynamic negative bias stress (NBS) because devices generally operate in the dynamic state and gate current generates an anomalous hump. The causes of the hump are explained in this letter.

The $Hf_xZr_{1-x}O_2$/metal gate p-MOSFETs ($x = 8\%–10\%$) used in this study is fabricated through the gate last process. First, high quality thermal oxide with thickness of 1 nm was grown as an interfacial layer. Second, HfO_2, ZrO_2, and HfO_2 dielectrics were deposited in that order by atomic layer deposition (ALD). Then, after annealing, $Hf_xZr_{1-x}O_2$ with thickness of 2 nm was formed. This process may be crystallized into monoclinic crystal structure or tetragonal crystal structure. Finally, Ti_xN_{1-x} was deposited by physical vapor deposition (PVD). Metal gate can eliminate gate depletion and resist remote phonon scattering.[15,16] The p-MOSFETs are stressed in the dynamic condition with 50% duty cycle. A pulse train with high-voltage of V_t-1.1 V, low-voltage of 0 V, and frequency of 10 kHz was applied on the gate terminal. I_g-V_g transfer curves were measured with the source, drain, and body terminals all grounded with V_g given from 0 V to −1.3 V. Then through body floating (BF) and source/drain floating (SDF) process, the current path and carrier polarity can be confirmed. Next, I_g-V_g curve is fitted by Frenkel-Poole current and tunneling current after 0 s and 1000 s dynamic NBS. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

Figures 1(a) and 1(b) show the I_d-V_g and I_g-V_g transfer characteristic curves with −50 mV drain voltage under the dynamic NBS at 0 s, 1 s, 10 s, 100 s, 300 s, 500 s, 700 s, and 1000 s. Clearly, the V_t shift 390 mV in the negative direction and on-current is degraded after the dynamic NBS. Furthermore, subthreshold swing degradation is slight. Thus, V_t shift can be mainly attributed to hole trapping in high-k bulk. However, the gate current hump appears clearly in Fig. 1(b) until 100 s dynamic NBS. With hole trapping increasing, the gate current hump becomes clearer. Therefore, the hump can be generated only when enough holes are trapped in high-k bulk.

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw.

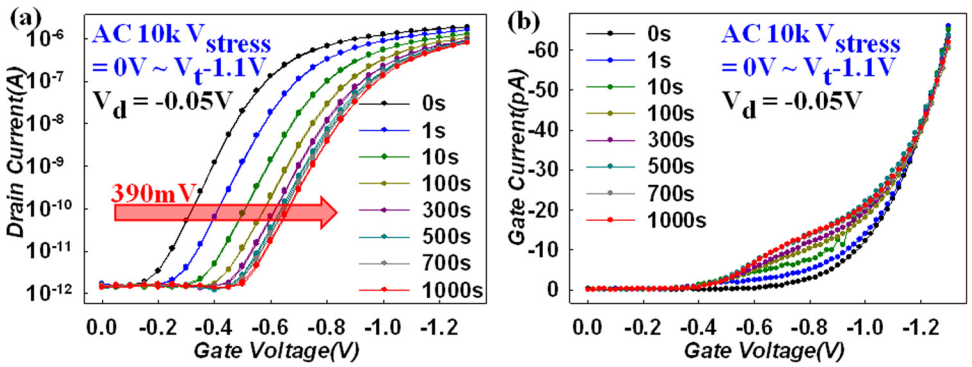

FIG. 1. (a) I_d-V_g and (b) I_g-V_g transfer characteristic curves of high-k/metal gate MOSFETs as function of stress time under dynamic NBS. The sweep was done at $V_d = -0.05$ V for both curves.

To further understand the causes of the hump, fitting and distinguishing gate current are necessary. Figure 2(a) shows I_g-V_g characteristics with BF, source/drain floating (SDF), and body/source/drain all grounded (SDB). Obviously, the I_g-V_g characteristic in BF is similar to that in SDB, and the I_g-V_g characteristic in SDF is much smaller than that in both SDB and BF. These results indicate that holes transfer from source/drain to the gate, rather than electrons transfer from gate to body. Moreover, gate current is fitted under initial as shown in Fig. 2(b), where it can be observed that gate current is confirmed to be the Frenkel-Poole mechanism. These results can be explained from the energy band diagram shown in Fig. 2(a); holes transfer from source/drain to gate with the Frenkel-Poole mechanism.

After confirming Frenkel-Poole mechanism under initial, the I_g-V_g characteristic is fitted after 1000 s dynamic NBS in the Fig. 3(a). Clearly, section A indicates the Frenkel-Poole current in Fig. 3(b), from $V_g = -0.44$ to $V_g = -0.56$, while section B is tunneling current in Fig. 3(c), from $V_g = -0.80$ to $V_g = -0.92$, and section C is again Frenkel-Poole current in Fig. 3(d), from $V_g = -1.18$ to $V_g = -1.3$. In addition, in the $V_g < V_t = 0.9$ V situation, Frenkel-Poole current transfers to tunneling current with V_g increasing. On the contrary, tunneling current transfers to Frenkel-Poole current when $V_g > V_t$. Frenkel-Poole current and tunneling current are a series; whichever current is smaller dominates the current path. Therefore, Frenkel-Poole current dominates current path because $J_{Frenkel\text{-}Poole} \ll J_{Tunneling}$, while tunneling current dominates current path when $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$. Therefore, the conditions under which a hump is generated is $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$.

Figures 4(a) and 4(b) show that energy diagrams for $V_g = 0$ V with hole trapping and without hole trapping, respectively. Note that $E_{high\text{-}k}$ becomes large and E_{SiO2} reduces with hole trapping. An increase in $E_{high\text{-}k}$ produces a larger Frenkel-Poole current, and a reduction in E_{SiO2} produces a larger ΔE_{trap}, causing tunneling current to decrease. ΔE_{trap} indicates the energy from the conduction band in the surface to trap level. Therefore, with hole trapping increasing, $J_{Frenkel\text{-}Poole}$ is larger than $J_{Tunneling}$. Because the hump generation condition is $J_{Frenkel\text{-}Poole} \gg J_{Tunneling}$, the hole trapping leads to a more significant hump. In Figs. 1(a) and 1(b), it can be observed that the more holes that are captured in high-k bulk, the clearer gate current hump we can see. Figure 4(c) shows energy diagrams in the $V_g < V_t$ situation with hole trapping. The electric field must follow the formula $E_{high\text{-}k}\ \varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\ E_{sio2} = \varepsilon' E_{sio2}$, where Q indicates the quantity of hole trapping ($Q > 0$), E_{sio2} indicates an electric field in the SiO_2, and $E_{high\text{-}k}$ is an electric field in the high-k. The voltage across gate oxide is small when $V_g < V_t$. Hence, Q/E_{sio2} cannot be ignored ($Q \gg E_{sio2}$). This result makes $\varepsilon_{high\text{-}k} < \varepsilon'$ and $E_{high\text{-}k} > E_{sio2}$. When V_g is swept from 0 V to V_t on the device with a large amount of hole trapping in high-k bulk, most of the applied gate voltage drops in the $Hf_xZr_{1-x}O_2$ layer. This is the reason why $J_{Frenkel\text{-}Poole}$ after dynamic NBS appears earlier than $J_{Frenkel\text{-}Poole}$ under initial. Nevertheless, relatively smaller voltage drops in the SiO_2 layer, leading to a slight rise in $J_{Tunneling}$ due to a small variation in ΔE_{trap}. With an increase in V_g, $J_{Frenkel\text{-}Poole}$ increases significantly while $J_{Tunneling}$ changes only slightly. This causes $J_{Frenkel\text{-}Poole}$ to change to $J_{Tunneling}$. At the beginning stages, $J_{Frenkel\text{-}Poole}$ appears in section A (Fig. 3(a)) owing to the supply of holes exceeding the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$). Next, $J_{Tunneling}$ appears in section B (Fig. 3(a)), because the supply of holes is unable to meet the demand ($J_{Tunneling} \ll J_{Frenkel\text{-}Poole}$).

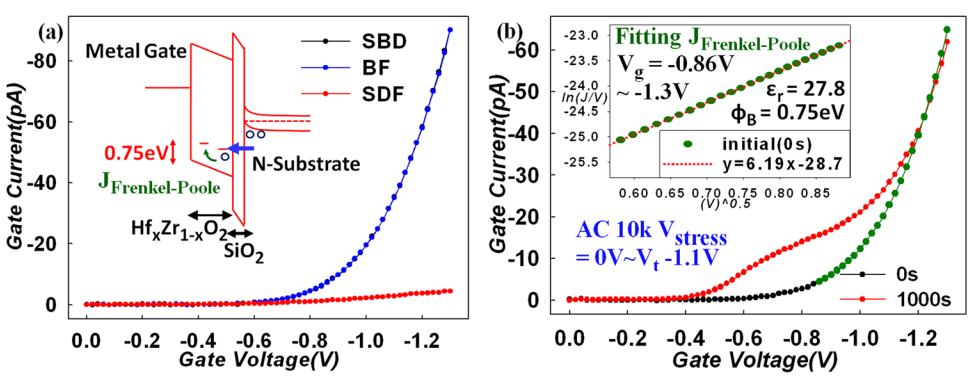

FIG. 2. (a) I_g-V_g characteristic curves in the SBD, BF, and SDB conditions. The energy band diagram shows gate current is the Frenkel-Poole path. (b) I_d-V_g transfer characteristic curves of high-k/metal gate MOSFETs under initial and after dynamic NBS. Inset shows that gate current is fitted by Frenkel-Poole model under initial.

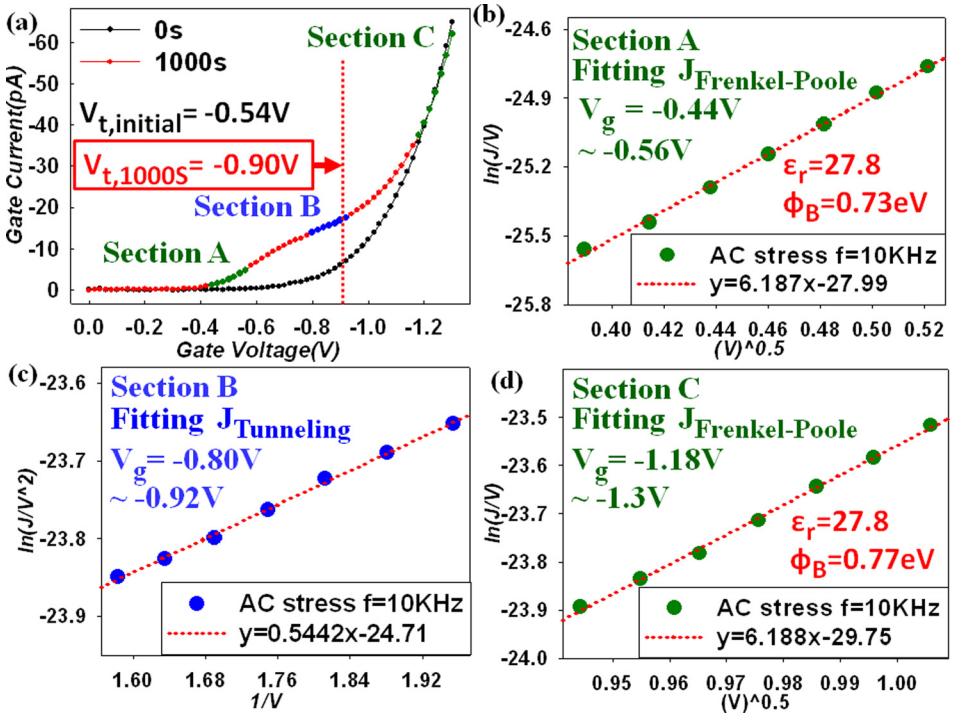

FIG. 3. (a) I_d-V_g transfer characteristic curves under initial and after dynamic NBS. (b) Gate current in section A is fitted by Frenkel-Poole model after dynamic NBS. (c) Gate current in section B is fitted by tunneling model after dynamic NBS. (d) Gate current in section C is fitted by Frenkel-Poole model after dynamic NBS.

Figure 4(d) shows energy diagrams in the $V_g > V_t$ condition with hole trapping. The electric field should also obey formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2} = (Q/E_{sio2} + \varepsilon_{sio2})\,E_{sio2}$. On the contrary, V_g applied to SiO_2 and $Hf_xZr_{1-x}O_2$ in the $V_g > V_t$ condition is large, causing Q/E_{sio2} to be ignored ($Q \ll E_{sio2}$). This result leads to $\varepsilon_{high\text{-}k} > \varepsilon_{sio2}$ and $E_{high\text{-}k} < E_{sio2}$. Therefore, with V_g increasing, ΔE_{trap} decreases, and $J_{Tunneling}$ increases sharply due to the exponential dependence on ΔE_{trap}. This is the reason why $J_{Tunneling}$ changes to $J_{Frenkel\text{-}Poole}$. Finally, $J_{Frenkel\text{-}Poole}$ appears in section C (Fig. 3(a)), since the supply of holes exceeds the demand ($J_{Tunneling} \gg J_{Frenkel\text{-}Poole}$).

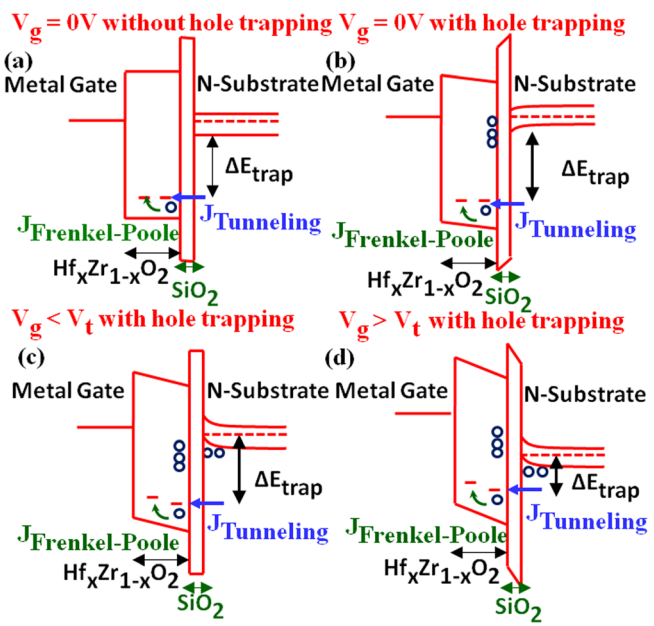

FIG. 4. The energy band diagram of high-k/metal gate MOSFETs in the $V_g = 0$ V condition (a) without hole trapping and (b) with hole trapping. (c) The energy band diagram of high-k/metal gate MOSFETs in the $V_g < V_t$ condition with hole trapping. (d) The energy band diagram of high-k/metal gate MOSFETs in the $V_g > V_t$ condition with hole trapping.

In summary, the V_t shifts 390 mV in the negative direction and the hump generates in the I_g-V_g transfer characteristic curves after dynamic NBS, and these are results of hole trapping in high-k bulk. Through fitting and distinguishing gate current under initial, holes transfer through the Frenkel-Poole mechanism from the source and drain. Gate current fitting after dynamic NBS indicates that $J_{Frenkel\text{-}Poole}$ changes to $J_{Tunneling}$ in the $V_g < V_t$ situation owing to the influence of $E_{high\text{-}k} > E_{sio2}$, while $J_{Tunneling}$ changes to $J_{Frenkel\text{-}Poole}$ in the $V_g > V_t$ condition due to the influence of $E_{high\text{-}k} < E_{sio2}$. These phenomena can be attributed to the fact that the electric field must follow the formula $E_{high\text{-}k}\,\varepsilon_{high\text{-}k} = Q + E_{sio2}\varepsilon_{sio2}$.

Part of this work was performed at United Microelectronics Corporation. The work was supported by the National Science Council under Contract No. NSC 100-2120-M-110-003.

[1]C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. C. Chen, C. T. Tsai, W. H. Lo, S. H. Ho, G. Xia, O. Cheng, and C. T. Huang, Surf. Coat. Technol. **205**, 1470–1474 (2010).
[2]C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, F. Y. Jian, W. H. Lo, S. H. Ho, C. E. Chen, W. L. Chung, J. M. Shih, G. Xia, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **32**, 7 (2011).
[3]W. H. Lo, T. C. Chang, C. H. Dai, W. L. Chung, C. E. Chen, S. H. Ho, O. Cheng, and C. T. Huang, IEEE Electron Device Lett. **33**, 3 (2012).
[4]Y. J. Kuo, T. C. Chang, P. H. Yeh, S. C. Chen, C. H. Dai, C. H. Chao, T. F. Young, O. Cheng, and C. T. Huang, Thin Solid Films **517**, 1715 (2009).
[5]Y. J. Kuo, T. C. Chang, C. H. Dai, S. C. Chen, J. Lu, S. H. Ho, C. H. Chao, T. F. Young, O. Cheng, and C. T. Huang, Electrochem. Solid-State Lett. **12**, H32 (2009).
[6]C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, S. H. Ho, T. Y. Hsieh, W. H. Lo, C. E. Chen, J. M. Shih, W. L. Chung, B. S. Dai, H. M. Chen, G. Xia, O. Cheng, and C. T. Huang, Appl. Phys. Lett. **99**, 012106 (2011).
[7]C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, W. H. Lo, S. H. Ho, C. E. Chen, J. M. Shih, H. M. Chen, B. S. Dai, G. Xia, O. Cheng, and C. T. Huang, Appl. Phys. Lett. **98**, 092112 (2011).

[8]C. H. Dai, T. C. Chang, A. K. Chu, Y. J. Kuo, Y. C. Hung, W. H. Lo, S. H. Ho, C. E. Chen, J. M. Shih, W. L. Chung, H. M. Chen, B. S. Dai, T. M. Tsai, G. Xia, O. Cheng, and C. T. Huang, Thin Solid Films **520**, 1511 (2011).
[9]W. H. Lo, T. C. Chang, J. Y. Tsai, C. H. Dai, C. E. Chen, S. H. Ho, H. M. Chen, O. Cheng, and C. T. Huang, Appl. Phys. Lett. **100**, 152102 (2012).
[10]M. Chang, M. Jo, S. Jung, J. Lee, S. Jeon, and H. Hwang, Appl. Phys. Lett. **94**, 262107 (2009).
[11]D. H. Triyoso, R. I. Hegde, J. K. Schaeffer, R. Gregory, X.-D. Wang, M. Canonico, D. Roan, E. A. Hebert, K. Kim, J. Jiang, R. Rai, V. Kaushik, and S. B. Samavedam, J. Vac. Sci. Technol. B **25**, 3 (2007).
[12]D. H. Triyoso, R. I. Hegde, J. Jiang, J. K. Schaeffer, and M. V. Raymond, IEEE Electron Device Lett. **29**, 1 (2008).
[13]W. C. Wu, T. S. Chao, T. H. Chiu, J. C. Wang, C. S. Lai, M. W. Ma, and W. C. Lo, IEEE Electron Device Lett. **29**, 12 (2008).
[14]H. S. Jung, S. A. Lee, S. h. Rha, S. Y. Lee, H. K. Kim, D. H. Kim, K. H. Oh, J. M. Park, W. H. Kim, M. W. Song, N. I. Lee, and C. S. Hwang, IEEE Trans. Electron Devices **58**, 7 (2011).
[15]W. J. Zhu and T. P. Ma, IEEE Electron Device Lett. **25**, 2 (2004)
[16]R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, Electron Devices Lett. **25**, 6 (2004).