Design and Iso-Area $V_{\min}$ Analysis of 9T Subthreshold SRAM With Bit-Interleaving Scheme in 65-nm CMOS

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***Abstract*—In this brief, a 9T bit cell is proposed to enhance write ability by cutting off the positive feedback loop of a static random-access memory (SRAM) cross-coupled inverter pair. In read mode, an access buffer is designed to isolate the storage node from the read path for better read robustness and leakage reduction. The bit-interleaving scheme is allowed by incorporating the proposed 9T SRAM bit cell with additional write wordlines (WWL/WWLb) for soft-error tolerance. A 1-kb 9T 4-to-1 bit-interleaved SRAM is implemented in 65-nm bulk CMOS technology. The experimental results demonstrate that the test chip minimum energy point occurs at 0.3-V supply voltage. It can achieve an operation frequency of 909 kHz with 3.51-μW active power consumption.**

***Index Terms*—Bit-interleaving scheme, iso-area analysis, subthreshold static random-access memory (SRAM).**

I. Introduction

EMBEDDED static random-access memories (SRAMs) dominate the power consumption, area, performance, and yield of emerging portable electronic devices. These devices require low energy consumption to allow long operational lifetimes as they are often battery powered. The design of subthreshold SRAMs is popularly utilized because lowering the supply voltage can quadratically reduce the energy consumption [1]. However, as the supply voltage is below the transistor threshold voltage, the variability of SRAM increases severely in design and process parameters regarding proper ratio of device strengths [2]. Major subthreshold SRAM stability issues include process-induced device variation, decreasing $I_{\rm ON}-I_{\rm OFF}$ ratio, and threshold voltage random variation (σ_{VT}) [3]. The standard 6T bit cell fails to perform reliable weak-inversion operations because of read-current-disturbance-induced static noise margin (SNM) degradation. Various more-than-6T bit cells were presented to address the read reliability issue, such as 8T bit cells [4], [5]. They added two transistors as the read buffer to isolate the storage node from the bitline, resulting in better read stability.

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The soft-error problem becomes more critical for ultralow-voltage SRAMs than superthreshold SRAMs because the critical charge in storage node is much less. As reported in [6], the soft-error rate increases by 18% for every 10% supply voltage reduction. In order to enhance subthreshold SRAMs' soft-error immunity, the bit-interleaving scheme is always preferred. It can spatially separate bits of a word in the row, and only simple single-bit error correction coding is needed. However, the read-buffered 8T bit cell designed with the bit-interleaving scheme suffered from write-half-select disturbance. To solve the issue, an array architecture and circuits with 12% area overhead, compared to 8T SRAM design, were presented in [7]. The array architecture addressed the half-select problem by decoupling large bitline capacitance from half-selected cells. In [8], a fully differential 10T bit cell was presented for high read stability. Meanwhile, it can be designed with bit-interleaving scheme by vertical and horizontal wordlines. It required boosted wordline technique to maintain robust write operation. Recently, a fully differential 8T SRAM with a column-based dynamic supply scheme was presented in [9]. By utilizing different cell supply voltages for basic modes, it successfully separated the read/write/standby operations to allow it to be bit interleaved.

In this brief, we propose a 9T bit cell with enhanced write ability by inserting a pass transistor into the cross-coupled inverter pair. To allow the bit-interleaving array scheme for 9T bit cells, two additional write wordlines (WWL/WWLb) are used. Some preliminary results were first presented in [10]. Advanced iso-area SRAM stability analysis and fabricated test chip experimental results are proposed in this work. The remainder of this brief is organized as follows: Section II describes the basic operations and layout considerations of our 9T bit cell. Advanced iso-area SRAM $V_{\min}$ analysis is discussed in Section III. Section IV shows the implementation of a 1-kb 9T SRAM with the bit-interleaving array scheme and the measurement results. The final section concludes this work.

II. 9T Subthreshold SRAM Bit-Cell Design

The block diagram of the proposed 9T bit cell is shown in Fig. 1. It adapts multiple threshold CMOS technique, including high V_t and regular V_t devices to deliver the benefits of saving leakage and increasing write margin (WM)/hold SNM (HSNM), respectively. Three n-type transistors, i.e., MAR, MAW, and MDR, construct the access buffer. Their device length increase to 100 nm, utilizing reverse short-channel effect for better $I_{\rm ON}-I_{\rm OFF}$ ratio and less threshold voltage variation

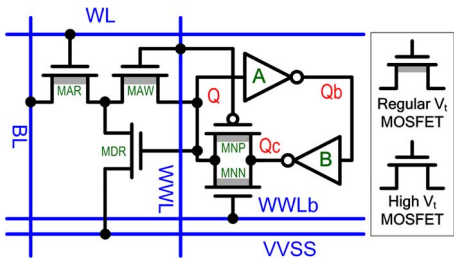

Fig. 1. Block diagram of the proposed 9T bit cell. The relative threshold voltage ratio of high-V_t MOSFET to a regular-V_t one is 1.3 to 1.

caused by random dopant fluctuation. The voltage drop of write operation is reduced by choosing the access transistors MAR and MAW of regular V_t devices. The pass transistors MNP and MNN are inserted into a cross-coupled inverter pair for write ability enhancement. However, they also cause HSNM degradation, which is negligible by having them in a regular V_t device. Other MOSFETs in the proposed bit cell are high V_t devices for leakage reduction. In addition, the single bitline scheme and virtual ground signal $VVSS$ are adopted for leakage reduction. $VVSS$ is attached to VDD, except that it is discharged to ground in read mode. To enable the SRAM design with the bit-interleaving scheme, there are three wordlines WL, WWL, and $WWLb$ in our 9T bit cell. The write-wordline WWL and its complementary signal $WWLb$ are enabled (disabled) only in write mode, whereas WL is enabled in both read and write modes.

During hold mode, MAR and MAW of the access buffer are turned off to form a cascaded transistor structure. It reduces the bitline leakage current considerably. In read mode, MAW is turned off to isolate the read path and storage node, thus eliminating read disturbance. Because of the isolation, its read SNM (RSNM) is nearly the same as its HSNM. The channel length of the read buffer MAR and MDR increases to 100 nm for single-ended read delay time and stability enhancement. Note that the foot of the read buffer is connected to virtual ground $VVSS$. While the foot of the selected word during read operation is pulled to GND, all the other feet of read buffers are connected to VDD in all rows of the SRAM arrays for leakage reduction. However, the read delay of this 9T bit cell is still $1.38\times$ slower than the differential 10T bit cell [11] with iso-area condition at 0.3-V supply voltage. It is acceptable since speed is not the primary constraint in subthreshold design.

Writing-"1" is the worst case of this 9T bit cell because it is much harder to pass "1" than "0" through the two n-type MAR and MAW in series of the access buffer. However, the pass transistor MNP and MNN is OFF to improve our 9T bit-cell WM by breaking the positive feedback loop of the cross-coupled inverter pair. Meanwhile, the virtual ground $VVSS$ is attached to VDD in write mode, thus helping the writing-"1" operation. The performances of 9T bit-cell basic operations are presented in our earlier work [10]. The WM of this 9T bit cell is $1.64\times$ better than that of the 10T bit cell with iso-area condition at 0.3-V supply voltage. Note that the disturbance caused by virtual ground during writing-"0" operation makes the write delay increase a little.

The proposed 9T bit cell not only effectively enhances write operation robustness but also provides efficient bit-interleaving

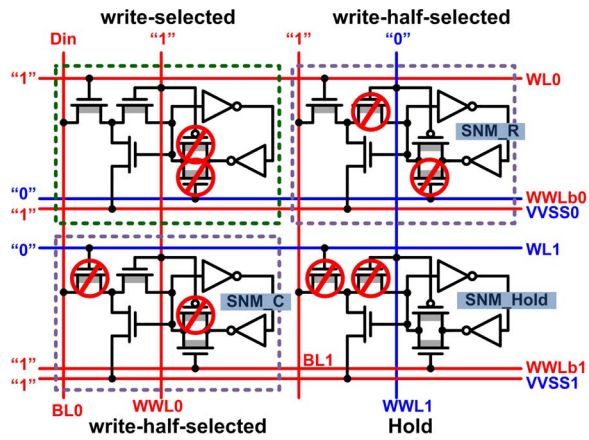

Fig. 2. Schematic illustration of the proposed 9T bit cells free of the write-half-select problem.

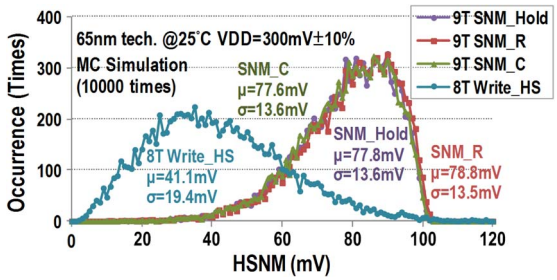

Fig. 3. HSNM distributions of write-half-selected 9T/8T bit cells.

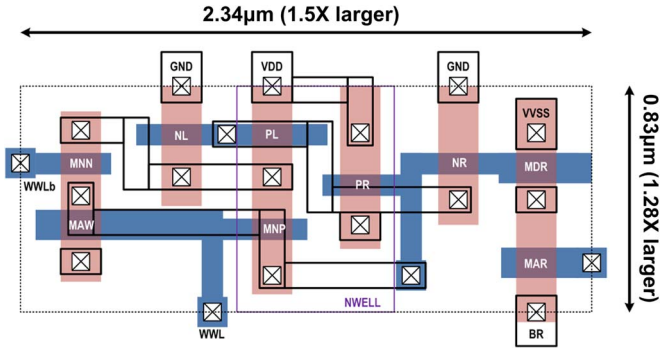

Fig. 4. Layout view of the proposed 9T bit cell. Its size is $1.92\times$ larger than 6T mincell.

scheme to achieve soft-error tolerance with simple error correction codes. In order to show our 9T bit cell to be free of the write-half-select problem, a schematic illustration with four bit cells in different operation modes is shown in Fig. 2. Monte Carlo simulations of HSNM are performed using 65-nm bulk CMOS technology models, which include global and local process variations. For an 8T write-half-selected bit cell, its HSNM distribution is degraded by the disturbance, as shown in Fig. 3. In this brief, the write-half-selected bit cell in the same row SNM_R is disturbance free because MAW is turned off by WWL. Meanwhile, the bit cell in the same column SNM_C is not affected by disturbance because MAR is turned off by WL. The HSNM distributions of them are nearly the same as the hold bit cell SNM_Hold, as shown in Fig. 3.

Layout implementation is under 65-nm bulk CMOS technology using logic design rules. In Fig. 4, the proposed 9T bit-cell

size is 2.34 μm $\times$ 0.83 μm with 2 poly-pitch thin-cell style. The write-wordline WWL is in the direction of the bitline. Its complementary signal $WWLb$ and virtual ground $VVSS$ are in the direction of the wordline. The 9T bit cell occupies 1.55$\times$ larger area, compared with an 8T bit-cell area. This is due to the additional pass transistors and the three-transistor access buffer with 100-nm channel length.

III. Iso-Area SRAM Bit-Cell $V_{\min}$ Analysis

A. Iso-Area Bit Cells

To analyze the minimum operation voltage ($V_{\min}$) for SRAM bit-cell hold/read/write operations, it is only fair to compare the bit cells under iso-area condition. In this brief, a 2$\times$ area of 6T mincell is adopted as a benchmark since the proposed 9T bit cell consumes approximately 1.92$\times$ area, as shown in Fig. 4. In a thin-cell layout approach, the SRAM bit-cell area is dominated by the contact and the diffusion spacing. If we expand the bit-cell area by increasing the channel length along the bitline direction, the bitline power consumption will be increased because of the larger bitline capacitance. Therefore, the best bit-cell upsizing means is increasing the device widths along the wordline since bitline power is a major part of the SRAM overall power consumption [11]. Monte Carlo simulations are performed using 65-nm bulk CMOS technology models, which include global and local process variations. Bit-cell failure probability is estimated, assuming Gaussian distribution of the threshold voltage.

1) 6T Iso-Area Bit Cell: In this brief, we use 6T mincell device widths of 120, 120, and 240 nm for pull-up/access/pull-down transistors, respectively. For the 2$\times$ larger area, the 6T mincell device widths need to be upsized by 4$\times$. All transistors in the 6T mincell are upsized uniformly to improve the read stability and write ability simultaneously.

2) 8T Iso-Subarray-Area Bit Cell: The single-ended 8T SRAM designs often prefer hierarchical bitline architecture to improve performance. The architecture is adopted because of large signal sensing and evaluation-delay/noise-immunity tradeoff at the local bitline node. Thus, single-ended 8T bitcell array efficiency is about 15%–30% lower than the 6T bit-cell array design. Considering the difference in the array efficiency, the 8T iso-area bitcell $V_{\min}$ should be evaluated at iso-subarray-area condition. In this brief, any additional area increase is used for the write access transistors to improve the write-$V_{\min}$ because the 8T bit cell has a buffered read structure. We use 8T iso-subarray-area bit-cell device widths of 120, 360, 240, and 120 nm for pull-up/access/pull-down/buffered-read transistors, respectively.

3) 10T Iso-Area Bit Cell: A 10T bit cell [8] with separated read/write operation was presented to enable the bit-interleaving scheme. The differential read path is designed to ensure reliable operation, instead of single-ended one. It is also a read-disturb-free design. Thus, any additional area is used to upsize the write-access transistors for iso-area comparison. The differential 10T bit cell consumes about 1.66$\times$ larger area, compared with the 6T mincell [11]. In this brief, we use 10T iso-area bit-cell device widths of 120, 240, 240, and

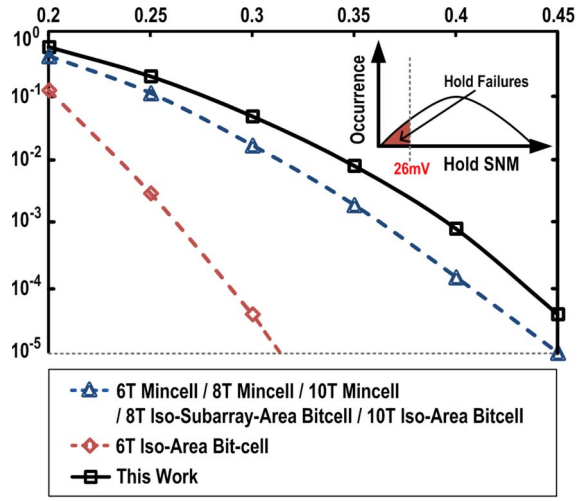

Fig. 5. Hold-failure probability comparison.

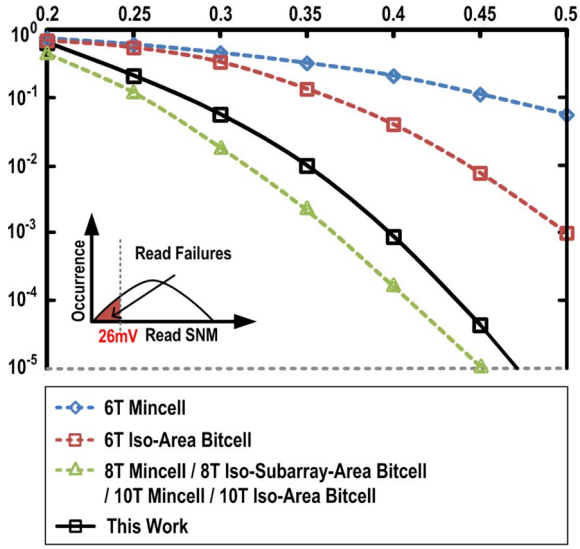

Fig. 6. Read-failure probability comparison.

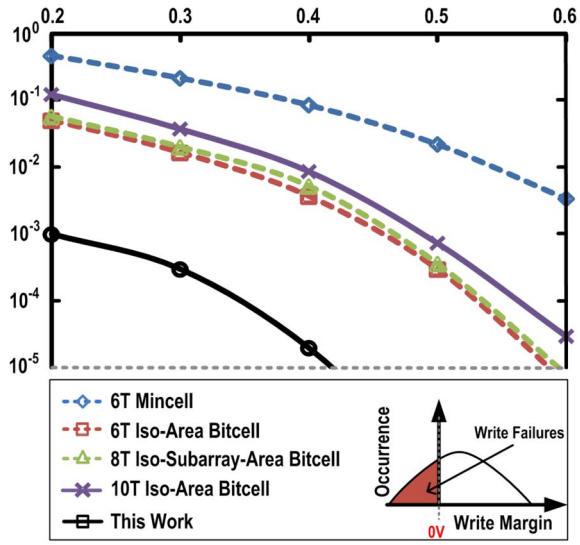

Fig. 7. Write-failure probability comparison.

TABLE I
V_{min} COMPARISON OF VARIOUS BIT-CELL TOPOLOGIES

Bit-Cell Topology	Hold V_{min} (mV)	Read V_{min} (mV)	Write V_{min} (mV)	V_{min} (mV)
6T mincell (1X Area)	450	1000	826	1000
6T bit-cell (4X upsized, Iso-Area)	313	599	588	599
8T bit-cell [4] (Iso-Subarray-Area)	450	450	591	591
10T bit-cell [8] (Iso-Area)	450	450	630	630
This Work (Iso-Area)	470	470	415	470

120 nm for pull-up/access/pull-down/buffered-read transistors, respectively.

B. Hold-Failure Probability

HSNM is used to quantify the hold stability of the SRAM bit cells. Hold-failure probability $(P_{\text{hold}-\text{fail}})$ is estimated as

$$P_{\text{hold}-\text{fail}} = Prob.(\text{HSNM} < kT). \quad (1)$$

If HSNM is lower than the thermal voltage ($kT = 26$ mV at 300K), the bit-cell contents can be flipped due to thermal noise. Hold-$V_{\min}$ is determined at the 3-sigma hold-failure probability (i.e., $P_{\text{hold}-\text{fail}} = 10^{-5}$). Fig. 5 shows hold-failure probability versus supply voltage for 6T mincell, 6T/8T/10T iso-area bit cell, and the proposed 9T iso-area bit cell. As the size of the cross-coupled inverter pair in the 8T/10T bit cell is the same as that for the 6T mincell, it would result in similar hold-failure probability. In addition, the HSNM of the upsizing 6T iso-area bit cell is better than that of the 6T mincell. In this brief, our 9T bit-cell HSNM is slightly degraded because of the pass transistor inserted into the cross-coupled inverter pair.

C. Read-Failure Probability

Similar to the hold stability case, read stability is estimated by computing the RSNM. Fig. 6 plots the read-failure probability variation versus supply voltage for 6T mincell, 6T/8T/10T iso-area bit cell, and the proposed 9T iso-area bit cell. As shown in the inset, the read-failure probability $(P_{\text{read}-\text{fail}})$ is calculated as

$$P_{\text{read}-\text{fail}} = Prob.(\text{RSNM} < kT). \quad (2)$$

Read-$V_{\min}$ is determined at the 3-sigma read failure probability (i.e., $P_{\text{read}-\text{fail}} = 10^{-5}$). For 8T and 10T bit cells, the read stability is the same as the hold stability as bit-cell nodes are not disturbed during the read operation. As previously explained, the cross-coupled inverter pair size in 8T/10T bit cell and 6T mincell are the same, it would show similar hold-failure probability, as shown in Fig. 5. It is also observed that upsizing 6T device dimensions enhance RSNM. In this brief, the MAW of the access buffer in our 9T bit cell is turned off to prevent read disturb. Therefore, its read-failure probability is the same as the hold-failure probability.

D. Write-Failure Probability

Write ability gives an indication of how easy or difficult it is to write to the bit cell. WM is defined as

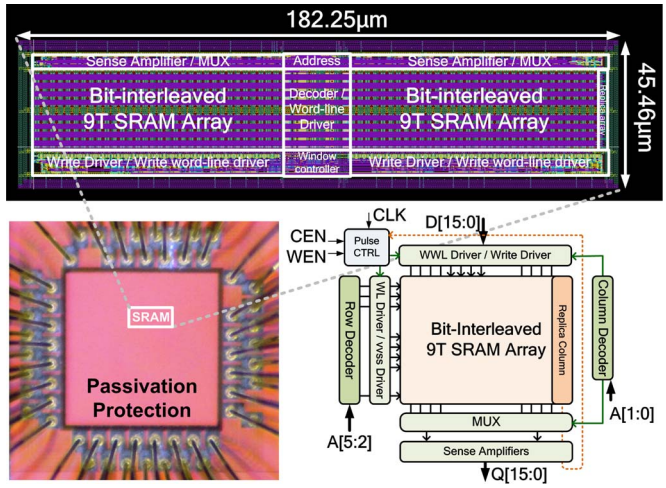

Fig. 8. Die photo and block diagram for the 1-kb 9T SRAM test chip fabricated in 65-nm bulk CMOS process.

VDD-Min.[V(WWL)]. Min.[V(WWL)] is the minimum write-wordline voltage required for flipping the bit cell. The higher the WM, the easier data are written into the bit cell. Fig. 7 shows the write-failure probability versus supply voltage. As shown in the inset, the write-failure probability $(P_{\text{write}-\text{fail}})$ is estimated as

$$P_{\text{write}-\text{fail}} = Prob.(\text{WM} < 0\ \text{mV}). \quad (3)$$

Write-$V_{\min}$ is determined at the 3-sigma write-failure probability (i.e., $P_{\text{write}-\text{fail}} = 10^{-5}$). The 10T bit cell has higher write-failure probability than the 6T/8T bit cells under iso-area condition because of the series access transistors. In this brief, cutting off the positive feedback loop of the cross-coupled inverter pair in 9T bit cell fairly improves its write ability.

E. Iso-Area $V_{\min}$ Comparison

Table I compares the estimated $V_{\min}$ for various bit-cell topologies. $V_{\min}$ is calculated as the maximum value of Hold-$V_{\min}$, Read-$V_{\min}$, and Write-$V_{\min}$. The $V_{\min}$ of 8T and 10T bit cells is limited by the write operation. The proposed 9T bit cell enhances the write ability by utilizing the pass transistor within the cross-coupled inverter pair. However, HSNM/RSNM is degraded a little. Our 9T bit cell has better $V_{\min}$ in these state-of-the-art bit cells. Note that the effect of various read/write assist techniques is not taken into account.

IV. MEASUREMENT RESULTS

The test chip fabricated in UMC 65-nm CMOS technology contains 1-kb (64-word by 16-bit) 9T 4-to-1 bit-interleaved

TABLE II
TEST CHIPS MEASUREMENT SUMMARY AND COMPARISON

Bit-cell	**8T** 2008JSSC [4]	**8T** 2009JSSC [5]	**10T** 2009JSSC [8]	**8T** 2011TCAS-I [9]	**9T** This Work
Bit-cell Size*	1	1.2	1.26**	1	1.55
#WL	1RWL+1WL	1WWL+1RWL	1WWL+1WL	1WL(+1CS)	2WWL+1WL
#BL	2WBL+1RBL	2WBL+1RBL	2BL	2BL	1BL
Bit-interleaving	N	N	Y	Y	Y
Technology	65nm CMOS	130nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Memory Size	256Kbit	64Kbit	32Kbit	8Kbit	1Kbit
Chip Size	1.12×1.89 mm^2	0.72×0.85 mm^2	4×2 mm^2	N/A	0.9×0.9 mm^2
Operating Voltage	0.35V	0.23V	0.16V	0.2V	0.3V
Frequency	25kHz	100kHz	0.5kHz	41kHz	909kHz
Active Power	3.39μW	0.989μW	0.123μW	0.012μW***	3.51μW
Power/Frequency	135.6μW/MHz	9.89μW/MHz	246μW/MHz	0.29μW/MHz****	3.86μW/MHz
Iso-area $V_{\min}$	591mV	591mV	630mV	550mV	470mV

*: The bit-cell size is normalized to [4]. **: The 10T bit-cell size was reported in [11].
: It was estimated from Fig. 20 in [9]. *: The best value was 0.13pJ at 0.3V supply voltage.

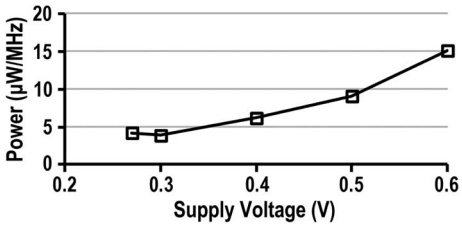

Fig. 9. Measured power of 1-kb 9T SRAM versus VDD.

SRAM design with core size 182.25×45.46 μm^2 using logic design rules. The die photo and block diagram are shown in Fig. 8. The proposed 9T bit-cell size is $1.92\times$ larger than the standard 6T thin cell layout based on the same design rules. Several circuit designs including address decoder, wordline driver, replica column, and read/write pulse controller were presented in [10]. Note that a replica column of 9T SRAM and a read pulse controller are implemented to adaptively control the wordline pulse width for process, voltage and temperature (PVT) variation tolerance. The test patterns are generated from logic analyzer 16900A, and the outputs of the test chips are captured by logic analyzer and digital oscilloscope. There are 18 dies being measured, and Table II shows the test chips measurement summary. The chip can successfully operate from 33 MHz at 0.6 V to 0.48 MHz at 0.27 V. The average leakage current of test chips is 585 nA at 0.3 V. Up to $3.91\times$ energy saving is achieved by scaling supply voltage from 0.6 to 0.3 V. The minimum energy point shown in Fig. 9 is at 0.3-V supply voltage, which takes 3.86 pJ (3.51 μW/909 kHz) energy consumption.

V. CONCLUSION

A subthreshold 9T SRAM with bit-interleaving scheme fabricated in 65-nm bulk CMOS process has been able to operate at a supply voltage of 0.27 V. By inserting the pass transistor into the cross-coupled inverter pair, the Write-$V_{\min}$ can be lowered to 415 mV at the 3-sigma write-failure probability. The best iso-area $V_{\min}$ of only 470 mV has been achieved. At a minimum energy point of 0.3 V, the test chip with an energy consumption of 3.86 pJ can compete with state-of-the-art SRAMs. The proposed 9T SRAM is an energy-efficient design for emerging ultralow-power applications.

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