The Effects of NH_3 Plasma Passivation on Polysilicon Thin-Film Transistors

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***Abstract*— The NH_3 plasma passivation has been performed for the first time on the polycrystalline silicon (poly-Si) thin-film transistors (TFT's). It is found that the TFT's after the NH_3 plasma passivation achieve better device performances, including the off-current below 0.1 pA/μm and the on/off current ratio higher than 10^8, and also better hot-carrier reliability as well as thermal stability than the H_2-plasma ones. These improvements were attributed to not only the hydrogen passivation of the grain-boundary dangling bonds, but also the nitrogen pile-up at SiO_2/poly-Si interface and the strong Si-N bond formation to terminate the dangling bonds at the grain boundaries of the polysilicon films.**

I. Introduction

POLYCRYSTALLINE silicon (Poly-Si) thin-film transistors (TFT's) are of interest for a number of applications, such as ultra-large-scale-integration (ULSI) memories and large-area electronic devices (displays, sensors, etc.) [1], [2]. In these devices, defects either in the bulk or at grain boundaries play a critical role [3]. To obtain high-performance poly-Si TFT's, it is necessary to reduce the trap-states of the polysilicon films. It is now well known that hydrogenation leads to tie up the grain boundary dangling bonds with hydrogen, thereby significantly improve the characteristics of the poly-Si TFT's [4]. However, it had been observed that the characteristics of the poly-Si TFT's after the hydrogen passivation suffer a low hot-carrier endurance and a low thermal stability [5], [6]. In this letter, a simpler technique, NH_3-plasma passivation, was employed to enhance both the electrical reliability and the thermal stability of the poly-Si TFT's.

II. Experimental Procedures

The poly-Si TFT's were fabricated on thermally oxidized silicon wafers. A 110 nm thick amorphous silicon (α-Si) was initially deposited at 550°C by low-pressure chemical vapor deposition (LPCVD) using pure SiH_4, and then furnace annealed at 600°C for 24 h in N_2 ambient to recrystallize the silicon films. After defining the active islands, a 70 nm thick silicon-dioxide was thermally grown by dry oxidation. Another 300 nm polysilicon film was deposited at 620°C in an LPCVD system and patterned to be the gates of the devices. A self-aligned $POCl_3$ doping was performed at 900 °C for 20 min to form the source, drain, and gate electrodes. Then, the samples were subjected to the NH_3 or H_2 plasma treatment in a parallel-plate plasma reactor at 300°C with a power density of 0.7 W/cm^2. The plasma conditions for NH_3 and H_2 had been optimized to obtain the optimum device performance, respectively. After a plasma-enhanced CVD (PECVD) SiO_2 of a thickness about 500 nm was deposited, contact holes were opened and the Al films was deposited and then defined. The I-V curves of TFT's were measured by an HP 4145 semiconductor parameter analyzer at room temperature. The concentration of the nitrogen atom was measured by detecting the Si-N signals using a secondary ion mass spectroscopy (SIMS) with Cs^+ as the primary ion.

III. Results and Discussion

The $I_d - V_g$ characteristics of the n-channel poly-Si TFT's with various NH_3-plasma exposure times from 0 to 120 min are shown in Fig. 1. The transfer curves of the devices with a 30 min H_2-plasma and without a plasma treatment are also shown for comparison. Table I lists the values of the minimum leakage current $I_{\min}$, the subthreshold swing SS, the on/off current ratio, the threshold voltage V_{th}, the field effect mobility μ_{FE}, and the trap-state density N_t. The SS and μ_{FE} were measured at $V_d = 0.1$ V for $W/L = 40$ μm/10 μm devices. The V_{th} is defined at a fixed drain current $I_d = I_{\rm dn} \times W/L$, for this work, where $I_{\rm dn}$ is a normalized drain current, 10 nA [7]. The $I_{\min}$ is the minimum value of the drain current measured at $V_d = 5$ V. The N_t is obtained by extracting a straight line on the plot of $\ln[I_d/(V_g - V_{\rm FB})]$ versus $1/(V_g - V_{\rm FB})^2$ at low source-drain voltage and high gate bias [8], [9]. It is obvious that the NH_3-plasma and H_2-plasma treatment both can effectively promote the performance of the TFT's. In addition, it seems that the devices treated by NH_3-plasma for 30 min have even better performance than that treated by H_2-plasma. Moreover, as the exposure time to NH_3-plasma increases, the TFT's performance can be enhanced increasingly, such as $I_{\min}$ and SS decreasing to 3.54 pA, and 200 mV/decade and μ_{FE} and on/off current ratio increasing to 79.93 cm^2/Vs and 2.23×10^8, respectively, for 120 min NH_3-plasma treated devices, unlike the earlier report that the TFT's exposed to H_2-plasma exhibited saturation characteristics [10].

The hot-carrier reliability of the NH_3-plasma-treated devices was also investigated. Fig. 2 shows the μ_{FE} and $I_{\min}$ variations for the devices with the NH_3 and H_2 plasma passivation, respectively, after they were stressed at $V_d = 20$

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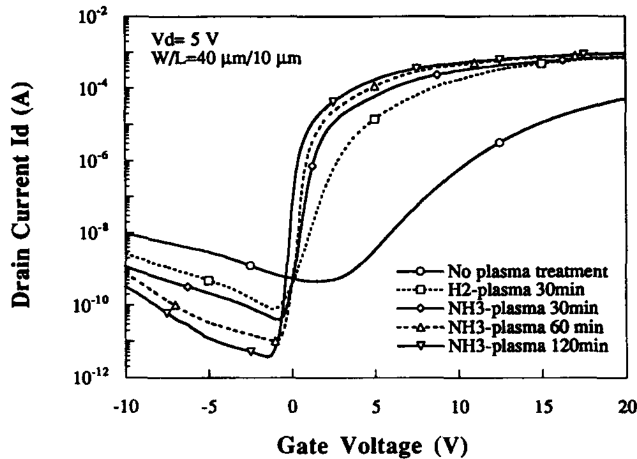

Fig. 1 The transfer characteristics of polysilicon TFT's after applying NH_3 plasma treatments.

TABLE I
THE VALUES OF $I_{\min}$, SS, μ_{FE}, V_{th}, AND N_t OF THE POLYSILICON TFT'S FOR VARIOUS PLASMA TREATMENTS

Plasma Gas	Time (min)	I_{min} (pA)	SS (V/dec.)	On/Off current ratio ($\times 10^6$)	V_{th} (V)	μ_{FE} (cm^2/Vsec)	N_t ($\times 10^{11}$ cm^{-2})
-	0	463.6	1.81	0.024	7.18	11.35	63.9
H_2	30	81.03	0.61	4.11	1.46	51.31	14.8
NH_3	30	39.50	0.34	14.2	0.72	59.92	13.9
NH_3	60	10.30	0.28	71.0	0.46	75.12	8.67
NH_3	120	3.54	0.20	223	-0.02	79.93	5.66

V, $V_g = 10$ V for different stress durations. It is found that the μ_{FE} decreases and $I_{\min}$ increases with hot-carrier stress time, and the variations of the μ_{FE} and $I_{\min}$ for NH_3-plasma-treated devices are less than those for H_2-plasma-treated samples. That is, the NH_3-plasma passivated devices have better hot-carrier reliability than the H_2-plasma ones. The performance degradation of both devices induced by hot carrier stress is thought to be due to the generation of poly-Si/SiO_2 acceptor-type interface states and the grain boundary states in the poly-Si channel layer [5], [11]. The hot-carrier endurance of NH_3-plasma passivation is better than that of the H_2-plasma passivation, suggesting that not only hydrogen atoms but also nitrogen atoms are diffusing into the poly-Si films. From the SIMS analysis, it is found that nitrogen atoms can even diffuse to the bottom of the channel region. It is possible that weak Si-H bonds in poly-Si channel and at poly-Si/SiO_2 interface had been replaced by strong Si-N bonds. It had been reported that with the nitrogen implantation in the poly-Si gate/SiO_2/c-Si substrate MOS structure, a much smaller interface-state generation rate was obtained after high-field/current stress [12]. Momose et al. also showed that with the low concentration (<1 atom %) nitrogen incorporation in the NH_3 rapid thermal nitrided-oxide, both drivability and hot carrier reliability of MOSFET could be improved [13].

Fig. 3 shows the μ_{FE} and $I_{\min}$ after thermal annealing for different annealing temperatures range from 350°C to 500°C. For the 350°C annealed devices, there is a slightly increase in μ_{FE} and a slightly decrease in $I_{\min}$. This is presumably because of the annihilation of plasma induced damages and/or hydrogen and nitrogen atoms indiffusion, leading to a further passivation effect. As the annealing

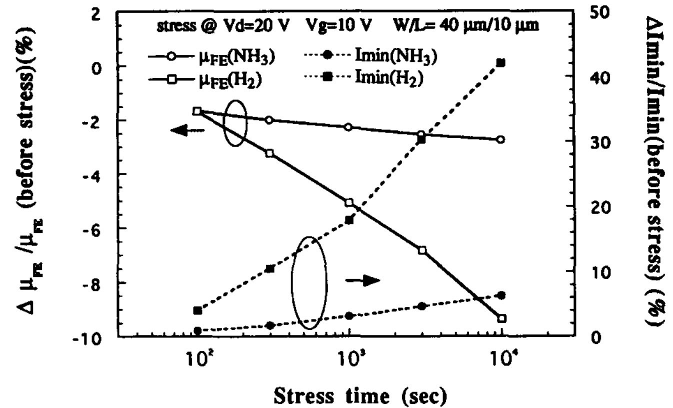

Fig. 2. The field effect mobility μ_{FE} and minimum drain current $I_{\min}$ for NH_3- and H_2-passivated devices as a function of stress time.

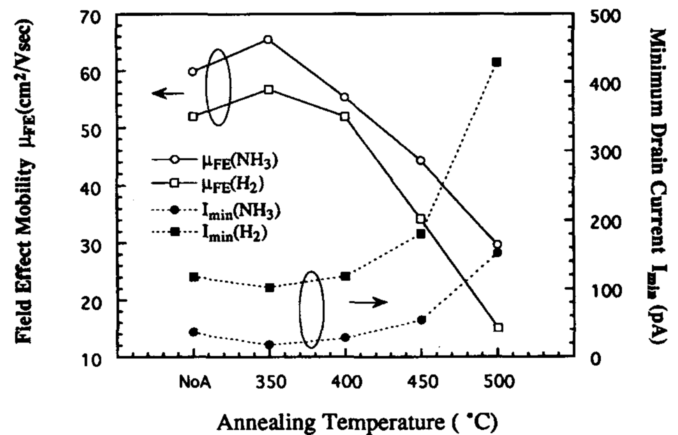

Fig. 3. The variation of field effect mobility μ_{FE} and minimum drain current $I_{\min}$ for NH_3- and H_2-passivated devices after thermal annealing at the temperature range from 300°C to 500 °C.

temperature continuously increases, the increase in $I_{\min}$ and decrease in μ_{FE} is attributed to the dehydrogenation effect since the hydrogen releases from the defect sites and causes the generation of trap states. But for the NH_3-treated TFT's, lower degrees of μ_{FE} and $I_{\min}$ degradations are observed with respect to the H $_2$-plasma ones. Even for 500°C annealing, the TFT's performance passivated with NH_3-plasma still keeps the relatively good electrical properties. Therefore, it suggests that the strong Si-N bonds exist in NH_3-passivated films and achieve superior thermal stability to weaker Si-H bonds.

IV. CONCLUSIONS

The NH_3-plasma passivation has been used to promote the electrical properties of poly-Si TFT's. It is found that the poly-Si TFT's after NH_3 plasma passivation exhibit significantly superior device characteristics, hot-carrier reliability, and thermal stability to those with the conventional H_2-plasma passivation. Both the nitrogen pile-up at the SiO_2/poly-Si interface and the strong Si-N bond formation to passivate the dangling bonds at the grain boundaries in the channel region are surmised to be the major causes.

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