Fast Transient (FT) Technique With Adaptive Phase Margin (APM) for Current Mode DC-DC Buck Converters

Yu-Huei Lee, *Student Member, IEEE*, Shao-Chang Huang, Shih-Wei Wang, and Ke-Horng Chen, *Senior Member, IEEE*

***Abstract*—This paper proposes a fast transient (FT) control with the adaptive phase margin (APM) to achieve good transient response in current-mode DC-DC buck converters at different load conditions. The overshoot/undershoot voltage and the transient recovery time are effectively reduced. The APM control can always maintain the system phase margin at an adequate value under different load conditions. That is, the compensation pole-zero pair is adapted to load current to extend the system bandwidth and get an adequate phase margin. Experimental results show the overshoot/undershoot voltage is smaller than 60 mV (3%) and transient period is smaller than 12 μs as load current suddenly changes from 100 to 500 mA, or vice versa. Compared with conventional designs without any fast transient technique, the undershoot voltage and recovery time are enhanced by 45% and 85%, respectively.**

***Index Terms*—Adaptive phase margin (APM), fast transient (FT), loop bandwidth, pole-zero cancellation, stability.**

I. Introduction

HIGH-QUALITY power management converters are demanded for portable devices such as cell phones, digital cameras, and other multimedia equipment. Voltage regulation and transient recovery time are treated as the important issues in providing a good power supply. The reason for the demand in high-quality power supply converters is that the unstable supply voltage in case of load variations may cause abnormal operation or deteriorate the performance of the portable devices. Among the applications like system-on-chip (SoC) and the motherboard, a stable power management, which features in the high-quality power supply, fast line/load transient response, and high power conversion efficiency, is the trend to increase the competitiveness of the portable products [1]. Therefore, the good transient response is the design consideration in DC-DC converter that is necessary for today's power management application.

Despite these challenges and the special design techniques, wireless USB receiver, which includes the power management module and the ultra-wide band (UWB) system as shown in Fig. 1, provides an ideal solution for wireless internet or some battery-operated portable applications. This structure allows the UWB protocol to support multiple low-power modes and data transmission. In the UWB system, if the throughput constraint is cycling between different operating modes, the power request is also changed in order to meet the supply power of different mode operations. When the UWB system enters into the data transmission period, the power request would increase suddenly that has a consequence of supply voltage variation. As depicted in Fig. 2, undershoot and overshoot voltages appear at the moment of mode transmission. The large dip supply voltage and the long voltage recovery time have a serious influence on the performance of UWB systems. Consequently, a high-quality power source is always an essential demand in the power management module design.

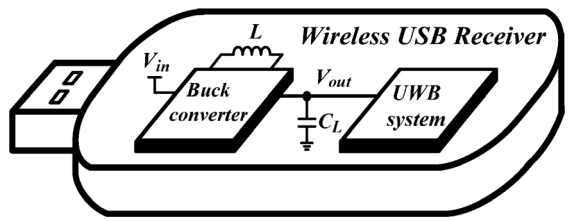


Fig. 1. Main structure of the wireless USB receiver.

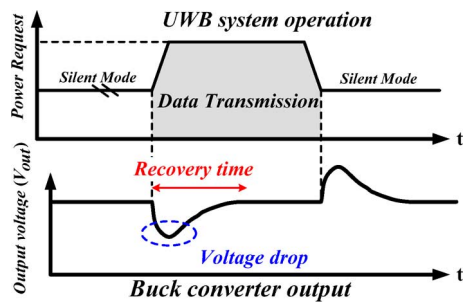


Fig. 2. Supply voltage variation under the different power request condition in UWB systems.

Several techniques are claimed to improve the transient response for getting a reliable supply voltage in DC-DC converters [2]–[10]. Some literatures in today's fast transient techniques are focused on speeding up the charging or discharging time for the large compensation capacitor [2], [3]. Thus, a large driving current is sourcing or sinking into the compensation capacitor when the load current changes. A careful design consideration of the system stability is needed to ensure a stable operation. The adaptive compensation in literature [5]

Manuscript received January 13, 2011; revised May 12, 2011; accepted July 18, 2011. Date of publication August 30, 2011; date of current version July 19, 2012. This work was also supported by the National Science Council, Taiwan, under Grant NSC 100-2220-E-009-050 and Grant NSC 100-2220-E-009-055.

The authors are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: khchen@cn.nctu.edu.tw).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2011.2163093

enhances the transient performance by deliberately adjusting the low-frequency gain to speed up the transient response in case of load current variations. The response time is decreased by raising the loop gain higher than that in steady-state to get a larger bandwidth. That is, the unstable response increases the transient voltage variation to achieve fast recovery of the output voltage. The hysteresis control can also achieve fast transient response. A fixed output frequency in ripple control scheme is proposed in [6] to solve the EMI problem in hysteresis controls. However, to get adequate noise margin for correct operation, large output voltage ripple is needed. Nevertheless, large output voltage ripple would affect the performance of the noise-sensitive circuit. Additionally, the current-mode control needs the slope compensation signal to avoid the sub-harmonic oscillation. The slope compensation signal independent of input and output can ensure a wide load range operation but has less help in accelerating the transient response [7]. The digital control methods [11]–[13] are also a wide-used mechanism in DC-DC converter for getting fast response. However, deteriorated performance and high cost are derived from the function of analog-to-digital converter. Moreover, there are different control methods in DC-DC buck converters [14]–[18]. These different control schemes achieve the good transient response but increases the design complexity.

In this paper, a fast transient with adaptive phase margin (APM) control is proposed in the current-mode DC-DC buck converters. The conventional compensation technique in DC-DC buck converters is presented in Section II. Fast transient control procedure with proposed APM is illustrated in Section III. Circuit implementations are described in Section IV. Experimental results are shown in Section V. Finally, a conclusion is made in Section VI.

II. Compensation Techniques in Voltage-Mode and Current-Mode DC-DC Buck Converters

There are some different design issue of compensation techniques between voltage and current mode DC-DC buck converters. Voltage-mode buck converter needs proportional-integral-differential (PID) compensator due to the LC dual poles, ω_{ps} and ω'_{ps}, as illustrated in Fig. 3(a) and the frequency response depicted in Fig. 3(b). The transfer function of the power stage $G_{pt}(\mathrm{s})$ is written as (1). The usage of a PID compensator in voltage-mode buck converters can enhance low-frequency gain and phase margin (PM). The PID compensator generates three poles and two zeros. One of the three poles is located at the origin as the system dominant pole to stabilize system and the other two poles are located at high-frequencies. These high-frequency poles are placed above the system crossover frequency. Those poles will not affect the system stability and can help minimize the effect of high-frequency noise. The two compensation zeros, ω_{z1} and ω_{z2}, are used to compensate the effects of the dual non-dominant poles. The PID compensator $H_{ea}(\mathrm{s})$ as depicted in Fig. 3(a) is expressed as (2) based on the assumption of $R_2 \gg R_3$ and $C_8 \gg C_7$. The PM is approximated to 60 degrees in case of load variations. However, the complexity of compensation and the need of many external passive components is the major disadvantage in the design of voltage-mode buck converters, as shown in (1)–(3) at the bottom of the page.

The compensation scheme of the current-mode buck converter is simpler than that of the voltage-mode control owing to the single pole at the power stage. That is, the proportional-integral (PI) compensator with a pole-zero pair is eligible to achieve system compensation. The compensation zero ω_z is usually used to cancel the load-dependent system pole ω_{ps} located at the output. However, the position of ω_z would affect the performance of the current-mode buck converter under the different load condition. The PI compensator, which generates a fixed compensation pole-zero pair, can ensure the system stability but cannot ensure a good transient response at any load conditions.

As shown in Fig. 4(a), ω_z is designed to cancel ω_{ps} at heavy loads. When load current changes from heavy to light, ω_{ps} moves toward the origin due to its characteristic of load dependence. The PM would deteriorate since the compensation zero cannot be moved back to cancel the system pole at light loads. It might suffer the ringing problem and the long settling time resulting from the insufficient PM in transient period. Moreover, when ω_z is designed to cancel the system pole at light loads as depicted in Fig. 4(b), the PM becomes larger than the optimal value. It has opposite performance to the requirement of fast transient response at heavy loads. The system is always stable but carries out the slow transient response because of the large PM.

Therefore, an adaptive compensation zero is needed in the current-mode buck converter to ensure large system bandwidth and adequate PM at any load conditions. The compensation zero should be located at low frequencies to cancel the effect of the system pole at light loads and be moved toward high frequencies

$$G_{pt}(s)=\left(\frac{R_{\mathrm{Load}}}{R_{Load}+R_{\mathrm{DCR}}}\right)V_{in}\times\frac{(1+sR_{\mathrm{ESR}}C_{\mathrm{Load}})}{\left\{1+s\left[C_{\mathrm{Load}}\left(R_{\mathrm{ESR}}+(R_{\mathrm{Load}}\|R_{\mathrm{DCR}})\right)+\frac{L}{R_{\mathrm{Load}}+R_{\mathrm{DCR}}}\right]+s^2LC_{\mathrm{Load}}\frac{R_{\mathrm{Load}}+R_{\mathrm{ESR}}}{R_{\mathrm{Load}}+R_{\mathrm{DCR}}}\right\}} \tag{1}$$

$$H_{ea}(s)=\left(\frac{1}{sR_2C_8}\right)\frac{(1+sR_5C_8)(1+sR_2C_6)}{(1+sR_3C_6)(1+sR_5C_7)} \tag{2}$$

where

$$\omega_{p1}=0,\quad \omega_{p2}=\frac{1}{R_3C_6},\quad \omega_{p3}=\frac{1}{R_5C_7},\quad \omega_{z1}=\frac{1}{R_5C_8},\quad \omega_{z2}=\frac{1}{R_2C_6} \tag{3}$$

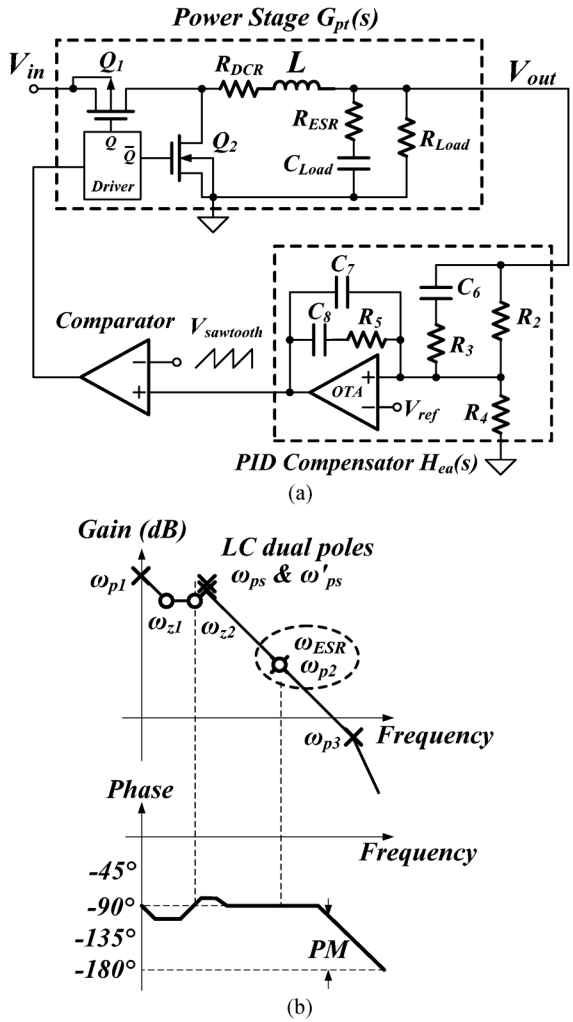


Fig. 3. (a) Compensation network in the design of the voltage-mode DC-DC buck converter. (b) Frequency response.

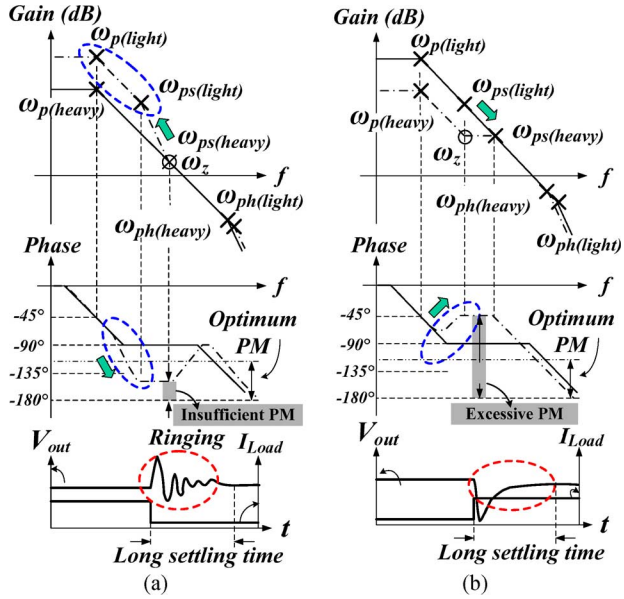


Fig. 4. Different positions of ω_Z in steady state. (a) ω_Z designed at high frequencies to cancel ω_{ps} at heavy loads, causes the PM worse at light loads. (b) ω_Z designed at low frequencies to cancel ω_{ps} at light loads, causes the PM larger than the optimum PM.

to cancel the effect of the system pole at heavy loads. During the load transient period, the dip output voltage depends on the ESR value of output capacitor and the system bandwidth. However, the voltage drop across the ESR is a material-related value. To maintain a large system bandwidth and adequate PM is therefore an effective way to enhance the power management module. Therefore, the proposed fast transient with APM control technique can achieve the fast and smooth load transient response through the control of compensation pole-zero pair.

III. Proposed Fast Transient Control Procedure With APM

The control-to-output transfer function of the conventional current mode DC-DC buck converter has two separated real poles, ω_{ps} and ω_{ph}, [19], [20]. ω_{ps} is located at the output of the regulator, that is, $\omega_{ps} = 1/(C_L R_L)$ where C_L is the output filter capacitor and load resistance R_L is inversely proportional to load current I_{load}. The output pole ω_{ps} is therefore proportional to the value of load current $I_{\rm load}$. Besides, the high-frequency pole ω_{ph} is located near the switching frequency region because of the characteristic of the current programmed control. It pushes the inductor-resulted pole to a high-frequency position to separate the double pole at output stage. The compensation method only needs to increase the low-frequency loop gain using the PI compensation to improve transient regulation performance.

The transfer function of an equivalent PI compensation technique proposed by [2] is given as (4). ω_p and ω_z are expressed in (5), where R_z and C_p are on-chip small compensation resistor and capacitor, respectively. R_o is the output resistance of the error amplifier (EA) and its value is much larger than that of R_z. G_m is the transconductance of the OTA [21]. K is the capacitor multiplier factor

$$T(s) \approx -G_m R_o \frac{1 + sKC_pR_z}{1 + sKC_p(R_z + R_o)} \tag{4}$$

$$\omega_p = \frac{1}{KC_p(R_z + R_o)} \qquad \omega_z = \frac{1}{KC_pR_z}. \tag{5}$$

A low-frequency pole-zero pair, ω_p and ω_z, can effectively compensate the current-mode DC-DC buck converter. This is because that the current generated by EA can be redirected to charge or discharge the small on-chip capacitor in compensation network for on-chip compensation. Moreover, the fast transient mechanism can be simultaneously achieved in case of load current variation [22].

Fig. 5 shows the proposed structure of the fast transient control with the APM technique in a current-mode buck converter. An adaptive compensation resistance R_z can achieve the APM technique to get the adequate system phase margin under different load conditions. In addition, an adaptive compensation capacitance C_c is implemented to further achieve fast and smooth transient response. As the fast transient technique in [2], the one-shot control is used to decide the duration of the fast transient period. However, it suffers from an oscillation problem when the positive feedback gain is larger than one.

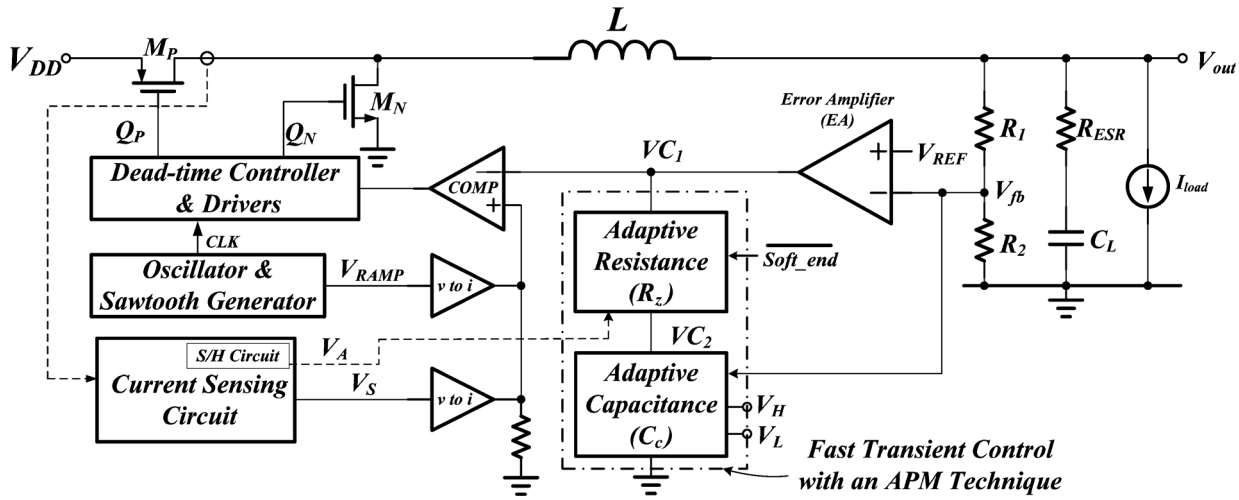


Fig. 5. Proposed compensation circuit is composed of the adaptive capacitance C_c and resistance R_z in current-mode buck converter.

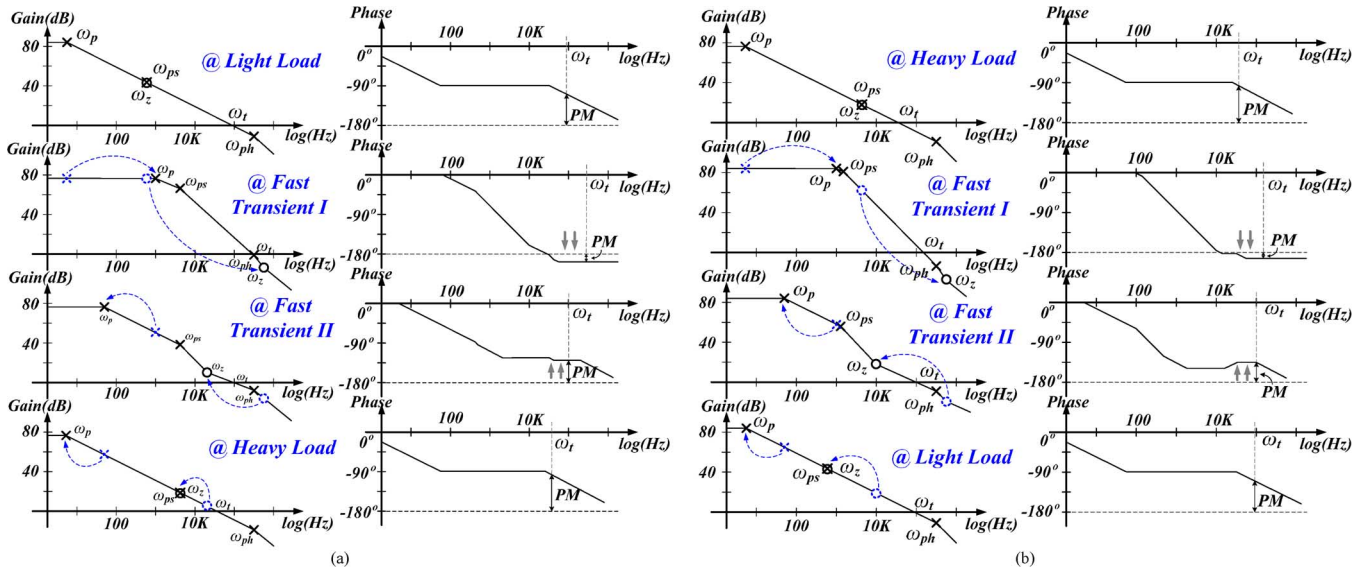


Fig. 6. Frequency response of the proposed current-mode buck converter at different loads. (a) The positions of ω_{ps}, ω_p, and ω_z when load current changes from light to heavy. (b) The positions of ω_{ps}, ω_p, and ω_z when load current changes from heavy to light.

Thus, the proposed adaptive compensation technique contains four steps to complete the fast transient response. The frequency response expression of the fast transient with APM control is shown in Fig. 6. At first, the system is in steady-state and waits for the occurrence of load transient response. When load current changes from light to heavy as depicted in Fig. 6(a), ω_p and ω_z are moved toward high frequencies to improve the transient response because of the small equivalent compensation capacitance and large system bandwidth. It is different from the technique proposed in [2] since ω_z is controlled by output voltage and current at the same time. ω_z is at lower frequencies than that of $\omega_{z(\mathrm{old})}$ in the previous design [2] to derive a large system bandwidth. After the fast transient I (FTI) period, ω_p and ω_z start to move back to the position in steady state when the transient procedure enters the fast transient II (FTII) to alleviate the oscillation problem. At this time, ω_p and ω_z still position at high frequencies to get a fast recovery time. Finally, ω_p and ω_z are moved back to the position in steady state.

Owing to the adaptive R_z with the ability to adjust the resistance in the PI compensator, the position of ω_z is no longer similar to that $\omega_{z(\mathrm{old})}$ in [2] because it reaches the position of ω_{ps} at heavy loads to achieve nearly exact pole-zero cancellation. Due to the pole-zero cancellation generated by the proposed adaptive compensation capacitance and resistance circuit, not only the system bandwidth can be magnified but also PM can be maintained a suitable value, which is near 60 degrees, to wait for load variations in steady state. On the other hand, ω_{ps} is located at high frequencies at heavy loads. Therefore, when load current changes from heavy to light as illustrated in Fig. 6(b), ω_p and ω_z are moved toward to high frequencies during the FTI. After FTI, ω_p and ω_z start to move back toward the origin during the FTII. Finally, at the end of transient response, ω_z is located at a low frequency position, which is close to the system pole at light loads, to achieve nearly exact pole-zero cancellation. Obviously, the proposed fast transient control with an APM can improve the transient response time during the transient period.

Besides, PM in steady state can be improved due to the nearly exact pole-zero cancellation. PM can be kept a suitable value to ensure the system stability at any loads.

Moreover, the performance of load transient response in the current-mode buck converter is determined by the output impedance and the loop crossover frequency. The load transient response of power management module can be evaluated by the transient dip voltage and the settling time, which can be indicated by the closed-loop output impedance. The accurate model of the current programmed control buck converter has been presented in [23]. The open-loop output impedance $Z(s)_{\text{open}}$ can be shown as (6)

$$Z(s)_{\text{open}} \approx \frac{R_L}{1+\frac{R_L T_S}{L}(m_C D' - 0.5)} \cdot F_p(s)$$

where

$$F_p(s) = \frac{1+sC_L R_{\text{ESR}}}{1+\frac{s}{\omega_p}} \qquad \omega_p = \frac{1}{C_L R_L}. \tag{6}$$

T_S is the switching cycle of the buck converter. m_C is the compensation slope. D' is the complement of duty cycle ($D' = 1 - D$). Besides, based on the proposed structure depicted in Fig. 5, the transfer functions of EA, the adaptive compensation resistance circuit, the adaptive compensation capacitance circuit, and the control to output voltage gain G_{vc} can be merged as a factor A shown in (7). $G_{vc}(s)$ represents the transfer function of the power stage in current-mode buck converter. In addition, the voltage divider at the output node of buck converter is considered as the feedback factor β expressed in (8). Therefore, the closed-loop output impedance can be shown in (9)

$$A(s) = G_m R_o \frac{1+sKC_pR_z}{1+sKC_p(R_z+R_o)} G_{vc}(s) \tag{7}$$

$$\beta = \frac{R_2}{R_1+R_2} \tag{8}$$

$$\begin{aligned} Z(s)_{\text{closed}} &= \frac{Z(s)_{\text{open}}}{1+A(s)\beta} \\ &\approx \frac{\frac{R_L}{1+\frac{R_L T_S}{L}(m_C D'-0.5)} \cdot \frac{1+sC_L R_{\text{ESR}}}{1+sC_L R_L}}{1+G_m R_o \frac{1+sKC_pR_z}{1+sKC_p(R_z+R_o)} G_{vc}(s) \cdot \frac{R_2}{R_1+R_2}}. \end{aligned} \tag{9}$$

Fig. 7 shows the output impedance of the current mode buck converter with conventional method, the APM technique, and the proposed FT control with the APM technique. The load transient response can be explained by the closed-loop output impedance in three different frequency regions. The closed-loop output impedance in high-frequency region can indicate voltage drop in the beginning of transient response. That is, the initial dip voltage in load transient response is the consequence of the closed-loop output impedance derived near the loop crossover frequency. As shown in Fig. 7 in high-frequency region, the closed-loop output impedance of both the APM technique and the FT control with APM technique are almost equivalent with a smaller value than that of the conventional method. Smaller closed-loop output impedance at the loop crossover frequency would come to a smaller transient dip voltage. Consequently, the transient voltage drop of the proposed FT control with the APM technique can be smaller than that of the conventional

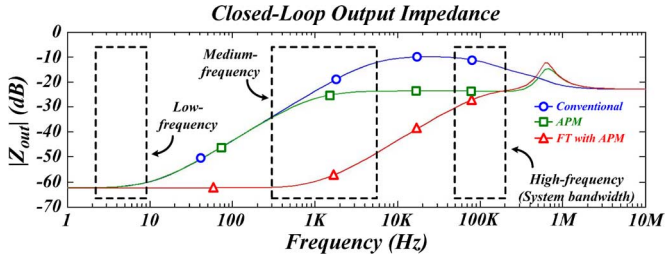


Fig. 7. Closed-loop output impedance of the buck converter with different control techniques.

method owing to the smaller closed-loop output impedance at the loop crossover frequency. The closed-loop output impedance $Z(s)_{\text{closed\_}H}$ in the high-frequency region near the crossover frequency is shown in (10) simplified from (9), which is proportional to the ratio between the output resistance of EA R_o and the compensation resistance R_z

$$\begin{aligned} Z(s)_{\text{closed\_}H} &\propto \frac{1}{\frac{sKC_pR_z}{sKC_p(R_z+R_o)}} \text{ (at high frequencies)} \\ &= \frac{sKC_p(R_z+R_o)}{sKC_pR_z} \\ &= \frac{(R_z+R_o)}{R_z} \xrightarrow{\text{if } R_o \gg R_z} \frac{R_o}{R_z}. \end{aligned} \tag{10}$$

In medium-frequency region of the closed-loop output impedance shown in Fig. 7, the proposed FT control with the APM technique also derives the smallest output impedance compared to those of the conventional method and the technique with APM only. The settling time in load transient response is also affected by the closed-loop output impedance within the loop crossover frequency. Smaller closed-loop output impedance would achieve shorter transient settling time. Therefore, the proposed FT control with the APM technique can derive the shortest settling time compared to the other control methods.

Moreover, the closed-loop output impedance $Z(s)_{\text{closed\_}M}$ in the medium-frequency region can be simplified as (11) from (9). $Z(s)_{\text{closed\_}M}$ is influenced by R_o, R_z, and C_c

$$\begin{aligned} &Z(s)_{\text{closed\_}M} \\ &\quad \propto \frac{1}{\frac{1+sKC_pR_z}{1+sKC_p(R_z+R_o)}} \text{ (at medium frequnecies)} \\ &\quad = \frac{1+sKC_p(R_z+R_o)}{1+sKC_pR_z} \xrightarrow{R_o \gg R_z} \frac{1+sKC_pR_o}{1+sKC_pR_z}. \end{aligned} \tag{11}$$

In the low-frequency region, the value of the output impedance is equivalent to the others. It indicates that the proposed technique would not affect the steady-state error. As a result, the proposed FT control with the APM technique can adjust the adaptive compensation capacitance and resistance to get smaller closed-loop output impedance, which carries out smaller transient dip voltage and transient settling time in the current-mode buck converter.

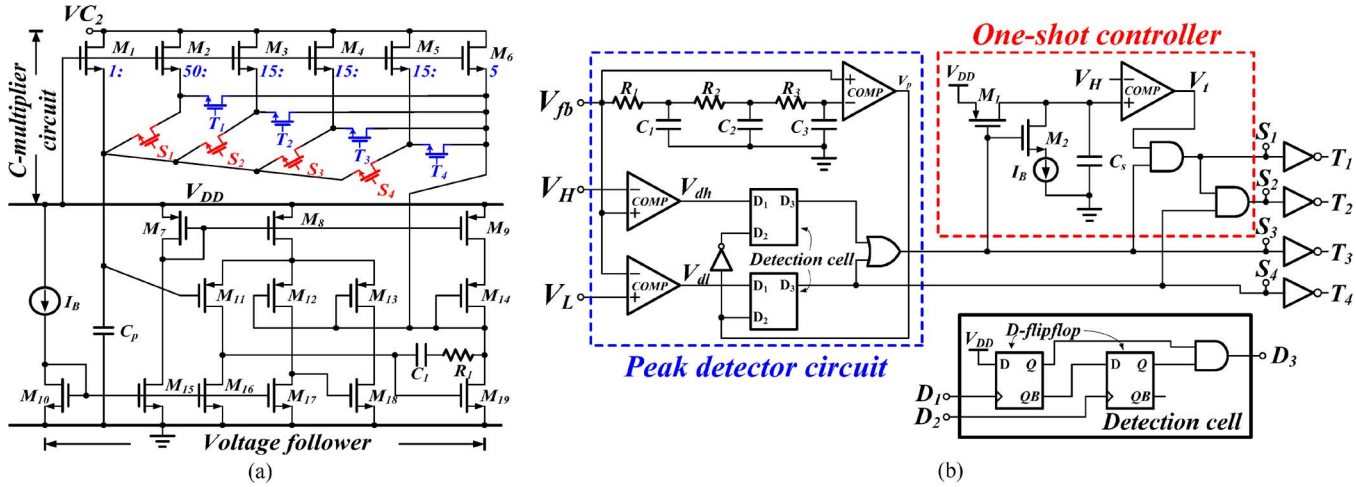


Fig. 8. Implementation of the adaptive compensation C_c circuit. (a) The schematic of the adaptive compensation capacitance. (b) One-shot controller decides the first fast-transient period and the peak detector decides the second fast-transient period.

IV. Circuit Implementations

A. Adaptive Compensation Capacitance C_c

The adaptive capacitance circuit can automatically adjust the value of compensation capacitance C_c by controlling the current flowing through the small capacitor C_p as shown in Fig. 8(a). As a result, the capacitor C_p can be amplified to an optimum value for system compensation in steady-state or adjusted to a small value in load transient period to accelerate the system response [22], [24]–[26].

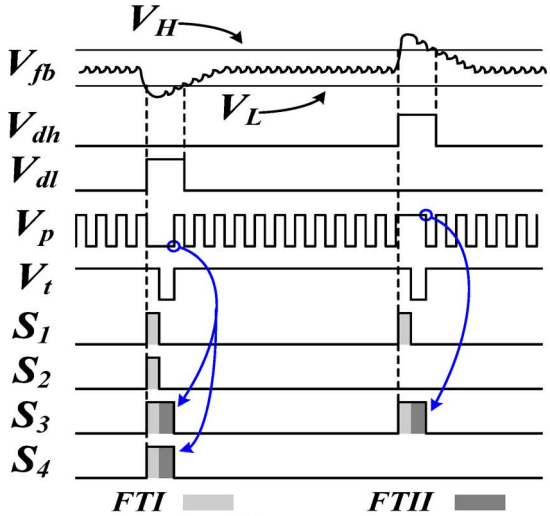
The operation of the adaptive capacitance circuit is separated into four steps. *Step 1* is in steady-state. Switches $S_1 \sim S_4$ are opened ($T_1 \sim T_4$ are closed) so that the current flowing through transistors $M_2 \sim M_6$ can not flow into the small on-chip capacitor C_p. It acts as a current source parallel with the current flowing through C_p to achieve the on-chip compensation [2]. The function of the adaptive capacitance circuit in this step is to maintain a large on-chip compensation capacitance. Besides, peak detector circuit and one-shot controller shown in Fig. 8(b) are used to control the fast transient operation. The low-pass filter in the peak detector circuit can react the feedback voltage variation to the oscillating signal V_p, which is utilized to determine the duration of fast transient response according to different load current steps. The larger load step will lead to the longer transient period. Thus, when the feedback voltage V_{fb} is larger than the high threshold voltage V_H or smaller than the low threshold voltage V_L, the fast transient mechanism would be activated. The fast transient period contains two steps, which are *step 2* named as FTI and *step 3* named as FTII.

In *step 2* (or FTI), V_{dh} or V_{dl} in the peak detector circuit are set to high to trigger the detection cell, which is composed of two D-flip-flops, to enable the one-shot controller. The control time diagram of the adaptive compensation capacitance C_c circuit is shown in Fig. 9(a). The switches $S_1 \sim S_4$ are closed and $T_1 \sim T_4$ are opened when the load current changes from light to heavy (S_1, S_3, T_2, and T_4 are closed but S_2, S_4, T_1, and T_3 are opened when the load changes from heavy to light). That is, a large current would directly inject into the small on-chip capacitor C_p at this period. Thus, the equivalent capacitance value of the adaptive capacitance C_c is decreased in order to accelerate the transient response.

At the end of the one-shot period, V_t is set to high and the fast transient response enters *step 3* (or FTII). Switches S_1 and S_2 are opened but S_3 and S_4 are still closed (T_1 and T_2 are closed; T_3 and T_4 are opened) when the load current changes from light to heavy (S_3, T_1, T_2, and T_4 are closed but S_1, S_2, S_4, and T_3 are opened when the load changes from heavy to light). The current flowing into the small on-chip capacitor C_p is less than that in *step 2*. Hence, the equivalent value of the adaptive capacitance C_c becomes larger than that in *step 2*, so that the compensation zero ω_z is pulled toward the origin to increase the PM and stabilize the system.

Finally, V_p would send an edge trigger to the detection cell to end the fast transient operation. The positive or negative trigger of V_p is generated when output voltage is returned back from the undershoot or overshoot, respectively. The period of the fast transient control, which is determined by the low-pass filter in the peak detector circuit, is proportional to the output load transient condition. When the operation enters into *step 4* of steady-state, switches $S_1 \sim S_4$ are opened ($T_1 \sim T_4$ are closed) and the adaptive capacitance C_c is again amplified to a large capacitance. Accompanied with an adaptive resistance R_z, which has a small value at heavy loads or a large value at light loads, the nearly exact pole-zero cancellation is achieved in order to extend the system bandwidth and PM. The states of these eight switches in fast transient period are shown in Fig. 9(b) and (c).

Two-stage fast transient operation in *step 2* and *step 3* has these advantages. 1) The system can be stabilized since the PM in *step 3* is better than that in *step 2* owing to the larger compensation capacitance. 2) The output voltage $V_{\rm out}$ can be smoothly regulated back to its steady-state value with little overshoot and undershoot because of the smooth control of compensation pole-zero pair. 3) The low-pass filter in peak detector circuit achieves the load-dependent control of adaptive capacitance C_c circuit that would dynamically determine the fast transient period according to different load current condition. Moreover, the predefined voltage V_H and V_L in the peak detector circuit of Fig. 8(b) is derived from the bandgap reference.



(a)

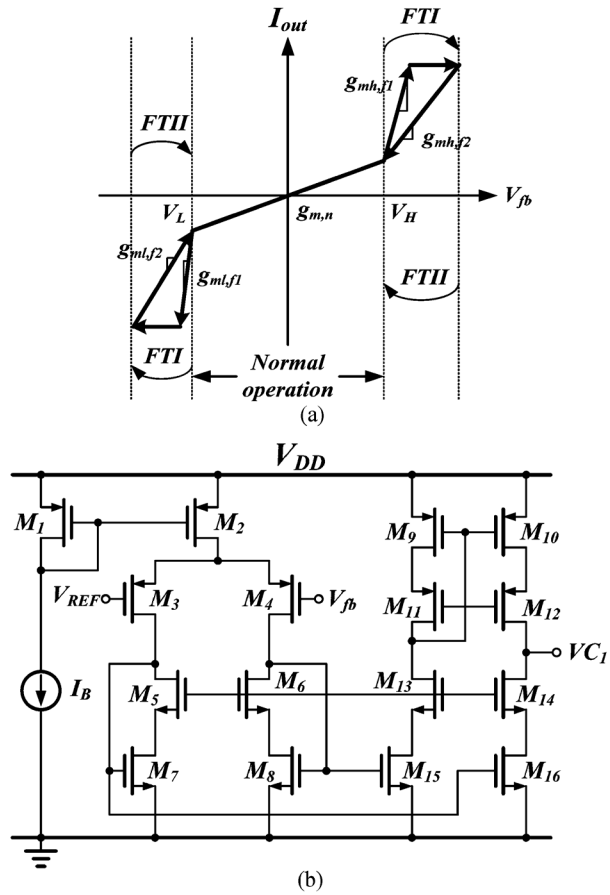
Period \ Switch	$S_1(T_1)$	$S_2(T_2)$	$S_3(T_3)$	$S_4(T_4)$
Light Load	Off (On)	Off (On)	Off (On)	Off (On)
Fast Transient I	On (Off)	On (Off)	On (Off)	On (Off)
Fast Transient II	Off (On)	Off (On)	On (Off)	On (Off)
Heavy Load	Off (On)	Off (On)	Off (On)	Off (On)

(b)

Period \ Switch	$S_1(T_1)$	$S_2(T_2)$	$S_3(T_3)$	$S_4(T_4)$
Heavy Load	Off (On)	Off (On)	Off (On)	Off (On)
Fast Transient I	On (Off)	Off (On)	On (Off)	Off (On)
Fast Transient II	Off (On)	Off (On)	On (Off)	Off (On)
Light Load	Off (On)	Off (On)	Off (On)	Off (On)

(c)

Fig. 9. Control scheme of the adaptive compensation C_c circuit. (a) Time diagram of the one-shot controller and peak detector circuit. (b) The status of the eight switches when load current changes from light to heavy. (c) The status of the eight switches when load current changes from heavy to light.



(a)

(b)

Fig. 10. (a) Transconductance of the transconductance amplifier with an auxiliary gain stage for the on-chip capacitor C_p. (b) The schematic of EA.

TABLE I
TRANSCONDUCTANCE COEFFICIENTS OF EA WITH AN AUXILIARY GAIN STAGE

Load changes from light load to heavy load *(k=100)*	
m_l=0.65	n_l=0.3
$g_{ml,f1}=96g_{m,n}$	$g_{ml,f2}=31g_{m,n}$
Load changes from light load to heavy load *(k=100)*	
m_h=0.5	n_h=0.15
$g_{mh,f1}=66g_{m,n}$	$g_{ml,f2}=16g_{m,n}$

Due to the implementation of auxiliary switches as depicted in Fig. 8(a), the value of on-chip compensation capacitance can be adjusted in the FT period. It can be considered that the transconductance of EA would be varied at the different periods of the FT response since the value of compensation capacitance, which is changed with a constant-biasing EA, is derived in the FT period. As shown in Fig. 10(a), the transconductance of EA with an auxiliary gain stage for the on-chip capacitor C_p is increased from $g_{m,n}$ to $g_{mh,f1}$, $g_{mh,f2}$, $g_{ml,f1}$ and $g_{ml,f2}$, respectively. The $g_{m,n}$ is the steady-state transconductance of EA. Once the system enters into fast transient of *step 2*, the value of the equivalent transconductance becomes $g_{mh,f1}$ and $g_{ml,f1}$ since the load changes from heavy to light or from light to heavy, which is expressed as (12). Similarly, the equivalent transconductance of the *step 3* is derived as (13). When load current changes from heavy to light, the multiplier factors $[1+(m_h+n_h)k]$ and $(1+n_hk)$ define the amplified factors in FTI and FTII, respectively. On other hand, when load current changes from light to heavy, the multiplier factors $[1+(m_l+n_l)k]$ and $(1+n_lk)$ define the amplified factors in FTI and FTII, respectively. k is the entire capacitance multiplier factor in the adaptive compensation capacitance circuit. The schematic of the EA in the proposed structure is depicted in Fig. 10(b). The coefficients in (12) and (13) are listed in Table I

$$\begin{aligned} g_{mh,f1} &= g_{m,n} + g_{m,n} \times (m_h + n_h)k \\ &= g_{m,n}\,[1 + (m_h + n_h)k] \\ g_{ml,f1} &= g_{m,n} + g_{m,n} \times (m_l + n_l)k \\ &= g_{m,n}\,[1 + (m_l + n_l)k] \end{aligned} \tag{12}$$

$$g_{mh,f2} = g_{m,n} + g_{m,n} \times n_h k = g_{m,n}(1 + n_h k)$$

$$g_{ml,f2} = g_{m,n} + g_{m,n} \times n_l k = g_{m,n}(1 + n_l k). \tag{13}$$

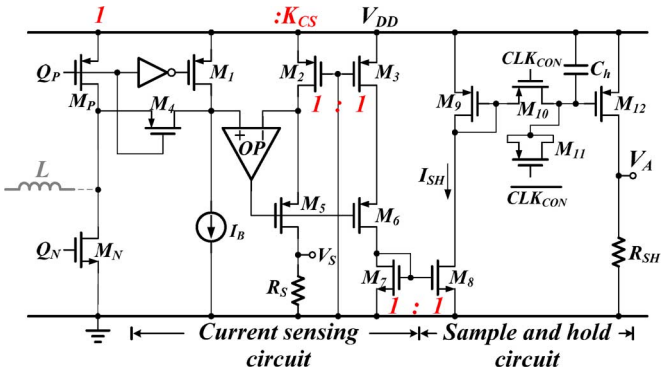


Fig. 11. Current sensing circuit with the SH circuit.

In order to prevent the converter from oscillating and ensure the system stability, a conservative value of the time duration is used to design first step pulse in FTI period to decrease output overshoot/undershoot. Since the APM technique, the adaptive resistance R_z at light loads is larger than that at heavy loads. Hence, the adaptive capacitance C_c should be decreased to a smaller value when the load changes from light to heavy than that when the load changes from heavy to light. Therefore, $g_{ml,f1}$ and $g_{ml,f2}$ should be larger than $g_{mh,f1}$ and $g_{mh,f2}$, respectively.

B. Current Sensing With Sample-and-Hold Circuit

According to the theorem of current mode control, the system pole ω_{ps} at output node is inversely proportional to load resistance. In other words, the position of ω_{ps} is proportional to the load current. The current sensing circuit with a sample-and-hold (SH) circuit [27] as depicted in Fig. 11 is used to derive the value of load current, and thereby moving the position of the compensation zero ω_z to the position where ω_{ps} locates. When the signal Q_P changes from high to low, the power p-MOSFET M_P is turned on to deliver energy from power source to the inductor and the output. Simultaneously, the transistor M_4 is also turned on to connect the drain of M_P to the non-inverting input of the op-amp. Thus, the transistors M_2 and M_3 can sense the current flowing through the power p-MOSFET M_P. The current flows through M_2 is used to generate the sensing voltage V_S for the operation of current-mode DC-DC buck converter. On other hand, the current that flows thorough M_3 is mirrored by the current mirror pair M_7 and M_8 to generate a current I_{SH} to the SH circuit. When the signal of $\mathrm{CLK_{CON}}$ is triggered from high to low, the sensing current I_{SH} is averaged by the SH circuit and thus the value of average inductor current can be derived by the signal V_A.

Furthermore, in order to alleviate the effects of clock shoot-through and charge injection, a complement transistor M_{11} is connected as a dummy switch and controlled by the signal $\overline{\mathrm{CLK_{CON}}}$. Owing to the current sensing circuit, the value of the sensing current, which is scaled down to K_{cs} times that of load current, is sampled and averaged by the SH circuit. After the I-V conversion across the resistor R_{SH}, the averaged inductor current value is converted to V_A as shown in (14)

$$V_A = K_{cs} \times I_{\mathrm{load}} \times R_{SH} \text{ where } K_{cs} \text{ is a constant.} \quad (14)$$

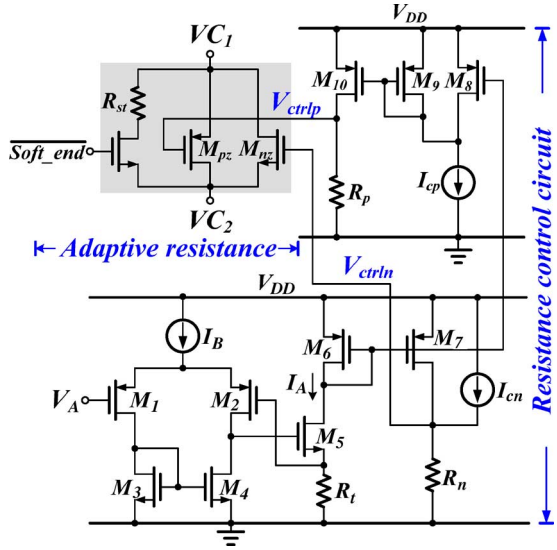


Fig. 12. Adaptive resistance control circuit.

C. Adaptive Compensation Resistance R_z

The position of the compensation zero ω_z is inversely proportional to the product of the compensation resistance and capacitance. To get an adequate PM at any load condition, ω_z needs to be adjusted adaptively to track the output load condition. As illustrated in Fig. 12, an adaptive resistance control circuit is used to derive the load-dependent compensation zero ω_z for the cancellation of the output pole ω_{ps}. The control signal V_A generated from the current sensing with a SH circuit indicates the averaged inductor current and can be used to control the position of ω_z to achieve a nearly exact pole-zero cancellation at different load condition. However, this adaptive resistance control circuit would not work properly with the uncertainty load condition during the start-up period. Thus, a small resistor R_{st} is designed to place parallel with the transistors M_{pz} and M_{nz} to eliminate this scenario.

When the start-up period ends, the signal $\overline{\mathrm{Soft\_end}}$ will be set to low to disconnect the current flowing through the resistor R_{st}. The parallel MOSFETs M_{pz} and M_{nz} are operated in deep triode region as the equivalent resistances R_{zp} and R_{zn}, which have their values determined by the gate controlling signals V_{ctrlp} and V_{ctrln}. These gate controlling signals are generated by the resistance control circuit in Fig. 12. V_A in (14) indicates the load condition, and thereby being used to adjust the position of ω_z. V_A is converted to a current I_A as expressed in (15) through the voltage-to-current (V-I) structure and utilized in the determination of V_{ctrlp} and V_{ctrln} in (16) and (17). Two constant currents, I_{cp} and I_{cn}, are generated to ensure the deep triode operation of the MOSFETs M_{pz} and M_{nz}. Therefore, the equivalent resistances R_{zp} and R_{zn} can be determined in (18) and (19), respectively

$$I_A = G_m V_A = \frac{V_A}{R_t} \quad (15)$$

$$V_{\mathrm{ctrlp}} = (I_{cp} - I_A)R_p = I_{cp}R_p - \frac{R_p}{R_t}V_A \quad (16)$$

$$V_{\mathrm{ctrln}} = (I_{cn} + I_A)R_n = I_{cn}R_n + \frac{R_n}{R_t}V_A \quad (17)$$

$$R_{zp} = \frac{1}{K_{pz}\left(VC_1 - V_{\text{ctrlp}} - |V_{tpz}|\right)} = \frac{1}{K_{pz}\left[VC_1 - \left(I_{cp}R_p - \frac{R_p}{R_t}V_A\right) - |V_{tpz}|\right]} \quad (18)$$

$$R_{zn} = \frac{1}{K_{nz}(V_{\text{ctrln}} - VC_2 - V_{tnz})} = \frac{1}{K_{nz}\left[\left(I_{cn}R_n + \frac{R_n}{R_t}V_A\right) - VC_2 - V_{tnz}\right]}. \quad (19)$$

V_{tpz} and V_{tnz} are the threshold voltages and K_{pz} and K_{nz} are the products of the mobility and aspect ratio of the transistors M_{pz} and M_{nz}, respectively. An equivalent resistance R_z, which determines the position of ω_z, is equal to the value of $R_{zp}\|R_{zn}$. Assuming that VC_1 and VC_2 have the similar value in steady-state operation, the inverse value of the equivalent resistance R_z in (20) is proportional to the load condition to achieve the compensation zero adjustment. Hence, the exact expression of the compensation zero can be derived in (21). The effects of the output pole ω_{ps} on the PM can be effectively alleviated due to the tracking of the compensation zero ω_z

$$\frac{1}{R_z} = \frac{1}{R_{zp}} + \frac{1}{R_{zn}} \xrightarrow{VC_1 \simeq VC_2}$$
$$\frac{1}{R_z} \approx K_{nz}(V_{\text{ctrln}} - V_{tnz}) - K_{pz}\left(V_{\text{ctrlp}} + |V_{tpz}|\right) = DV_A + E$$

where

$$D = K_{nz}\frac{R_n}{R_t} + K_{pz}\frac{R_p}{R_t} \approx 4.6\ \mu$$

and

$$E = K_{nz}(I_{cn}R_n - V_{tnz}) - K_{pz}\left(I_{cp}R_p + |V_{tpz}|\right) \approx 0.14\ \mu \quad (20)$$

$$\omega_z = \frac{1}{R_z C_c} = \frac{DV_A + E}{C_c} = D'\frac{I_{load}}{C_c} + E'$$

where

$$D' = \left(K_{nz}\frac{R_n}{R_t} + K_{pz}\frac{R_p}{R_t}\right)K_{cs}R_{SH} \approx 9.2\ \mu$$

and

$$E' = \frac{\left[K_{nz}(I_{cn}R_n - V_{tnz}) - K_{pz}\left(I_{cp}R_p + |V_{tpz}|\right)\right]}{C_c} \approx 750. \quad (21)$$

Fig. 13 is the simulation result of the adaptive R_z circuit. The gate control signals, V_{ctrlp} and V_{ctrln}, would be modulated according to the load-dependent signal V_A. The resistance R_z would be inverse proportional to the load current to achieve the adaptive compensation. Table II lists the locations of the dominant pole ω_p, the output pole ω_{ps} and the compensation zero ω_z during the load transient period between 100 and 500 mA. These movements are achieved through the proposed adaptive compensation technique. Moreover, to implement the transistors M_{pz} and M_{nz} in parallel can deal with the sudden load variations. When load current I_{load} changes from light to heavy rapidly, the output node of error amplifier VC_1 can be raised to a higher voltage level immediately. It results in a large voltage difference between nodes VC_1 and VC_2, and thereby pushing the transistor M_{nz} into the saturation region. The equivalent resistance across transistor M_{nz} would become very large. Fortunately, the transistor M_{pz} still operate in deep triode region as a linear resistance that the compensation zero can be held properly in order to prevent the oscillation problem. Similarly, the transistor M_{pz} may operate in the saturation region at the beginning of transient response due to the instant decrease at node VC_1. However, transistor M_{nz} can still work in the deep triode region to form an adaptive compensation resistance R_z for the adaptive compensation. It is obvious that the fast transient control and the nearly exact pole-zero cancellation are achieved.

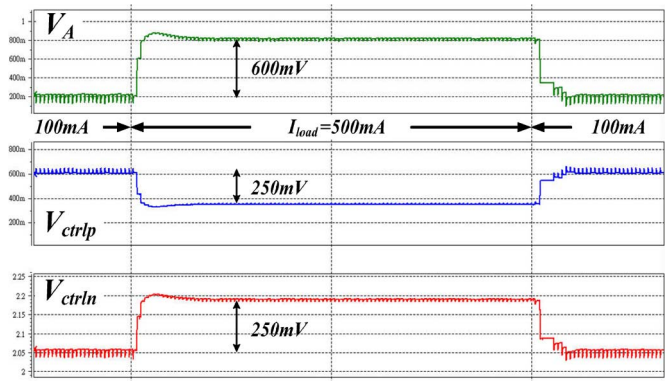


Fig. 13. Simulation of the adaptive compensation resistance R_z circuit.

TABLE II
LOCATION LIST OF ALL POLES AND ZERO

Frequency (Hz)	Dominant Pole (ω_p)	System Pole (ω_{ps})	Compensation Zero (ω_z)
Load current changed from light load to heavy load			
Light load (100mA)	12	800	900
Fast transient I (FTI)	778	3.2K	165K
Fast transient II (FTII)	360	4K	60K
Heavy load (500mA)	12	4K	4.1K
Load current changed from heavy load to light load			
Heavy load (500mA)	12	4K	4.1K
Fast transient I (FTI)	600	1.2K	391K
Fast transient II (FTII)	180	800	80K
Light load (100mA)	12	800	900

In the proposed structure with the FT technique and the APM method, the variation of compensation resistance R_z is in the range from 150 to 800 kΩ when the load changes from heavy load to light load. The variation of C_c is in the range of 2 to 200 pF in load transient period owing to the adaptive compensation capacitance circuit. Fast transient period is determined by the value of load current steps to ensure the smooth transient response and to prevent the overcharge and undercharge issues. Moreover, the APM method with the adaptive compensation resistance circuit adjusts the compensation resistance for deriving the optimal compensation zero. These mechanisms can guarantee both R_z and C_c to be adjusted in the designed range. The simulated results of the open-loop frequency response of the proposed buck converter at both different output voltages and different load conditions are shown in Fig. 14.

V. EXPERIMENTAL RESULTS

The proposed technique was fabricated with 0.35 μm CMOS process. The chip micrograph and the PCB layout are shown

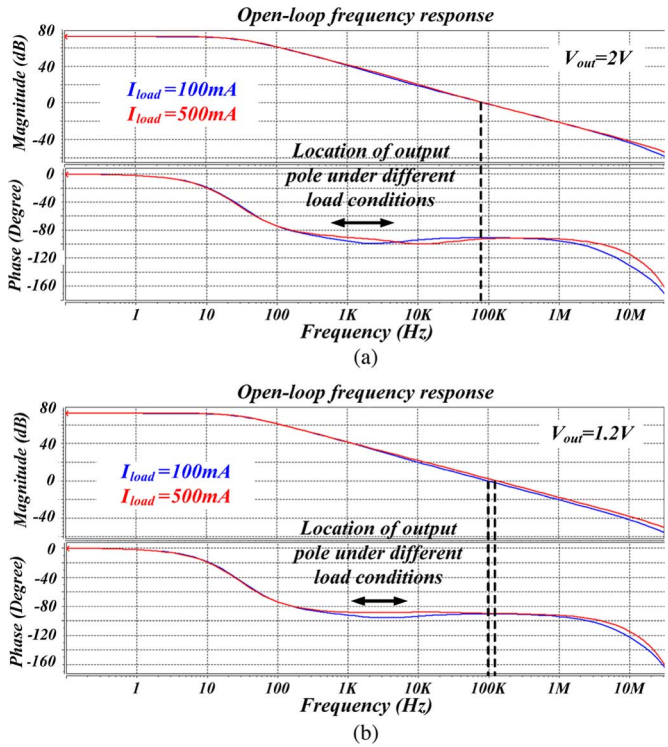


Fig. 14. Simulated results of open-loop frequency response of the proposed buck converter at different load conditions. (a) $V_{\rm out} = 2$ V. (b) $V_{\rm out} = 1.2$ V.

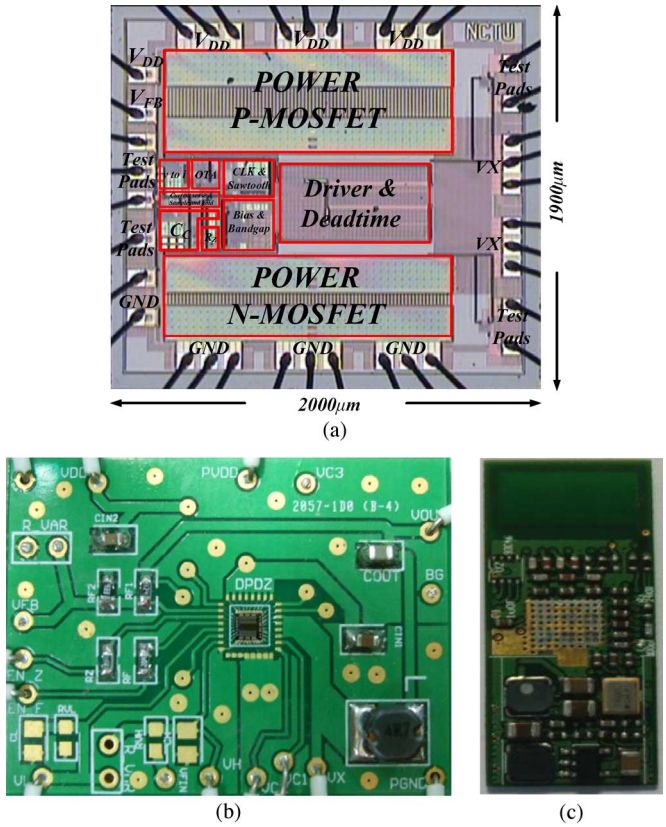


Fig. 15. (a) Chip micrograph. (b) PCB layout. (c) Wireless USB receiver.

in Fig. 15(a) and Fig. (b), respectively. The total silicon area is about 2000 μm $*$ 1900 μm, including the testing pads. The silicon overhead of the FT control with APM technique is only 150 μm $*$ 140 μm. The external inductor and capacitor are 4.7 μH and 10 μF, respectively. The switching frequency is 1 MHz. The output voltage ripple is about 15 mV. Fig. 15(c) shows the photo of the wireless USB receiver.

Fig. 16 shows $V_{\rm out}$ and inductor current I_L when I_{load} steps from 100 to 500 mA, or vice versa. The overshoot and undershoot voltages are 38 and 60 mV, respectively. The transient recovery times of undershoot and overshoot voltages are 6 and 12 μs, respectively. It is obvious that the performance of the proposed technique has small overshoot/undershoot voltage and setting time when load current suddenly changes. The waveform demonstrates that the adaptive R_z and C_c can increase the system bandwidth and PM according the instant load current condition.

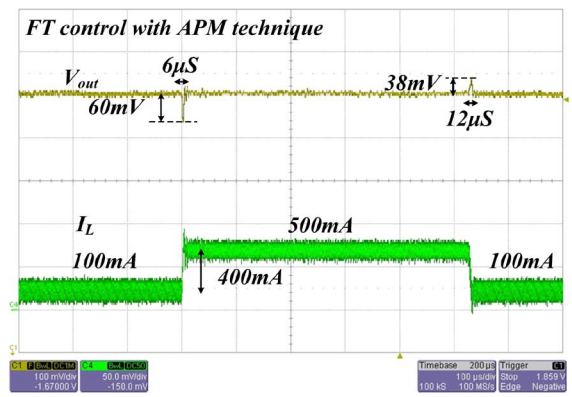


Fig. 16. Waveforms of the load transient response.

Fig. 17 shows the comparison between the proposed FT control with the APM technique, the conventional design without any fast transient techniques, and the design with APM technique only. As shown in Fig. 16, when $I_{\rm load}$ steps from 100 to 500 mA, the undershoot voltages of three results are 60 mV for the proposed method, 84 mV for the method with APM only, and 110 mV for the conventional design. The proposed method has the best performance due to the FT control with APM technique during load transient period. Besides, owing to the APM technique, the adaptive resistance R_z is adjusted according to the load condition. Thus, when the load suddenly changes from light load to heavy load, the adaptive resistance R_z would be set as a larger value than that in conventional method since the adaptive system compensation is achieved at light load. Therefore, the smaller closed-loop output impedance can be derived near the loop crossover frequency compared to conventional method through (10). The transient dip voltage is about 85 mV in conventional design and 60 mV achieved by the APM technique.

Besides, the transient recovery times are 6 μs for the proposed method, 45 μs for the method with only APM, and 42 μs for the conventional design. The closed-loop output impedance below the loop crossover frequency can affect the transient settling time. The closed-loop output impedance at the medium-frequency region shown in (11) is influenced by the system compensation coefficient. The proposed FT control with the APM technique can dynamically adjust the compensation capacitance and resistance during the load transient response. That is, when

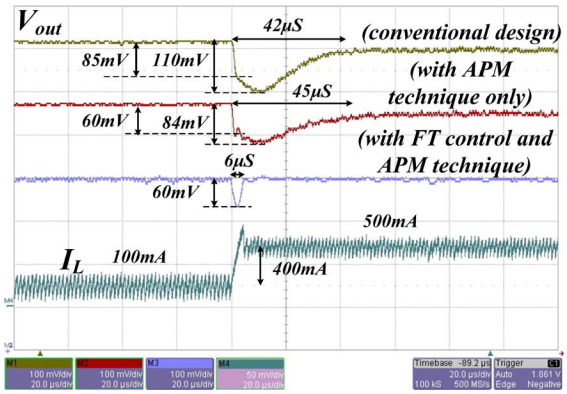


Fig. 17. Measured load transient response when load changes from 100 to 500 mA with the three fast transient techniques by separating three output waveforms.

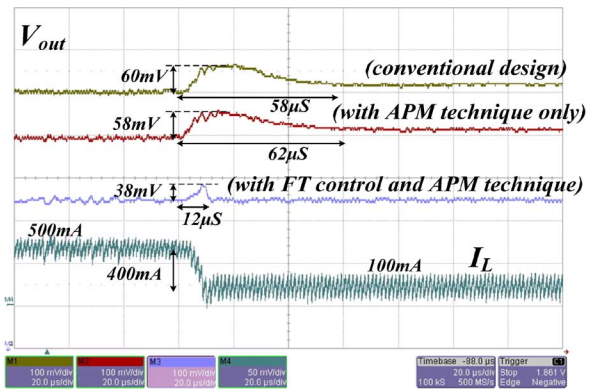


Fig. 18. Measured load transient response when load changes from 500 to 100 mA with the three fast transient techniques by separating three output waveforms.

TABLE III
RELATIVE COEFFICIENTS OF OUTPUT IMPEDANCE

The variation of output impedance at high-frequency region:				
Control method	R_o	R_z	$C_c=KC_p$	$Z(s)_{closed\_H} \propto R_o/R_z$
Conventional	70 MΩ	150 KΩ	200 pF	447
APM only	70 MΩ	800 KΩ	200 pF	87.5
FT with APM	70 MΩ	800 KΩ	2 pF	87.5
The variation of output impedance at medium-frequency region:				
Control method	R_o	R_z	$C_c=KC_p$	$Z(s)_{closed\_M} \propto \frac{1+sKC_pR_o}{1+sKC_pR_z}$
Conventional	70 MΩ	150 KΩ	200 pF	66.67
APM only	70 MΩ	800 KΩ	200 pF	44.3
FT with APM	70 MΩ	800 KΩ	2 pF	7.69

the load transient occurs, the FT control can minimize the compensation capacitance. Thus, the closed-loop output impedance can be derived as a smaller value due to the proposed FT control with the APM technique, which achieves the shortest voltage recovery time.

Fig. 18 shows the transient recovery time and the overshoot voltage between the three results when I_{load} changes from 500 to 100 mA. Certainly, the performance of the proposed method is better than those of two results. The overshoot voltages of three results are 38 mV for the proposed method, 58 mV for the method with only APM, and 60 mV for the conventional

TABLE IV
COMPARISON OF THE RELATED FAST TRANSIENT METHOD

	Load current changes from light to heavy (100 mA to 500 mA)		Load current changes from heavy to light (500 mA to 100 mA)	
	Undershoot voltage	Recovery time	Overshoot voltage	Recovery time
Conventional (w/o FT and APM)	110 mV	42 μs	60 mV	58 μs
Positive feedback [3]	76 mV	20 μs	50 mV	25 μs
AFC [4]	87 mV	70 μs	81 mV	70 μs
APM (w/o FT)	84 mV	45 μs	58 mV	62 μs
This work (w/i FT and APM)	60 mV	6 μs	38 mV	12 μs

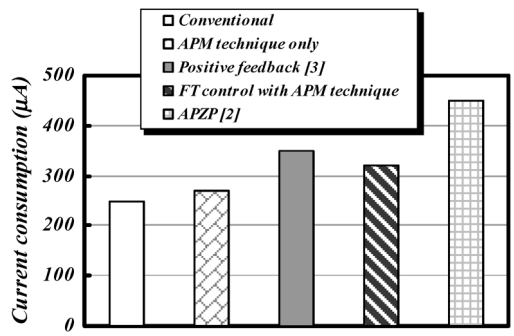


Fig. 19. Comparison in current consumption under different fast transient techniques in the design of current-mode DC-DC converters.

TABLE V
SPECIFICATIONS OF THE PROPOSED CONVERTER

Technology	*0.35 μm CMOS*
Inductor (off-chip)	*4.7 μH*
Capacitor (off-chip)	*10 μF*
Input voltage	*2.7 V~3.6 V (normal 3.3 V)*
Output voltage	*2 V*
Maximum output load current	*500 mA*
Switching frequency	*1 MHz*
Power conversion efficiency	*Max 94 % @ 300 mA*
Overshoot/undershoot (w/i FT and APM) Light load to heavy load(100mA to 500mA) Heavy load to light load(500mA to 100mA)	 *60 mV* *38 mV*
Recovery time (w/i FT and APM) Light load to heavy load(100mA to 500mA) Heavy load to light load(500mA to 100mA)	 *6 μs* *12 μs*
Die size(including pads)	*2000 μm x 1900 μm*

design. Moreover, the transient recovery times are 12 μs for the proposed method, 62 μs for the method with only APM, and 58 μs for the conventional design.

Table III shows the relative coefficients for the output impedance in the proposed buck converter of the FT control with APM technique. Owing to the adaptive compensation, the closed-loop output impedance can be varied when the fast transient mechanism is activated.

Table IV lists the comparison with the related method of fast transient techniques in the design of DC-DC converters. Obviously, the proposed FT control with the APM technique has the better performance than those of other fast transient techniques.

TABLE VI
LIST OF OTHER FAST TRANSIENT CONTROL METHODOLOGY

	This work	[2]	[7]	[10]	[11]	[13]
Technology	0.35 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.6 μm CMOS	0.25 μm CMOS	Prototype
Inductor	4.7 μH	4.7 μH	2.2 μH	4.7 μH	15.2 μH	1 μH
Capacitor	10 μF	10 μF	10 μF	10 μF	21.6 μF	288 μF
Input voltage	2.7 – 3.6 V	1.8 V	2.5 – 3.3 V	2.2 – 6 V	2.5 V	6.5 V
Output voltage	2 V	1.0 V	0.5 – 2.5 V	0.6 – 5.8 V	1.1 – 2.3 V	1.3 V
Switching Freq.	1 MHz	1 MHz	5 MHz	1.1 MHz	460 – 860 kHz	780 kHz
Maximum current	600 mA	500 mA	500 mA	1 A	N/A	10 A
Control mechanism	Current mode PWM control	Current mode PWM control	PWM with quadratic slope compensation	Current mode PWM control	Digital sliding control	Proximate time-optimal digital (PTOD) controller
Transient voltage drop	60 mV	48 mV	50 mV	80 mV	30 mV	36 mV
Transient recovery time	6 μs	10 μs	50 μs	20 μs	10 μs	30 μs
Transient load step ΔI_{load}	400 mA	400 mA	180 mA	500 mA	80 mA	7.5 A
Peak efficiency	93 %	86 %	85 %	96.7 %	95 %	N/A
Chip size	3.8 mm^2	3.8 mm^2	5.3 mm^2	1.35 mm^2	1.43 mm^2	N/A

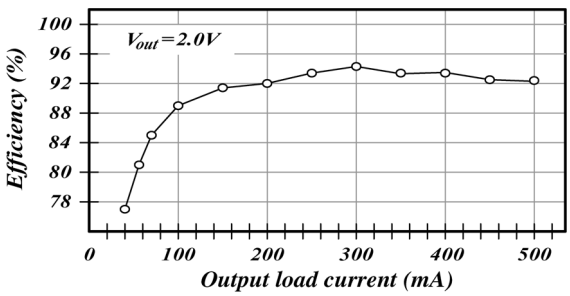


Fig. 20. Power conversion efficiency of the proposed converter.

Fig. 19 shows the current consumption of four different design methods. Owing to the small overhead of the implementation in the adaptive resistance, the current consumption of the APM technique is increased about 20 μA compared to the conventional design. Besides, the current consumption of the positive feedback is larger than that of the conventional about 100 μA. Thus, the FT control with APM technique needs more 70 μA quiescent current than that of the conventional design. Moreover, the APZP technique reported in [2] can has the good transient response but lead to a large current consumption owing to the combination of adaptive frequency control (AFC) technique.

Fig. 20 shows the power conversion efficiency of the proposed DC-DC converter through the FT control with APM technique. The efficiency can be kept at 92% at medium to heavy loads. The light-load efficiency is deteriorated to 78% at load current 40 mA. The reason is that the operation of the converter enters the discontinuous conduction mode (DCM) operation and thus the switching loss dominates the total power consumption. Therefore, the operation can be switched to dithering skip-modulation (DSM) or pulse frequency modulation (PFM) operation [28] to improve the power conversion efficiency. The detail specifications of the proposed DC-DC buck converter are listed in Table V.

Table VI shows the list of other popular fast transient control methodologies. The fast transient response and the small output voltage ripple are the advantages of the proposed converter. The proposed FT control with the APM technique is suitable to the modern battery-operated system and can strengthen the quality of the power source in power management modules.

VI. CONCLUSION

In this paper, the FT control with the APM technique is proposed to achieve good transient response in current-mode DC-DC buck converters at different load conditions. The fast transient control can effectively improve the overshoot/undershoot voltage and the transient recovery time. The compensation pole-zero pair can be dynamically moved toward high frequencies during transient period. After the output voltage is regulated to its steady-state value, the compensation pole-zero pair is smoothly moved back to the steady-state position. Thus, the overshoot/undershoot voltage can be decreased. Besides, owing to the APM technique, the compensation zero is moved to nearly close to the position of the system pole to achieve the pole-zero cancellation. Thus, the PM of the system can be always kept an adequate value in steady state. Experimental results show that the overshoot/undershoot voltage is smaller than 60 mV and the transient response time is smaller than 12 μs as load current suddenly changes from 100 to 500 mA, or vice versa. Compared with conventional designs without any fast transient technique, the performances of undershoot voltage and recovery time are enhanced by 45% and 85%, respectively.

ACKNOWLEDGMENT

The authors would like to thank Energy Pass Incorporation for their help.

REFERENCES

[1] G. Patounakis, Y. W. Li, and K. L. Shepard, "A fully integrated on-chip DC-DC conversion and power management system," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 443–451, Mar. 2004.

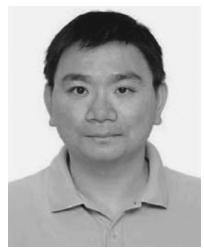
[2] C.-Y. Hsieh and K.-H. Chen, "Adaptive pole-zero position (APZP) technique of regulated power supply for improving SNR," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2949–2963, Nov. 2008.

[3] H.-W. Huang, H.-H. Ho, C.-C. Chien, K.-H. Chen, G.-K. Ma, and S.-Y. Kuo, "Fast transient DC-DC converter with on-chip compensated error amplifier," in *Proc. Euro. Solid-State Circuits Conf.*, 2006, pp. 324–327.

[4] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Adaptive frequency controltechnique for enhancing transient performance of DC-DC converters," in *Proc. Euro. Solid-State Circuits Conf.*, 2007, pp. 174–177.
[5] L. Chen and B. Ferrario, "Adaptive Frequency Compensation for DC-to-DC Converter," U.S. Patent 20 060 176 098, Aug. 10, 2006.
[6] C.-H. Tso and J.-C. Wu, "A ripple control buck regulator with fixed output frequency," *IEEE Power Electron. Lett.*, vol. 1, pp. 61–63, Sep. 2003.
[7] K. Umimura, H. Sakurai, and Y. Sugimoto, "A CMOS current-mode DC-DC converter with input and output voltage-independent stability and frequency characteristics utilizing a quadratic slope compensation scheme," in *Proc. Euro. Solid-State Circuits Conf.*, 2007, pp. 178–181.
[8] A. Barrado, A. Lázaro, R. Vázquez, V. Salas, and E. Olías, "The fast response double buck DC-DC converter (FRDB) operation and output filter influence," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1261–1270, Nov. 2005.
[9] J. J. Chen, F. C. Yang, and C. C. Chen, "A new monolithic fast-response buck converter using spike-reduction current-sensing circuits," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1101–1111, Mar. 2008.
[10] F.-F. Ma, W.-Z. Chen, and J.-C. Wu, "A monolithic current-mode buck converter with advanced control and protection circuit," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1836–1846, Sep. 2007.
[11] J. Kim and M. A. Horowitz, "An efficient digital sliding controller for adaptive power-supply regulation," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 639–647, May 2002.
[12] J. Xu, G. Zhou, and M. He, "Improved digital peak voltage predictive control for switching DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3222–3229, Aug. 2009.
[13] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcón, L. Pao, and D. Maksimović, "Proximate time-optimal digital control for synchronous buck DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008.
[14] K. K.-S. Leung and H. S.-h. Chung, "A comparative study of the boundary control of buck converters using first- and second-order switching surfaces," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1196–1209, Jul. 2007.
[15] W.-T. Yan, C. N.-M. Ho, H. S.-H. Chung, and K. T. K. Au, "Fixed-frequency boundary control of buck converters with second-order switching surface," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2193–2201, Sep. 2009.
[16] M. Karppanen, J. Arminen, T. Suntio, K. Savela, and J. Simola, "Dynamical modeling and characteristics of peak-current-controlled superbuck converter," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1370–1380, May 2008.
[17] E. Figueres, G. Garcera, J. M. Benavent, M. Pascual, and J. A. Martinez, "Adaptive two-loop voltage-mode control of DC-DC switching converters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 239–253, Feb. 2006.
[18] Y. S. Lai and C. A. Yeh, "Predictive digital-controlled converter with peak current-mode control and leading-edge modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1854–1863, Jun. 2009.
[19] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.
[20] C. M. Lia, S. J. Chiang, C. Y. Lai, K. H. Pan, G. C. Pan, and G. S. Hsu, "Modeling and controller design of a current-mode controlled converter," *IEEE Trans. Ind. Electron.*, vol. 41, no. 2, pp. 231–240, Apr. 1994.
[21] J. Roh, "High-performance error amplifier for fast transient DC-DC converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 9, pp. 591–595, Sep. 2005.
[22] K.-H. Chen, C.-J. Chang, and T.-H. Liu, "Bidirectional current-mode capacitor multipliers for on-chip compensation," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 180–188, Jan. 2008.
[23] B. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.
[24] G. A. Rincon-Mora, "Active capacitor multiplier in miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.
[25] I.-C. Hwang, "Area-efficient and self-biased capacitor multiplier for on-chip loop filter," *IEEE Electron. Lett.*, vol. 42, no. 24, pp. 1392–1393, Nov. 2006.
[26] G. Palumbo and S. Pennisi, "A high-performance CMOS voltage follower," in *Proc. IEEE Int. Conf. Electron. Circuits Syst.*, 1998, vol. 2, pp. 21–24.
[27] B. Razavi, *Design of Analog CMOS Integrated Circuit*. New York: McGraw-Hill Higher Education, 2001.
[28] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering skip modulation, width and dead time controllers in highly efficient DC-DC converters for system-on-chip applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2451–2465, Nov. 2007.

Yu-Huei Lee (S'09) was born in Taipei, Taiwan. He received the B.S. and M.S. degrees from the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2007 and 2009, respectively. He is currently pursuing the Ph.D. degree in the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan.

He is a faculty member with the Mixed-Signal and Power Management IC Laboratory, Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan. His current research interests include the power management integrated circuit design, LED driver IC design, and analog integrated circuits.



Shao-Chang Huang received the B.S. and M.S. degrees in electrical engineering from the National Cheng Kung University, Tainan, Taiwan, in 1994 and 1996, respectively, and the Ph.D. degrees from the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2011.

From 1996 to 1998, he was an Officer in National Compulsory Military Service. From 1998 to 1999, he was engaged in thin-film-transistor device at ERSO, ITRI, Taiwan. From 1999 to 2006, he worked on ESD/Latch-up/IO research in UMC, Ltd., HBA, Ltd., TSMC, Ltd. and NOVATEK, Ltd. As a UMC engineer, he worked on 90 nm process ESD solutions at IBM, Fishkill, NY, in 2001. Since the end of 2006, he joined eMemory Technology, Taiwan, where he is currently the ESD/IO Department Manager. He is the author or coauthor of more than 8 papers published in journals and conferences, and he holds more than 20 patents. His current research interests include ESD/Latch-up devices and circuits, and I/O related circuits.

Shih-Wei Wang was born in Hualien, Taiwan, in 1980. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan, in 2006, and the M.S. degree from the Department of Electrical and Control Engineering, National Chiao Tung University, Hsinchu, Taiwan, in 2010, where he is currently pursuing the Ph.D. degree in the Institute of Electrical Control Engineering.

His research interests include the design of switch-mode power converters, linear regulators, analog integrated circuits, and mixed-signal integrated circuits.

Ke-Horng Chen (M'04–SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a part-time IC Designer with Philips, Taipei, Taiwan. From 1998 to 2000, he was an Application Engineer with Avanti, Ltd., Taiwan. From 2000 to 2003, he was a Project Manager with ACARD, Ltd., where he was engaged in designing power management ICs. He is currently an Associate Professor with the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 80 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, display algorithm and driver designs of liquid crystal display (LCD) TV, red, green, and blue (RGB) color sequential backlight designs for optically compensated bend (OCB) panels, and low-voltage circuit designs.