Design of Compact ESD Protection Circuit for V-Band RF Applications in a 65-nm CMOS Technology

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***Abstract*—Nanoscale CMOS technologies have been widely used to implement radio-frequency (RF) integrated circuits. However, the thinner gate oxide and silicided drain/source in nanoscale CMOS technologies seriously degraded the electrostatic discharge (ESD) robustness of RF circuits. Against ESD damage, an on-chip ESD protection design must be included in the RF circuits. As the RF circuits operate in the higher frequency band, the parasitic effect from ESD protection circuit must be strictly limited. To provide the effective ESD protection for a 60-GHz low-noise amplifier with less RF performance degradation, two new ESD protection circuits were studied in a 65-nm CMOS process. Such compact ESD protection circuits have been successfully verified in silicon chip to achieve the 2-kV human-body-model ESD robustness with the low insertion loss in small layout area. With the better performances, the proposed ESD protection circuits were very suitable for V-band RF ESD protection.**

***Index Terms*—CMOS, electrostatic discharge (ESD) protection, radio frequency (RF), V-band.**

I. Introduction

As CMOS technologies advanced, the radio-frequency (RF) integrated circuits have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production [1]–[3]. However, nanoscale CMOS technologies seriously degraded the electrostatic discharge (ESD) robustness of integrated circuits. ESD protection must be taken into consideration during the design phase of integrated circuits, especially the RF circuits [4], [5]. In the RF circuits, the input and output pads are usually connected to the gate terminal or silicided drain/source terminal of the metal–oxide-semiconductor field-effect transistor (MOSFET), which leads to a very low ESD robustness if no appropriate ESD protection design is applied. Once the RF circuit is damaged by ESD event, it cannot be recovered and the RF functionality is lost. Therefore, on-chip ESD protection design must be provided for all input and output pads in RF circuits.

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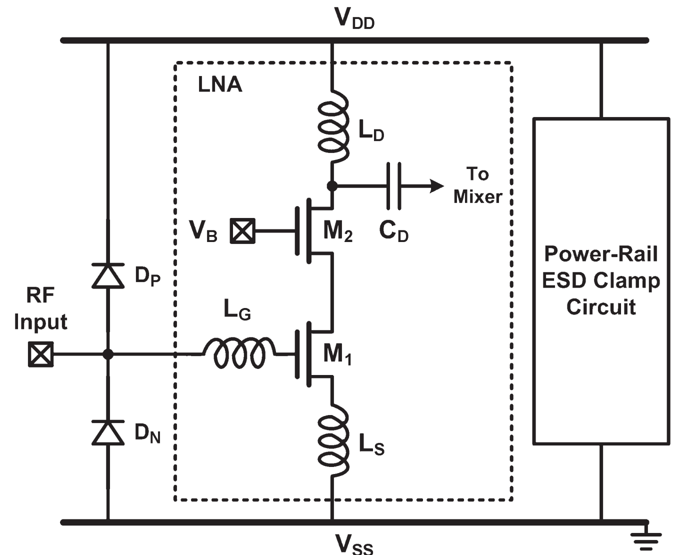

Fig. 1. Conventional ESD protection design with double diodes and power-rail ESD clamp circuit for LNA.

Adding ESD protection causes RF performance degradation with several undesired effects [6]–[9]. Parasitic capacitance of ESD protection device is one of the most important design considerations for RF circuits. A typical specification for a giga-Hz low-noise amplifier (LNA) on human-body-model (HBM) ESD robustness and the maximum parasitic capacitance of ESD protection device are 2 kV and 200 fF, respectively [9]–[11]. As the operating frequencies of RF circuits increase, the parasitic capacitance was more strictly limited. In order to fulfill such a tight specification, diodes had been commonly used for RF ESD protection [12]. The conventional double-diode ESD protection design for LNA is shown in Fig. 1, where two ESD diodes (D_P and D_N) at input pad are assisted with the power-rail ESD clamp circuit to prevent LNA from ESD damage [13]. When D_P and D_N are under forward-biased condition, they can provide efficient discharging paths from input pad to V_{DD} and from V_{SS} to input pad, respectively. Besides, the power-rail ESD clamp circuit provides the ESD current paths between V_{DD} and V_{SS}.

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The conventional ESD protection circuit in Fig. 1 can provide the corresponding current discharging paths under ESD events. Under positive-to-$V_{\rm DD}$ mode (PD-mode) and negative-to-$V_{\rm SS}$ mode (NS-mode) ESD stresses, ESD current is discharged through the forward-biased D_P and D_N, respectively. To avoid the ESD diodes from being operated under breakdown condition under positive-to-$V_{\rm SS}$ mode (PS-mode) and negative-to-$V_{\rm DD}$ mode (ND-mode) ESD stresses, which results in substantially lower ESD robustness, the power-rail ESD clamp circuit is applied between $V_{\rm DD}$ and $V_{\rm SS}$ to provide ESD current paths between the power rails. Thus, ESD current is discharged from the input pad through the forward-biased D_P to $V_{\rm DD}$, and discharged to the grounded $V_{\rm SS}$ pad through the turn-on efficient power-rail ESD clamp circuit during PS-mode ESD stresses. Similarly, ESD current is discharged from the $V_{\rm DD}$ pad through the turn-on efficient power-rail ESD clamp circuit and the forward-biased D_N to the input pad under ND-mode ESD stresses.

To mitigate the performance degradation caused by ESD protection devices, some design techniques had been developed to reduce the parasitic capacitance of ESD protection devices [14]. The parasitic capacitance of ESD protection devices can be tuned out by using inductors [15]–[17]. The Inductors exhibit higher impedance at higher frequencies, and they can block the RF signals [18]. The ESD protection circuit with reduced parasitic capacitance can be easily combined or co-designed with RF circuits [19], [20]. In this paper, two new designs of the compact ESD protection circuits for V-band RF applications are proposed [21]. Such ESD protection designs have been implemented in cell configuration and reached 50-Ω input/output matching, which can be directly applied to the 60-GHz RF LNA. Therefore, the proposed ESD protection cell in this paper is suitable for RF circuit designer for them to easily apply ESD protection for V-band RF applications.

This paper consists of six Sections. The impacts of ESD protection on RF performance of LNA are calculated in Section II. The proposed ESD protection designs are presented in Section III. The circuit realization and measurement results in silicon are presented in Section IV. The simulation results of appling the proposed ESD protection circuit to a 60-GHz LNA are presented in Section V. Section VI concludes this work.

II. IMPACTS OF ESD PROTECTION ON RF PERFORMANCE

In the circuit of Fig. 1, the parasitic effects of ESD protection diodes caused RF performance degradation. Some equations can be calculated to describe this condition [22]. The insertion loss of ESD protection diodes $(\mathrm{IL}_{\rm ESD})$ can be expressed as

$$IL_{\rm ESD} = \left|1+\frac{Z_0}{2Z_{\rm ESD}}\right| = \left|\frac{1}{S_{21,\rm ESD}}\right| \quad (1)$$

where Z_0 is the 50-Ω normalization impedance, and $Z_{\rm ESD}$ is the parasitic impedance of ESD protection diodes. Using the expression in dB, the insertion loss $(\mathrm{IL}_{\rm ESD})$ is equal to the absolute value of S_{21}-parameter $(S_{21,\rm ESD})$.

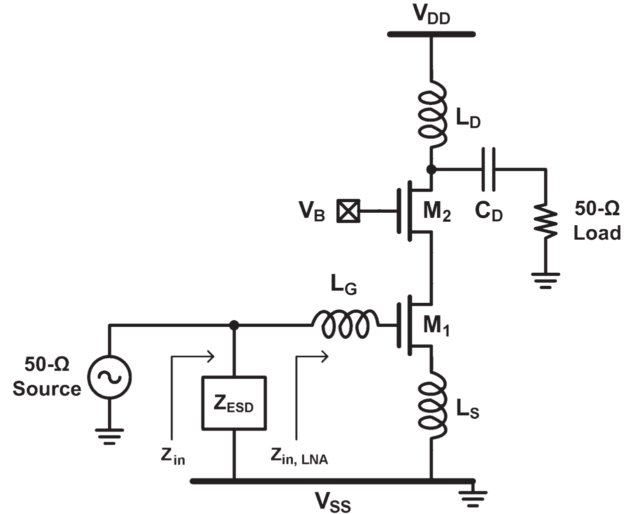


Fig. 2. LNA with parasitic impedance of input pad and ESD protection diodes for calculating the power gain.

The power gain of an RF LNA with the parasitic effects of ESD protection device has been calculated from the schematic circuit diagram, as shown in Fig. 2. A simple expression for the input impedance $(Z_{\rm in,LNA})$ of the inductively degenerated LNA at resonance is

$$Z_{\rm in,LNA} = s(L_s+L_g)+\frac{1}{sC_{\rm gs}}+\left(\frac{gm}{C_{\rm gs}}\right)L_s \approx \omega_T L_s = Z_0 \quad (2)$$

where ω_T is the unity-gain frequency of the MOS transistor. The overall input impedance $(Z_{\rm in})$ of the RF LNA with ESD protection diodes is

$$Z_{\rm in} = Z_{\rm ESD}//Z_{\rm in,LNA} \approx Z_{\rm ESD}//Z_0. \quad (3)$$

Therefore, the overall transconductance (G_m) of the LNA is

$$G_m = \frac{Z_{\rm ESD}}{Z_{\rm ESD}+Z_0}\frac{\omega_T}{s(Z_0+Z_{\rm in})} = \frac{\omega_T}{sZ_0}\frac{1}{2+\frac{Z_0}{Z_{\rm ESD}}}. \quad (4)$$

To analyze the overall power gain of the LNA, the feedback capacitor $C_{\rm gd}$ of the MOS transistor was neglected first, and the input and output were assumed to be conjugately matched to get a simpler expression for the power gain. The transducer power gain (G_T) is

$$G_T = \frac{P_L}{P_{\rm avs}} = \frac{\frac{1}{8}|V_sG_m|^2(R_o//Z_0)}{\frac{1}{8}\frac{|V_s|^2}{Z_0}} = \frac{\omega_T^2(R_o//Z_0)}{4\omega_o^2 Z_0 IL_{\rm ESD}^2} \quad (5)$$

where P_L is the average power delivered to the load, $\mathrm{P}_{\rm avs}$ is the average power available from the source, R_o is the output impedance of the cascoded NMOS transistors, and ω_o is the operating frequency of input RF signal. From (5), the insertion loss of ESD protection is disadvantageous to the transducer power gain of LNA. Therefore, ESD protection circuit with low insertion loss is needed for RF applications.

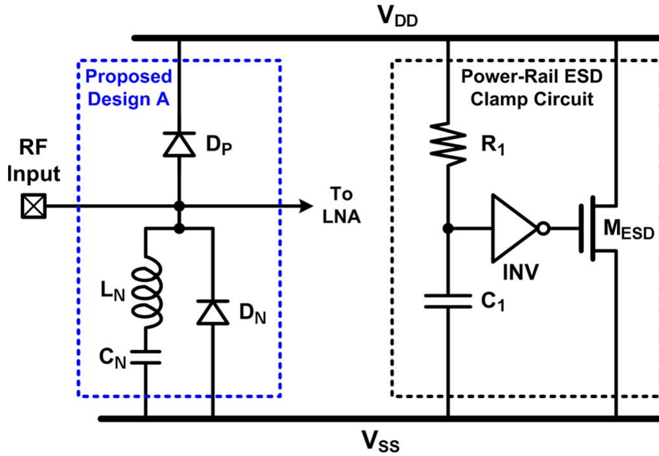


Fig. 3. Proposed ESD protection design A and power-rail ESD clamp circuit.

If the parasitic impedance of ESD protection diodes (Z_{ESD}) can be increased, the power gain of the RF LNA can be improved. The device dimensions of ESD protection diodes should be reduced to decrease (increase) the parasitic capacitance (resistance), which in turn reduces RF performance degradation caused by the parasitic impedance of the ESD protection diodes. However, ESD robustness needs to be maintained, so the minimum device dimensions of ESD protection diodes cannot be shrunk unlimitedly. The parasitic impedance of the ESD diodes, even with limited device sizes, still generates the Z_{ESD} into above equations.

As the operating frequency of RF circuits increases, the Z_{ESD} will be decreased due to capacitive component. As Z_{ESD} decreases, the insertion loss in (1) will be increased, and the transducer power gain in (5) will be decreased. Therefore, how to design an effective on-chip ESD protection circuit for RF circuits operating in higher frequency bands with minimum RF performance degradation is a challenge, which must be solved for safe mass production of RF integrated circuits.

III. Proposed ESD Protection Designs

Fig. 3 shows the circuit of one proposed ESD protection design, where a pair of the ESD protection diodes (D_P and D_N) and a series inductor and capacitor (L_N and C_N) are placed beside the input pad. The ESD protection diodes provide the ESD current paths between input and $V_{\mathrm{DD}}/V_{\mathrm{SS}}$. The power-rail ESD clamp circuit is also needed to provide the ESD current paths between V_{DD} and V_{SS}.

The inductor in series with the capacitor can block the dc leakage path from input pad to V_{SS} under normal circuit operating conditions. Besides, the series inductor and capacitor are designed to resonate at low frequency. As the frequency is lower (higher) than the resonant frequency of the series inductor and capacitor, the capacitance (inductance) dominated the impedance. The equivalent inductance of the series inductor and capacitor (L_{eq}) can be expressed as

$$L_{\mathrm{eq}} = L_N - \frac{1}{\omega^2 C_N}. \tag{6}$$

At operating frequency of input RF signal, the inductance (L_{eq}) can be used to eliminate the parasitic capacitance of ESD protection diodes (C_{Diodes}).

The resonant frequency of parallel L_{eq} and C_{Diodes}, which is designed to be the operating frequency of RF circuit, can be obtained by

$$\omega_o = \frac{1}{\sqrt{L_{\mathrm{eq}} C_{\mathrm{Diodes}}}}. \tag{7}$$

From (6) and (7), the equations can be held once the inductor, capacitor, and ESD protection diodes satisfy

$$\omega_o L_N - \frac{1}{C_N} = \frac{1}{C_{\mathrm{Diodes}}}. \tag{8}$$

Once the design parameters have been chosen, including the size of ESD protection diodes and operating frequency of RF circuit, the required inductor and capacitor for resonation can be calculated. Therefore, the RF input port will see a large impedance from the ESD protection circuit (Z_{ESD}), where the parasitic capacitance (C_{Diodes}) has been eliminated, and the parasitic resistance (R_{Diodes}) remains large.

To reduce the inductance used in L_N, another supplement capacitor (C_S) can be added between RF input and V_{SS}. In other words, the parasitic capacitance of ESD protection diodes (C_{Diodes}) is increased by adding the parallel capacitor (C_S). It is better to add the supplement capacitor rather then increase the diode size, because the supplement capacitor provides a purely capacitive device, while increasing diode size lowers the parasitic resistance, which leads to the lower parasitic impedance and higher insertion loss. With this structure, the L_N with smaller radius can be used to reduce the cell area. Since the C_{Diodes} depend on the required ESD robustness, the sizes of C_N and C_S can be designed to optimize the cell area and RF performances.

The power-rail ESD clamp circuit, which consists of the RC-inverter-triggered NMOS, is used to provide ESD current paths between V_{DD} and V_{SS} under ESD stress conditions. The R_1 ($\sim$10 kΩ) and C_1 ($\sim$10 pF) with the time constant of 0.1 μs $\sim$ 1 μs can distinguish the ESD transients from the normal circuit operating conditions. The NMOS (M_{ESD}) with $\sim$2000-μm width is used as the main ESD clamp device. As positive ESD stress from V_{DD} to V_{SS}, the large-sized NMOS (M_{ESD}) is turned on to provide ESD current path from V_{DD} to V_{SS}. As negative ESD stress from V_{DD} to V_{SS}, the parasitic diode in large-sized NMOS (M_{ESD}) also provides the ESD current path from V_{SS} to V_{DD}. Since the power-rail ESD clamp circuit is placed between V_{DD} and V_{SS}, it does not contribute parasitic effects to RF input port.

As the ESD stress to the input pin of RF LNA, the ESD current path of PD-mode (NS-mode) consists of one ESD protection diode D_P (D_N). Besides, the PS-mode (ND-mode) ESD current is discharged through the D_P (D_N) and the power-rail ESD clamp circuit.

Fig. 4 shows the circuit of another proposed ESD protection design. A pair of the ESD protection diodes (D_P and D_N) is still used to provide ESD current paths, but the series inductor

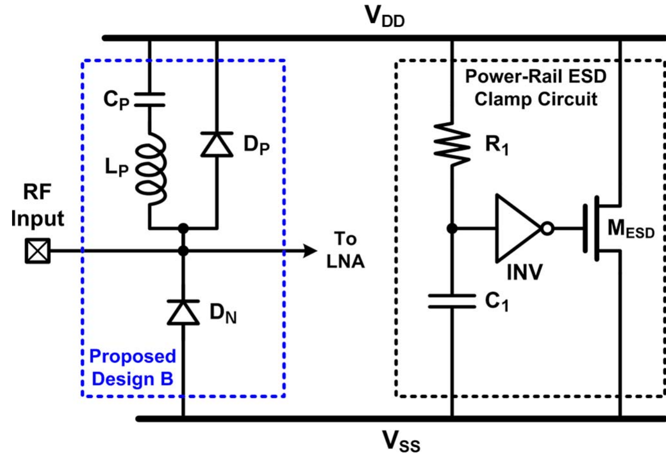


Fig. 4. Proposed ESD protection design B and power-rail ESD clamp circuit.

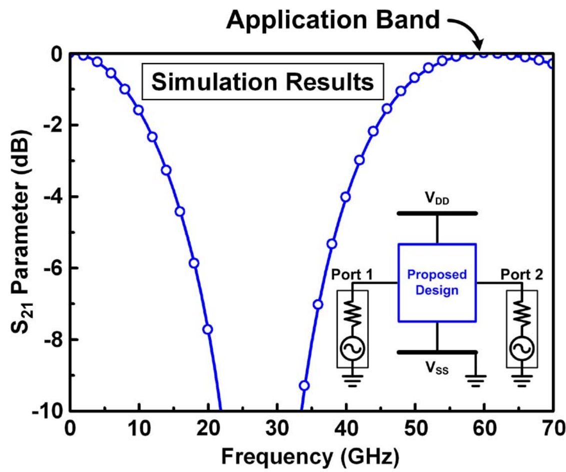


Fig. 5. Simulated S_{21}-parameter of proposed design.

and capacitor (L_P and C_P) are placed between RF input and V_{DD}. The operation of proposed design B is similar to that of proposed design A. The design parameters can be calculated by

$$\omega_o L_P - \frac{1}{C_P} = \frac{1}{C_{\mathrm{Diodes}}}. \tag{9}$$

The proposed designs are simulated by using the ideal devices. A 0.11-nH inductor and a 300-fF capacitor are used for the series inductor and capacitor. The ESD protection diodes are simplified to be an 80-fF capacitor. Since the ideal devices are used, the proposed designs A and B have the same simulation results. The simulated S_{21}-parameter $(S_{21,\mathrm{ESD}})$ of the proposed design is shown in Fig. 5. The S_{21} value at 60 GHz can be designed to be 0 dB, which means that insertion loss from ESD protection circuit is also 0 dB.

IV. Verification in Silicon

A. Test Circuits

The test circuits of the proposed ESD protection designs have been fabricated in a 65-nm CMOS process. Both proposed designs are split to 4 test circuits with different sizes of ESD protection diodes. The device dimensions of the test circuits

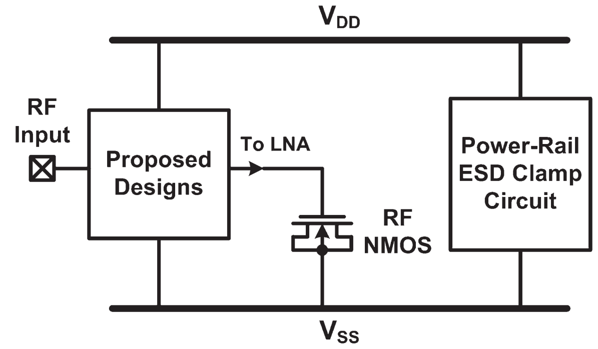


Fig. 6. RF-NMOS emulator to verify ESD robustness of proposed ESD protection designs.

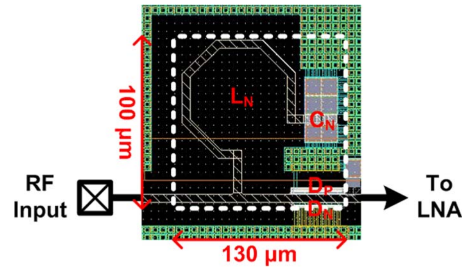


Fig. 7. Layout top view of test circuit A4.

are listed in Table I. The width of D_P or D_N in test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are split as 8, 15, 23, and 30 μm, respectively, while the length of D_P or D_N are kept at 0.6 μm. In this configuration, the C_{Diodes} of test circuits A1 (B1), A2 (B2), A3 (B3), and A4 (B4) are 21 fF, 40, 61, and 80 fF, respectively. The L_N and L_P are chosen as 0.11 nH for designs A and B. Therefore, the C_N and C_P are designed as 300 fF, and the C_S with 60, 40, and 20 fF are added to the test circuits A1 (B1), A2 (B2), and A3 (B3), respectively.

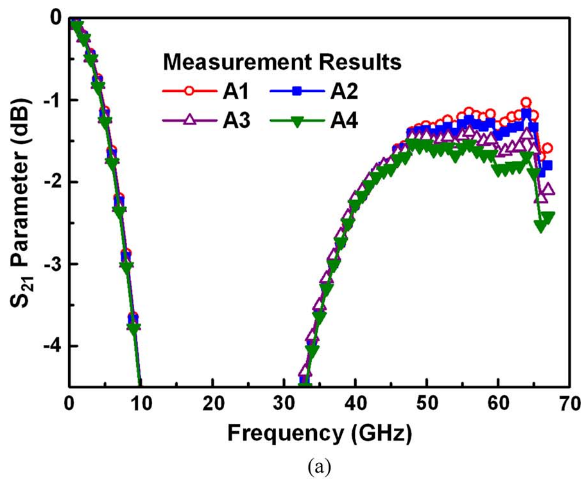
To facilitate the on-wafer RF measurement, one set of these test circuits are arranged with G–S–G style in layout. Besides, another set of the test circuits are implemented with the RF-NMOS emulator [23], as shown in Fig. 6. The ESD robustness of ESD-protected RF circuits can be estimated by the ESD protection design with RF-NMOS emulator. All test circuits have been fabricated for RF and ESD verifications. Part of the layout top view of one test circuit is shown in Fig. 7. The test circuit A4 with 0.11 nH L_N, 300 fF C_N, and $30 \times 0.6\ \mu\mathrm{m}^2$ D_P (D_N) is drawn in a compact layout area of $130 \times 100\ \mu\mathrm{m}^2$. The same layout areas are used to draw the other test circuits, since almost same components are used in every test circuits.

B. RF Performances

With the on-wafer measurement, the RF characteristics of the test circuits have been extracted. The two-port S-parameters of the test circuits from 0 to 67 GHz were measured by using the vector network analyzer. During the S-parameter measurement, the port 1 and port 2 were biased at 0.5 V, which is $V_{\mathrm{DD}}/2$ in the given 65-nm CMOS process. The dc bias of 1-V V_{DD} was also supplied to the test circuits. In order to extract the

TABLE I
DEVICE PARAMETERS OF PROPOSED ESD PROTECTION DESIGNS

Test Circuit	Proposed Design A				Proposed Design B			
	A1	A2	A3	A4	B1	B2	B3	B4
L_P	N/A	N/A	N/A	N/A	0.11 nH	0.11 nH	0.11 nH	0.11 nH
C_P	N/A	N/A	N/A	N/A	300 fF	300 fF	300 fF	300 fF
D_P	8 μm x 0.6 μm (9 fF)	15 μm x 0.6 μm (18 fF)	23 μm x 0.6 μm (27 fF)	30 μm x 0.6 μm (36 fF)	8 μm x 0.6 μm (9 fF)	15 μm x 0.6 μm (18 fF)	23 μm x 0.6 μm (27 fF)	30 μm x 0.6 μm (36 fF)
L_N	0.11 nH	0.11 nH	0.11 nH	0.11 nH	N/A	N/A	N/A	N/A
C_N	300 fF	300 fF	300 fF	300 fF	N/A	N/A	N/A	N/A
D_N	8 μm x 0.6 μm (12 fF)	15 μm x 0.6 μm (22 fF)	23 μm x 0.6 μm (34 fF)	30 μm x 0.6 μm (44 fF)	8 μm x 0.6 μm (12 fF)	15 μm x 0.6 μm (22 fF)	23 μm x 0.6 μm (34 fF)	30 μm x 0.6 μm (44 fF)
C_S	60 fF	40 fF	20 fF	N/A	60 fF	40 fF	20 fF	N/A



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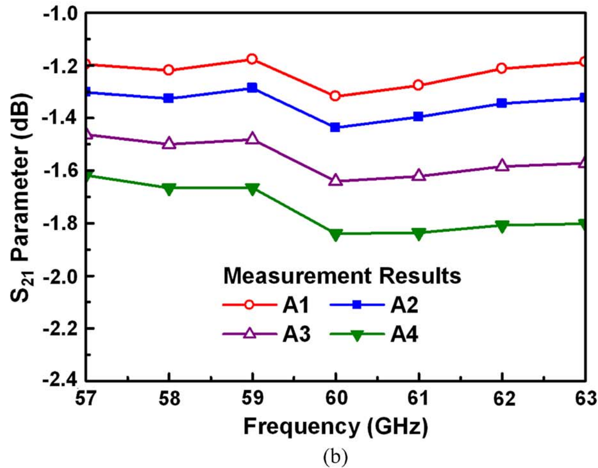
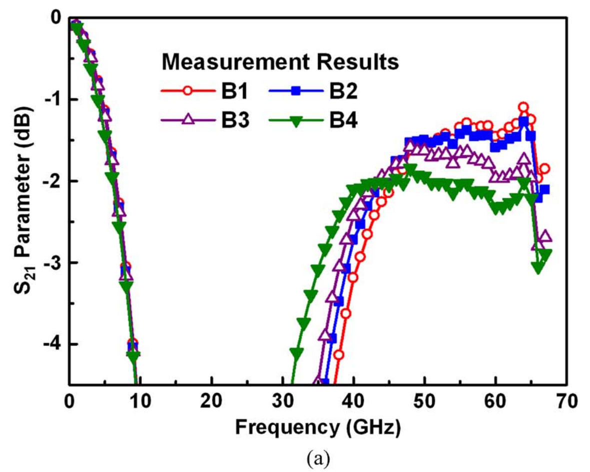
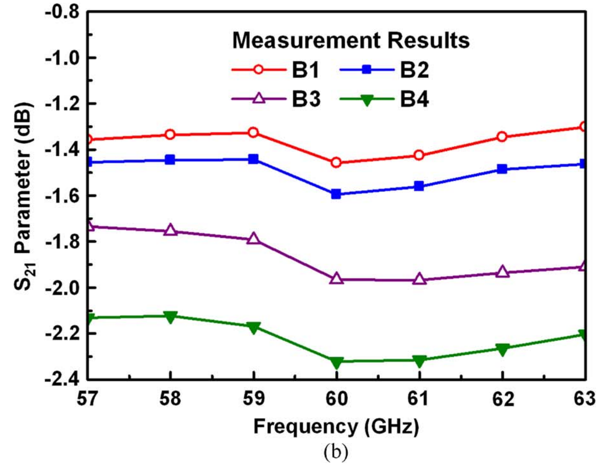


(b)

Fig. 8. Measured S_{21}-parameters of proposed design A within (a) 0–67 GHz and (b) 57–63 GHz.



(a)



(b)

Fig. 9. Measured S_{21}-parameters of proposed design B within (a) 0–67 GHz and (b) 57–63 GHz.

intrinsic characteristics of the test circuits in high frequencies, the parasitic effects of the G–S–G pads have been removed by using the de-embedding technique [24]. The source and load resistances to the test circuits are kept at 50 Ω.

The measured S_{21}-parameters versus frequencies among the test circuits are shown in Figs. 8 and 9. As shown in Fig. 8, the proposed design A can reduce the insertion loss at designed frequency band. The insertion loss of the proposed design

TABLE II
COMPARISON ON EXPERIMENTAL RESULTS AMONG ESD PROTECTION CIRCUITS IN SILICON

	Proposed Design A				Proposed Design B				Reference [25]
	A1	A2	A3	A4	B1	B2	B3	B4	
S_{11}-Parameters at 60 GHz	-16 dB	-17 dB	-19 dB	-21 dB	-22 dB	-29 dB	-26 dB	-26 dB	-22 dB
S_{21}-Parameters at 60 GHz	-1.3 dB	-1.4 dB	-1.6 dB	-1.8 dB	-1.4 dB	-1.6 dB	-2.0 dB	-2.3 dB	-2.1 dB
Noise Figures at 60 GHz	0.9 dB	1.2 dB	1.6 dB	2.0 dB	0.9 dB	1.3 dB	1.7 dB	2.2 dB	-
PS-Mode HBM ESD Robustness	0.25 kV	1.5 kV	1.75 kV	2 kV	0.25 kV	1 kV	1.75 kV	2.25 kV	2.5 kV
PD-Mode HBM ESD Robustness	0.25 kV	1.5 kV	2.25 kV	2.5 kV	0.25 kV	1.5 kV	2.25 kV	2.5 kV	3.5 kV
NS-Mode HBM ESD Robustness	0.5 kV	1.25 kV	2 kV	2.25 kV	0.5 kV	1 kV	1.75 kV	2.25 kV	2.75 kV
ND-Mode HBM ESD Robustness	0.25 kV	1.25 kV	2 kV	2.25 kV	0.25 kV	1 kV	1.75 kV	2.25 kV	2.75 kV
Layout Area	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	100x130 μm^2	110x220 μm^2

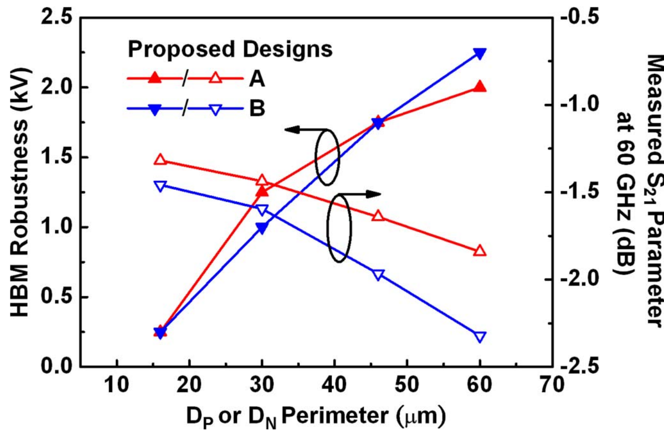
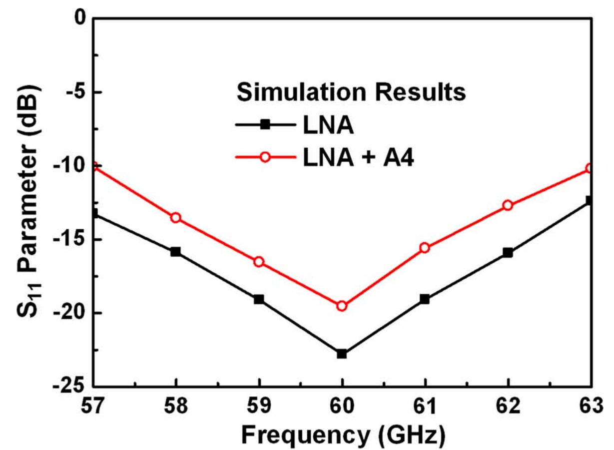


Fig. 10. Dependence of HBM ESD robustness and measured S_{21}-parameters at 60 GHz of ESD protection circuits on different D_P or D_N size.

cannot be ideally 0 dB, since the parasitic resistance of ESD protection diodes (R_{Diodes}), which cannot be eliminated by inductance, also loses the RF signals. At 60 GHz, the test circuits A1, A2, A3, and A4 have about 1.3, 1.4, 1.6, and 1.8-dB insertion loss, respectively, which are summarized in Table II. Table II also lists the measured S_{11}-parameters. All test circuits exhibit good input matching ($S_{11} < -15$ dB) at 60 GHz.

The proposed design B can also reduce the insertion loss at 60 GHz, as shown in Fig. 9. At 60 GHz, the test circuits B1, B2, B3, and B4 have about 1.4, 1.6, 2.0, and 2.3-dB insertion loss, respectively. The slightly increased insertion loss in this design may be due to the more complex metal routing in layout when the series inductor and capacitor connected to V_{DD}.

Under the same bias condition, the noise figures of the ESD protection cells are measured around 60 GHz. At 60 GHz, the



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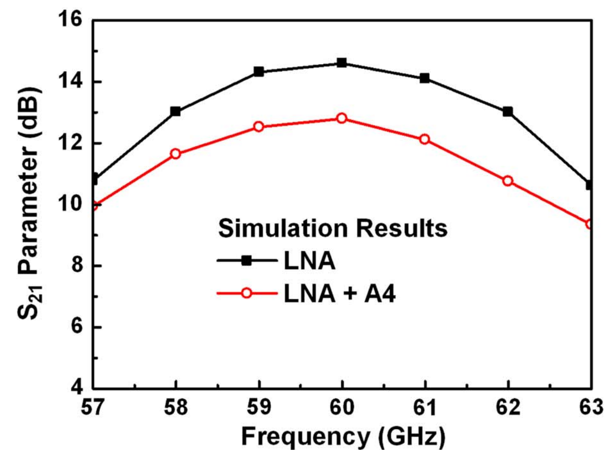

(b)

Fig. 11. Simulation results on (a) S_{11}-parameters, and (b) S_{21}-parameters, of 60-GHz LNA with and without ESD protection.

test circuits A1, A2, A3, and A4 (B1, B2, B3, and B4) have 0.9, 1.2, 1.6, and 2-dB (0.9, 1.3, 1.7, and 2.2-dB) noise figures, respectively.

C. ESD Robustness

ESD robustness of the ESD test circuits with RF-NMOS emulators are evaluated by the ESD tester. The ESD pulses are stressed to each test circuit under PS-mode, PD-mode, NS-mode, and ND-mode ESD stress conditions. The failure criterion is defined as the I–V characteristics seen at RF input shifting over 30% from its original curve after ESD stressed at every ESD test level. The PS-mode, PD-mode, NS-mode, and ND-mode human-body-model (HBM) ESD robustness of all ESD test circuits are measured, as listed in Table II. The HBM ESD robustness of all ESD test circuits can be obtained from the lowest level of PS-mode, PD-mode, NS-mode, and ND-mode ESD robustness. The test circuits A1, A2, A3, and A4 (B1, B2, B3, and B4) have 0.25, 1.25, 1.75, and 2-kV (0.25, 1, 1.75, and 2.25-kV) HBM ESD robustness, respectively.

To investigate the turn-on behavior and the I–V characteristics in high-current regions of the ESD protection cells, the transmission line pulsing (TLP) system with a 10-ns rise time and a 100-ns pulse width is used. The secondary breakdown current (It_2), which indicated the current-handling ability of ESD protection circuit, can also be obtained from the TLP-measured I–V curve. Under PS-mode stress, the test circuits A1, A2, A3, and A4 (B1, B2, B3, and B4) can achieve It_2 of 0.4, 0.9, 1.2, and 1.4 A (0.4, 0.7, 1.2, and 1.5 A), respectively. To evaluate the effectiveness of the ESD protection cells in faster ESD-transient events, another very fast TLP (VF-TLP) system with 0.2-ns rise time and 1-ns pulse width is also used in this study. The test circuits A1, A2, A3, and A4 (B1, B2, B3, and B4) can achieve VF-TLP-measured It_2 of 0.8, 1.5, 1.8, and 2.0 A (0.8, 1.2, 1.8, and 2.1 A), respectively.

D. Comparison

The HBM ESD robustness and the measured S_{21}-parameters at 60 GHz of the proposed ESD protection designs are compared in Fig. 10. Among the proposed designs A and B, the test circuit A4 (B4) can achieve 2-kV HBM ESD robustness with 1.8-dB (2.3-dB) insertion loss.

The comparison among the proposed designs A and B and the reference design [25] is also provided in Table II. The layout area of the proposed designs can be significantly reduced from $110 \times 220\ \mu\mathrm{m}^2$ to $100 \times 130\ \mu\mathrm{m}^2$. Besides, the test circuit A4 can also provide the required 2-kV HBM ESD robustness with the low insertion loss. Therefore, the compact ESD protection circuit for V-band RF applications can be realized by using the test circuit A4. The proposed design can easily be used for ESD protection in the 60-GHz RF LNA.

V. Example of ESD Protection Design Applied to LNA

The LNA circuit shown in Fig. 1 is simulated. Besides, by using the extracted RF characteristics in Section IV, the LNA with the proposed ESD protection design is also simulated. The measured S-parameters of the test circuit A4 are inserted at the input port of the 60-GHz LNA.

Fig. 11 shows the simulated S-parameters of the 60-GHz LNA. As shown in Fig. 11(a), both the stand-alone LNA and the LNA with proposed ESD protection circuit achieve good input matching $(S_{11} < -15\ \mathrm{dB})$ at operating frequency. The LNA without ESD protection circuit achieves 14.6-dB gain (S_{21}) at 60 GHz, as shown in Fig. 11(b). With the ESD protection circuit A4 adding in the LNA, the simulated gain becomes 12.8 dB at 60 GHz. Although the ESD protection circuit slightly degrades the RF performances of LNA, it can provide suitable ESD protection. The proposed ESD protection design in this work has been proved to achieve the required ESD robustness in a compact layout size with little RF performance degradation.

VI. Conclusion

The new compact ESD protection circuits for V-band RF applications have been designed, fabricated, and characterized in a 65-nm CMOS process. These ESD protection circuits are developed to support RF circuit designers for them to easily apply ESD protection in the 60-GHz RF circuits. The proposed ESD protection design uses the inductor, capacitor, and ESD protection diodes, which devices are all provided in the commercial CMOS process. Such compact ESD protection circuits can achieve the 2-kV HBM ESD robustness with 1.8-dB insertion loss and small layout area, which is the useful solution for on-chip ESD protection design for 60-GHz RF applications. Thus, the proposed compact ESD protection design can be used for V-band RF ESD protection.

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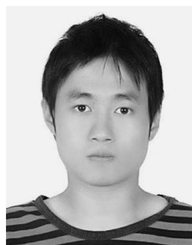

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