Post-Polysilicon Gate-Process-Induced Degradation on Thin Gate Oxide

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***Abstract*— The post-polysilicon gate-process-induced degradation on the underlying gate oxide is studied. The degradation includes an increase in the electron trapping rate and a decrease in the charge-to-breakdown, Q_{bd}, of the gate oxide. It is found that N_2O nitrided gate oxide is more robust than O_2 gate oxide in resisting the degradation. Also, to grow a thin polyoxide on the polysilicon-gate in N_2O rather than in O_2 lessens the degradation on the underlying gate oxide. It is nitrogen, which diffuses through the polysilicon gate and piles up at both polysilicon/oxide and oxide/silicon-substrate interfaces, that improves the oxide quality for the N_2O process.**

I. Introduction

For EPROM and EEPROM memories, the device performance is primarily determined by the electrical properties of the gate oxide [1]. The tunneling oxide between the single-crystal substrate and the first polysilicon film requires a high Q_{bd}. It was reported that for the polysilicon gate structure, a post polysilicon annealing results in degradation on Q_{bd} [2]–[4]. The degradation is related to trap generation and stress built-up in the gate oxide during the high temperature annealing [2]–[4]. Recently, the use of N_2O as either an oxidant or as a post-oxidation annealing ambient to grow oxynitride has received much attention due to its good endurance to Fowler–Nordheim (F–N) stress [5]–[7]. This is due to the incorporation of nitrogen at the oxide/silicon-substrate interface [6]–[8]. However, the post-polysilicon gate-process-induced degradation on the thin gate oxide in the N_2O ambient has not been investigated.

In this letter, the degradation of the thin gate dielectrics induced by growing a thin oxide on the polysilicon gate in N_2O or O_2 ambient is reported for the first time. It is found that N_2O nitrided gate oxide is more robust than O_2 gate oxide in resisting the degradation. Also, growing a thin oxide on the polysilicon-gate in N_2O ambient lessens the degradation on the underlying gate oxide more than growing it in O_2 ambient does.

II. Experiments

Poly-Si gate MOS capacitors were fabricated on ⟨100⟩ p-Si, 15–20 Ω cm wafers. The O_2 gate oxide was grown in dry O_2 at 900°C to a thickness of 85 Å. The N_2O nitrided oxide was first grown in dry O_2 at 900°C followed by an anneal in N_2O for 20 min at the same temperature to control the final oxide thickness of 85 Å. The oxide thickness was determined by C–V measurement. For some samples, a thin polyoxide on the polysilicon gate was grown in O_2 or N_2O ambient at 900°C for 30 min after 3000 Å polysilicon deposition, to simulate the inter-polyoxide in the EEPROM process [1], [2]. As shall be shown later, degradation was induced on the underlying gate dielectric by this thermal cycle.

The preparation sequences for these samples are summarized in Table I. Six groups of samples were prepared: three for O_2 oxides and three for N_2O nitrided oxides. The O_2 oxide samples are denoted as OP (without grown thin polyoxide), OPN (thin polyoxide grown in N_2O), and OPO (thin polyoxide grown in O_2). The N_2O nitrided oxide grown samples are denoted as ONP (without grown thin polyoxide), ONPN (thin polyoxide grown in N_2O), and ONPO (thin polyoxide grown in O_2). The thin polyoxides were removed in a dilute HF solution and all samples were $POCl_3$-doped at 950°C for 15 min and metallized and patterned to form MOS capacitors.

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III. Results and Discussions

Fig. 1 shows the gate voltage shifts under constant current (100 mA/cm^2) stressing. All N_2O nitrided oxides showed smaller electron trapping rates than their corresponding O_2 oxides. This was due to nitrogen incorporation at the oxide/Si-substrate interface of the N_2O samples [6]–[8]. The OP and ONP samples, which had no thin polyoxides grown on the polysilicon gate, showed lower electron trapping rates than their corresponding samples: OPN, OPO, and ONPN, ONPO, respectively, which had thin polyoxides. Therefore, the process of growing a thin polyoxide on poly-Si gate causes degradation on the underlying gate oxide. The degradation is caused by stress built-up at polysilicon/oxide and oxide/silicon-substrate interfaces [4]. In this figure, it is also seen that N_2O nitrided oxides (ONPN and ONPO) show less degradation than their corresponding O_2 oxides (OPN and OPO). This indicates that N_2O nitrided oxide is more robust than O_2 oxide. The degradation caused by growing a thin polyoxide in N_2O (i.e., samples OPN and ONPN) is less than that caused by growing a thin polyoxide in O_2 (i.e., samples OPO and ONPO). Therefore, growing the polysilicon-gate oxide in N_2O lessens the degradation than growing it in O_2. Fig. 2 shows Weibull plots of Q_{bd} of all samples under 100 mA/cm^2 stressing for 40 capacitors. For O_2 oxides, OPN showed little degradation on

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TABLE I
THE PREPARATION SEQUENCES FOR SAMPLES IN THIS STUDY

Samples	Gate dielectrics O_2 oxidation	N_2O annealing	Poly-Si gate	Thin poly-oxide grown on poly-Si gate
OP	√	-	√	-
OPN	√	-	√	√ (N_2O)
OPO	√	-	√	√ (O_2)
ONP	√	√	√	-
ONPN	√	√	√	√ (N_2O)
ONPO	√	√	√	√ (O_2)

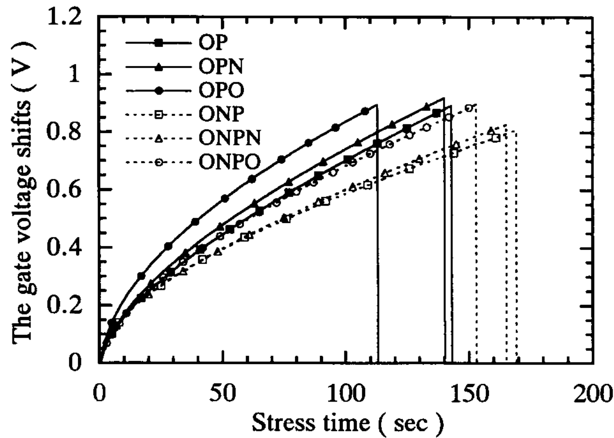

Fig. 1. The gate voltage shifts under 100 mA/cm^2 stressing from gate injection for all samples. The gate area was 5×10^{-4} cm^2.

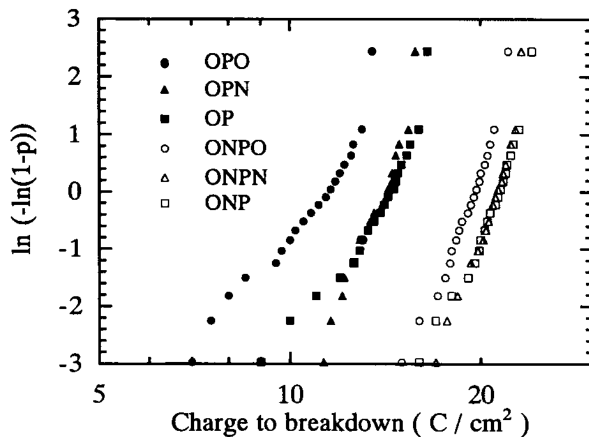

Fig. 2. The Weibull plots for the Q_{bd} of all samples. The stressing condition was 100 mA/cm^2 injected from the gate and the gate area was 5×10^{-4} cm^2.

Q_{bd} but OPO had significant degradation. For N_2O nitrided oxides, there was little degradation on ONPN and slight degradation on ONPO. This is consistent with the result of Fig. 1 since Q_{bd} is related to electron trapping in the oxide [3].

An OPN sample with a gate oxide of 100 nm thick was SIMS analyzed to obtain its oxygen and nitrogen depth profiles which were shown in Fig. 3. The use of a thick gate oxide is to ensure adequate depth resolution. For the SIMS sample, the N_2O annealing was done at 900°C for 60 min, which was 30 min longer than the 8.5 nm oxide (OPN sample). This nitrogen profile is quite similar to that of nitrogen ion implantation through-silicon-gate where the gate oxide integrity was significantly improved [9]. We conclude that during the N_2O annealing or oxidation, nitrogen diffuses through poly-Si gate and piles up at both the poly-Si/oxide and oxide/Si-substrate interfaces, improving the oxide quality.

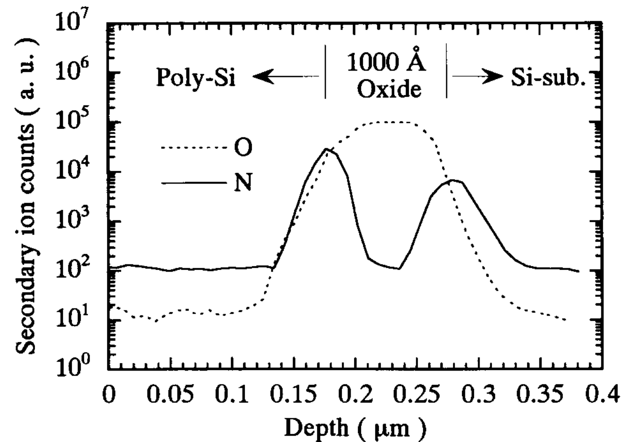

Fig. 3. The nitrogen and oxygen SIMS profiles of an OPN sample with a gate oxide thickness of 1000 Å. The use of a thick gate oxide is to ensure adequate depth resolution. The post-polysilicon N_2O anneal condition was 900°C for 60 min. Nitrogen piled up at both the poly-Si/oxide and oxide/Si-substrate interfaces.

IV. SUMMARY

The post-polysilicon gate oxidation causes degradation on the underlying gate oxide. It causes both an increase in the electron trapping rate and a decrease in Q_{bd}. For the underlying gate dielectric, it is found that N_2O nitrided gate oxide is more robust than O_2 gate oxide in resisting this degradation. For the post-polysilicon gate oxidation, growing a thin oxide on poly-Si gate in N_2O rather than in O_2 lessens the degradation on the underlying gate oxide. The nitrogen, which diffuses through the polysilicon gate and piles up at both oxide interfaces, results in superior reliability properties.

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