Dual cross-coupling LNA with forward body bias technique

Chia-Hung Chang, Tao Wang and Christina F. Jou

A fully integrated low-power LNA with dual cross-coupling and forward body bias (FBB) techniques is presented. The first cross-coupling circuit is applied at the transconductance stage. By connecting body nodes to each other's source terminals, the body cross-coupling network forms the gate-driven and body-driven simultaneously input stage to gain its effective transconductance, which in turn improves the noise performance and decreases current consumption. In addition, the second capacitor cross-coupling configuration is applied at the input stage to form a feed-forward connection, which results in not only boosting the effective transconductance, but also reducing the influence of the gate noise from the input transistors as well. Moreover, to decrease the overall power consumption further, the FBB technique is employed to lower the supply voltage. The measured noise figure is lower than 3.38 dB and the core circuit consumes only 2.16 mW.

Introduction: The tendency towards low power for a front-end LNA is required in wireless communication. As a consequence, maintaining the same performance with less power consumption is desirable for portable devices. Several low-power LNAs have been reported to meet the demands of saving power in recent years. Decreasing the supply voltage is an efficient way to lessen power dissipation. However, an insufficient overdrive voltage causes a poor linearity. Although the LNA without a cascode transistor increases the headroom, it cannot provide better isolation, higher output resistance, and minimised Miller effect. Forward body bias (FBB) is one of the solutions to achieve low supply voltage [1–3]. By providing a DC voltage to control the forward bias of the P-N junction, threshold voltage, V_{th}, is decreased and then low supply voltage operation is acceptable to mitigate the problem of inadequate voltage headroom. In this reported work, the proposed fully differential LNA incorporates both dual cross-coupling (DCC) and FBB to diminish power dissipation. Moreover, the LNA with a current-reused topology performs with low power consumption without degrading gain and noise performance due to the DCC technique.

LNA circuit design: Fig. 1 shows the proposed LNA. The core circuit comprises three techniques to lower power dissipation. The first one is body cross-coupling [4], which is applied at the transconductance stage by connecting the body and source terminals of each MOSFET. The configuration forms the dual driven input stages. The input impedance, Z_{in}, has been hence turned into $1/(g_{m1}+g_{mb1})$, where g_{mb1} is the body transcondance. Furthermore, the input transconductance, G_{m1}, is also boosted from g_{m1} to $g_{m1}+g_{mb1}$. Assuming the ratio of g_{mb1} and g_{m1} is approximatly 0.15, G_{m1} can be improved by 15% without additional power consumption due to the body cross-coupling. Consequently, insufficient voltage gain could be relieved in the low power design.

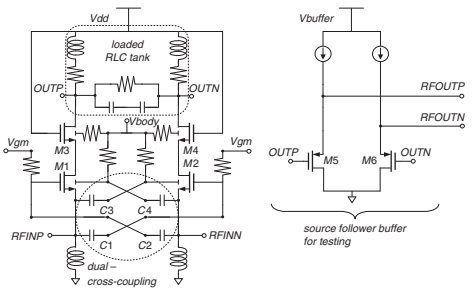

Fig. 1 *Schematic of proposed LNA and its testing buffer*

A capacitor cross-coupled common-gate configuration is the second means to decrease overall power dissipation. $C1$ and $C2$ are employed to allow differential input voltage to drop across the gate and source terminals of each input transistor. If the coupling factor, $C_1/(C_{gs1}+C_1)$, is equivalent to 1, the effective transconductance, $G_{m1,eff}$, can be further increased by a factor of 2 because of the feed-forward connection [5]. Therefore, combining body cross-coupling and capacitive cross-coupling in the input transconductance stage, the $G_{m1,eff}$ is approximately 2.3 times the g_{m1}, which in turn decreases the current dissipation and increases the entire voltage gain. If the coupling capacitor is large enough and the input impedance is perfectly matched, the overall differential voltage gain of the LNA at resonance can be $A_{diff,voltage} = 4G_{m1,eff}R_L/(1+2G_{m1,eff}R_S) \fallingdotseq 2R_L/R_S$, where R_S is the source impedance, 50 Ω, and R_L is the load impedance. To achieve an input impedance match, the boosted effective transcondance, $2G_{m1,eff} = g_{m1}+g_{mb1}$, is designed as the inverse of the R_S. Hence, a 20 dB voltage gain at resonance can be obtained by choosing $R_L = 250$ Ω. In this case, suppose the overdrive voltage and supply voltage are 0.25 V and 0.9 V, respectively, only a 1.6 mA of the current consumption is required to achieve adequate gain. In comparison to the conventional common-gate amplifier, the proposed DCC LNA mitigates the requirement of the power substantially under the same voltage gain.

Fig. 2 shows the input referred noise analysis of the proposed LNA with load resistors at resonance. If the channel length modulation and flicker noise contributions are neglected, the input referred noise voltage and current are obtained. The equation is hence expressed as $NF = 10log\{1+(4/3)(1/G_{m1,eff}R_S)(g_{m1}/G_{m1,eff})+[(1/G_{m1,eff}R_S)^2+1](2R_S/R_L)\}$, which reveals that the noise contributions are in terms of the $G_{m1,eff}$, R_S, and R_L. Assuming $G_{m1,eff} = 1/R_S = 50$ Ω, $g_{m1}/G_{m1,eff} = 1/2.3$, $R_S = 50$ Ω and $R_L = 250$ Ω, a typical value gives the $NF = 3.765$ dB. To improve the noise performance further, the $G_{m1,eff}$ and R_L have to be large enough. Accordingly, for the consideration of the trade-off between input return loss and NF, the source impedance can be less than 50 Ω on condition that S_{11} is less than −10 dB, which allows a larger $G_{m1,eff}$ value to reduce NF. Thanks to the DCC scheme, the second term can be further improved because the $G_{m1,eff}$ is boosted by a factor of 2.3 and the ratio of g_{m1} and $G_{m1,eff}$ is approximately 0.435. Thus, the boosted $G_{m1,eff}$ without consuming extra DC current or increasing the transistor's size is well suitable for the low power design.

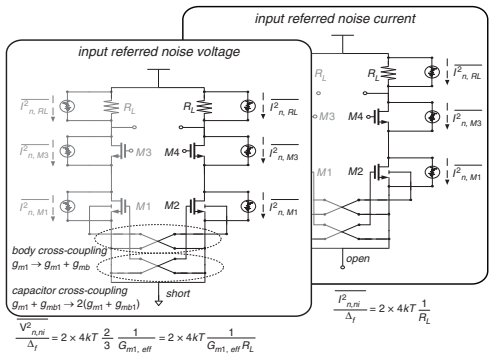

Fig. 2 *Input referred noise analysis at resonance*

The third design technique applies FBB to the input and cascode stages. By biasing the body-source voltage, V_{BS}, the V_{th} of the transistors can be decreased, thereby enabling a lower supply voltage design. However, a relatively low V_{th} causes a higher leakage current. Thus, a limited V_{th}, which is below the P-N junction voltage, is acceptable to meet a negligible leakage current. The well-known I-V characteristic equation of the P-N junction is defined as $I_{leakage} = I_S(\exp(V_{BS}/nV_T)-1)$, where I_S is the reverse bias saturation current, n is the ideality factor and V_T is the thermal voltage. Supposing $I_S = 10^{-12}$ A for silicon diodes, ideality factor $n = 1.5$, body to source voltage $V_{BS} = 0.6$ V, and $V_T = 25.85$ mV at 300K room temperature, approximately only 12.5 μA leakage current is introduced because of FBB. As a result, for the consideration of $V_{BS} \leq 0.6$ V, the simulated FBB voltages against overall NFs and drain currents with different gate to source voltages, V_{gs}, from the g_m stage are shown in Fig. 3. The noise performance can be improved with a larger V_{BS} because the drain current is increased by the decreased V_{th}. Moreover, the noise contribution is further reduced by increasing V_{gs} and then boosting the transconductance. Based on the above NF equation, the transconductance is inversely proportional to the NF. Therefore, a proper V_{BS} drives the operation of the transistors from weak inversion into strong inversion, resulting in a better noise performance and voltage gain at the lower supply voltage. Furthermore, the deep N-well MOSFET is employed at the transconductance and cascode stages to separate its body region and degrade the noise source from the substrate coupling [6]. To diminish the overall power consumption,

the lower supply voltage is performed by adjusting the V_{BS} and the transconductance is enhanced by means of the DCC technique.

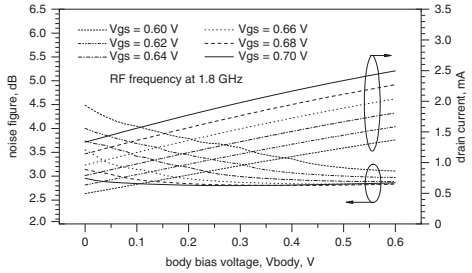

Fig. 3 *Simulated NF and drain current characteristics of g_m stage*

Measurement results: A fully differential low-power LNA with DCC and FBB techniques was fabricated using standard 0.25 μm CMOS technology. Fig. 4 shows the chip photograph. The chip occupies 1.23 mm^2 of chip area including bonding pads. The external 180° hybrid baluns are also used at the LNA inputs and outputs, respectively. The power consumption of the core circuit is 2.16 mW at the supply voltage 0.863 V.

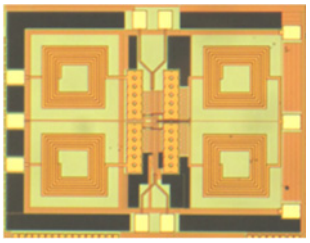

Fig. 4 *Chip photograph*

The measured S_{11} and S_{21} of the LNA can be less than −10 dB and higher than 9.5 dB, respectively. The de-embedded NF from the loss of the external balun is lower than 3.38 dB at the highest power gain due to the proposed DCC. To compare with the performance of other FBB LNAs [7–8], a figure of merit (FOM) [9] is proposed to evaluate each characteristic. Table 1 summarises the performances and compares these with other FBB LNAs. Combining the three techniques achieves relatively low power consumption without suffering from degradation of its performance. The FOM of 1.93 in this work is hence better than others.

Table 1: Chip performance and comparison with other FBB LNAs

Parameter	This work	[1]	[2]	[3]	[7]	[8]
Frequency (GHz)	1.8	5	6.5	0.4–0.9	5.1	5.2
S_{21} (dB)	9.5	10.23	16	20	10.3	10
S_{11} (dB)	<−10	−17.9	<−12	<−10	−17.7	−13.4
NF (dB)	3.38	4.1	3.4	2.95	5.3	3.37
IP1dB (dBm)	−10	−23.8	N/A	N/A	−22	−18
IIP3 (dBm)	−0.4*	−15	−13	N/A	−12.4*	−8.6
Area (mm^2)	1.23	0.792	0.62	0.07	1.15	0.78
Power (mW)	2.16	0.8	4.5	0.385	1.03	1.08
FOM	1.93	0.41	0.38	N/A	0.39	1.79

*Estimated from IIP3 = IIP1 + 9.6 dB

Conclusion: A fully integrated low power LNA using DCC and FBB techniques is proposed. A low supply voltage design is realised by the FBB scheme, which decreases V_{th} and then drives the transistors into strong inversion. Moreover, both the body cross-coupling and the capacitor cross-coupling provide an adequate power gain with relatively lower DC dissipation and improve noise performance. To demonstrate the properties of DCC and FBB, the proposed LNA with power consumption of only 2.16 mW and a FOM of 1.93 is analysed and designed.

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One or more of the Figures in this Letter are available in colour online.

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References

1 Chang, C.-P., Chen, J.-H., and Wang, Y.-H.: 'A fully integrated 5 GHz low-voltage LNA using forward body bias technology', *IEEE Microw. Wirel. Compon. Lett.*, 2009, **19**, (3), pp. 176–178
2 Li, C.-M., Li, M.-T., He, K.-C., and Tarng, J.-H.: 'A low-power self-forward-body-bias CMOS LNA for 3–6.5 GHz UWB receivers', *IEEE Microw. Wirel. Compon. Lett.*, 2010, **20**, (2), pp. 100–102
3 Liu, J., Liao, H., and Huang, R.: '0.5 V ultar-low power wideband LNA with forward body bias technique', *Electron. Lett.*, 2009, **45**, (6), pp. 289–290
4 Chatterjee, S., Tsividis, Y., and Kinget, P.: '0.5-V analog circuit techniques and their application in OTA and filter design', *IEEE J. Solid-State Circuits*, 2005, **40**, (12), pp. 2373–2387
5 Zhuo, W., Li, X., Shekhar, S., Embabi, S.H.K., de Gyvez, J.P., Allstot, D.J., and Sánchez-Sinencio, E.: 'A capacitor cross-coupled common gate low noise amplifier', *IEEE Trans. Circuits Syst. II, Express Briefs*, 2005, **52**, (12), pp. 875–879
6 Yeh, W.K., Chen, S.M., and Fang, Y.K.: 'Substrate noise-coupling characterization and efficient suppression in CMOS technology', *IEEE Trans. Electron Devices*, 2004, **51**, (5), pp. 817–819
7 Wu, D., Huang, R., Wong, W., and Wang, Y.: 'A 0.4-V low noise amplifier using forward body bias technology for 5 GHz application', *IEEE Microw. Wirel. Compon. Lett.*, 2007, **17**, (7), pp. 543–545
8 Hsieh, H.-H., Wang, J.-H., and Lu, L.-H.: 'Gain-enhancement techniques for CMOS folded cascode LNAs at low-voltage operations', *IEEE Trans. Microw. Theory Tech.*, 2008, **56**, (8), pp. 1807–1816
9 Linten, D., Aspemyr, L., Jeamsaksiri, W., Ramos, J., Mercha, A., Jenei, S., Thijs, S., Garcia, R., Jacobsson, H., Wambacq, P., Donnay, S., and Decoutere, S.: 'Low-power 5 GHz LNA and VCO in 90 nm RF CMOS'. VLSI Circuits, Symp. 2004, Dig. Tech. Pprs., Honolulu, HI, USA, 2004, pp. 372–375