Superior Low-Pressure-Oxidized Si_3N_4 Films on Rapid-Thermal-Nitrided Poly-Si for High-Density DRAM's

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***Abstract*— High-performance stacked storage capacitors with small effective-oxide-thickness ($t_{ox,eff}$) as thin as 37 Å has been achieved using low-pressure-oxidized nitride films deposited on NH_3-nitrided poly-Si electrodes. The capacitors exhibit excellent leakage property and time-dependent-dielectric-breakdown (TDDB) characteristics. Furthermore, this technique is promising for the 64- and 256-Mb dynamic-random-access-memory (DRAM) applications because the process temperatures never exceed 850°C.**

I. Introduction

For 64 Mb DRAM's and beyond, the drastic reduction in cell size has necessitated three dimensional cell structure and high-performance ultrathin capacitor dielectrics. The CVD-Ta_2O_5 film on smooth poly-Si was shown to possess high capacitance, but high leakage current and process-induced degradation were inevitable and needed to be conquered [1]. Conventional oxide/nitride (ON) stacked dielectric has been extensively utilized as stacked cell capacitors because of its low defect density, high breakdown field and reliability. However, limitations of capacitance increase and leakage reduction still exist [2]. Many methods have been proposed to improve the properties of ON dielectric [3], [4]. The ON films fabricated by rapid-thermal-processing have been shown to express excellent characteristics for DRAM applications [5], [6]. Nevertheless, thermal stress and high temperature treatment will cause serious problems. Recently, a novel technique to fabricate superthin oxide/nitride/oxide (ONO) stacked dielectric has been proposed by oxidizing very thin Si_3N_4 at low pressure on silicon substrate [7]. This dielectric exhibited not only high maximum attainable capacitance ($t_{ox,\,eff} \sim 46$ Å) but also low leakage current and high reliability.

In this letter, by using rapid thermal nitridation (RTN) of smooth poly-Si films prior to Si_3N_4 deposition to avoid the native oxide formation, [8], [9], high-performance dielectrics with even higher-capacitance ($t_{ox,\,eff} \sim 37$ Å) can be fabricated after the low pressure oxidation of the nitride films under the processing temperature of 850°C.

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II. Experimental Procedures

Capacitors with doped smooth poly-Si bottom electrodes were fabricated on Si substrates covered with SiO_2. A 3000 Å-thick LPCVD poly-Si was deposited at 620°C using pure SiH_4 gas. Subsequently, $POCl_3$-diffused, p-glass stripped and then these wafers were cleaned by standard RCA procedures. Prior to LPCVD Si_3N_4 deposition, the samples received RTN in pure NH_3 at 850°C for 60 s. After 30 Å-thick Si_3N_4 deposition, low-pressure oxidation was performed at 850°C, 0.5 Torr for 30 min, followed by top poly-Si deposition, doping, and patterning. Both the top and bottom poly-Si layers were $POCl_3$-doped at 850°C. For comparison, capacitors with the 50 Å-thick pure Si_3N_4 films on the RTN-treated poly-Si were formed. Consequently, capacitance-voltage (C-V) measurements revealed that the effective oxide thicknesses ($t_{ox,\,eff}$) for the dielectrics with low-pressure oxidized Si_3N_4 and pure nitrides were 37.2 and 36.1 Å, respectively. In such a case, the effective oxide thickness is calculated from the capacitance using the oxide dielectric constant of 3.9. The breakdown field (E_{bd}) is defined as the breakdown voltage (V_{bd}) divided by $t_{ox,\,eff}$ and the effective electric field (E_{eff}) is therefore defined as the gate voltage divided by $t_{ox,\,eff}$.

III. Results and Discussion

Fig. 1 compares the cumulative failure rates under ramp-voltage test for the capacitors with the low-pressure-oxidized Si_3N_4 (LPON) and pure nitride (PN) films under both gate polarities. For each type of samples, 15 capacitors were tested to construct the breakdown statistics. Obviously, the capacitors with LPON show larger breakdown fields (E_{BD}) for both polarities than those with PN. For the negative gate-bias ($-Vg$), the Weibull distribution of the capacitors with LPON is similar to that with PN. In contrast, the capacitors with PN express a wider range of Weibull than those with LPON for positive gate-bias ($+Vg$). Low pressure oxidation of nitride films has been reported to be able to grow the oxide on the top and bottom of the nitride layers [7]. Therefore, an ONO structure is surmised to result in the higher and tighter electrical-breakdown-field (E_{BD}) distribution for the capacitors with LPON under both polarities. In addition, since the bottom native oxide has been eliminated by RTN, it is also found that all the capacitors with LPON and PN layers exhibit the breakdown field higher than 8 MV/cm. These results are consistent with previous research [4].

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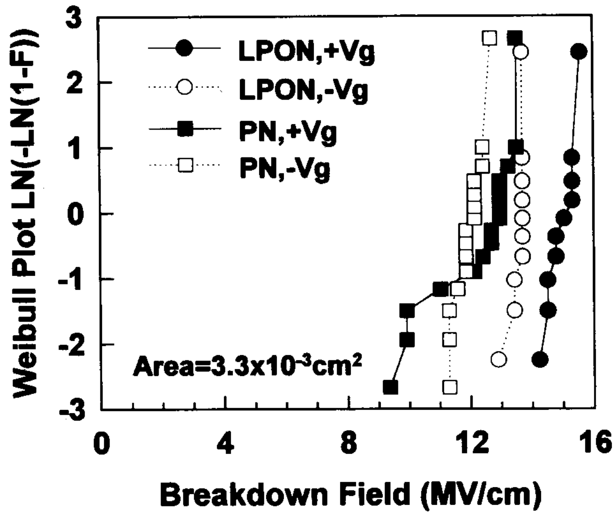

Fig. 1. The cumulative failure rates under ramp-voltage test for the capacitors with the low-pressure oxidized Si_3N_4 (LPON) and pure nitride (PN) under both gate polarities.

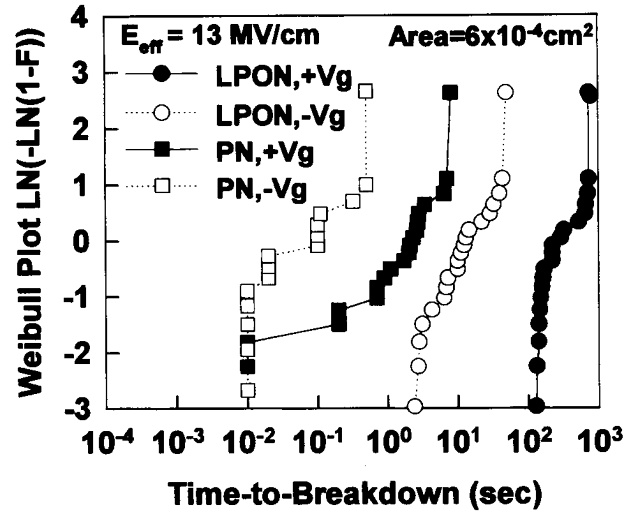

Fig. 3. Weibull plots of TDDB characteristics under constant electric field stress ($E_{\text{eff}} = 13$ MV/cm) for the capacitors with LPON and PN under both gate polarities.

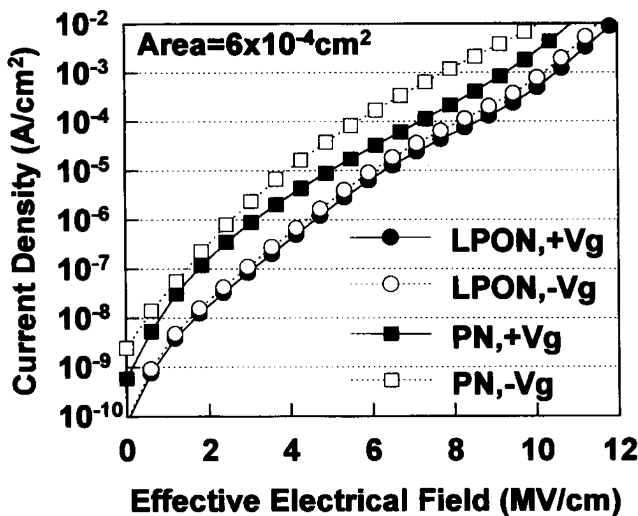

Fig. 2. The curves of current-density versus electrical-field (J–E) for the capacitors with LPON and PN biased at both gate polarities.

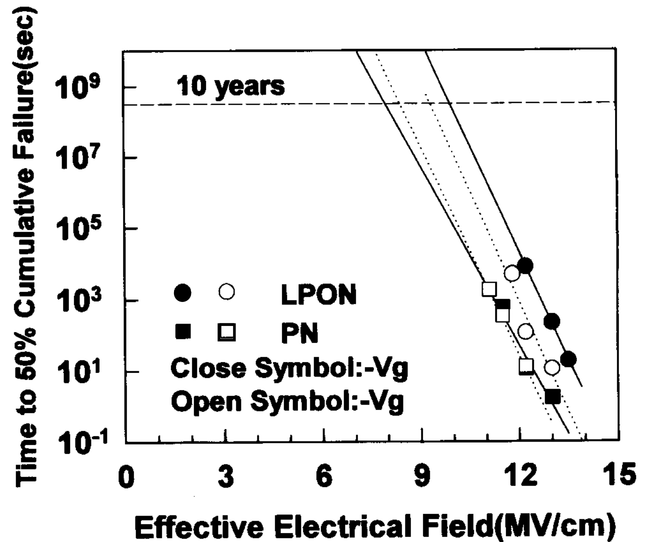

Fig. 4. The TDDB lifetime extracted from the time-to-50% cumulative-failure as a function of applied field E_{eff}.

The curves of current-density versus electrical-field (J-E) for the capacitors with LPON and PN biased at both gate polarities are shown in Fig. 2. A significant reduction in leakage current is also observed for the capacitors with LPON for both gate polarities as compared to those with PN. RTN prior to Si_3N_4 deposition has been reported to be a useful technique for reducing low-field leakage current [3]. However, low-pressure oxidation of nitride can further decrease leakage current without sacrificing the increased $t_{\text{ox, eff}}$. For the capacitors with LPON, the current densities at +1.65 V and −1.65 V are 0.74×10^{-6} A/cm² and 1.04×10^{-6} A/cm², respectively, fulfilling the requirement of 64 Mb DRAM's. Moreover, the current densities at +0.75 V and −0.75 V are 1.65×10^{-8} A/cm² and 2.10×10^{-8} A/cm², accordingly. The reduction in leakage current for the LPON is believed to be due to the formation of ONO stacked structure.

Weibull plots of TDDB characteristics under constant electric field stress ($E_{\text{eff}} = 13$ MV/cm) for the capacitors with LPON and PN under both gate polarities are shown in Fig. 3. Both gate biases were applied on the capacitors with an area of 6×10^{-4} cm². The capacitors with LPON have a longer t_{BD} as well as tighter t_{BD} distribution than those with PN. This result is consistent with the outcome of the ramp-voltage tests, i.e., the breakdown field plots. Hence, LPON is an effective method for reducing the defect density and improving the reliability.

Fig. 4 shows the TDDB lifetime extracted from time-to-50% cumulative-failure as a function of applied E_{eff}. The area of the measured capacitors is 6×10^{-4} cm². Capacitors with LPON show much longer t_{BD} than those with PN at the same effective electric field for both gate polarities. The long-term lifetime can be predicted by using this figure and the capacitors with LPON are estimated to survive long enough for more than 10 years at a stress field of ~10 MV/cm.

IV. Conclusions

In summary, the low-pressure oxidation of ultrathin nitrides on the RTN-treated smooth poly-Si exhibits high capacitance ($t_{ox, eff} \sim 37$ Å), low leakage current, and high reliability. Since the properties of the dielectrics can satisfy the requirements of 64 Mb DRAM's, this technology is promising for future high-density DRAM application.

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