area performance of the proposed array is $O(N^2\log_2 N)$ and the time performance is $O(\log_2 N)$. Thus, the resulting (area × time)^2 is $O(N^2\log_2{}^3 N)$, which is < $O(N^3\log_2{}^3 N)$ achieved by the arrays in [8, 9]. The features of high throughput performance and low area-time complexity make the proposed array useful for very high speed applications. It is also worth noting that the design for the 1-D IDCT can be directly applied to evaluate the 2-D IDCT based on row-column decomposition.

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Yu-Tai Chang and Chin-Liang Wang (*National Tsing Hua University, Institute of Electrical Engineering, Hsinchu, Taiwan 30043, Republic of China*)

Chin-Liang Wang: corresponding author

E-mail: clwang@ee.nthu.edu.tw

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Unified array architecture for discrete cosine transform, sine transform and their inverses

Jiun-In Guo, Chingson Chen and Chein-Wei Jen

Indexing terms: Discrete cosine transforms, Sine transforms, Systolic arrays

A unified array design for the discrete cosine transform, discrete sine transform and their inverses based on a new general formulation is presented. The presented design provides the flexibility to adaptively select different types of transforms in transform coding according to the characteristics of images for minimising the bit rate as much as possible.

Introduction: In transform coding, the discrete cosine transform (DCT) and discrete sine transform (DST) have been widely used owing to the good performance and acceptable computational complexity as compared with the statistically optimal Karhunen-Loeve transform (KLT) [1 – 3]. To meet the speed requirement of real-time applications, dedicated DCT or DST hardware designs are developed [4 – 8], (see references in [2, 3, 9]). Owing to the different properties of the transform kernels, there are different applications for the DCT and DST. For images with high correlation coefficients, e.g. $\rho \geq 0.9$, using DCT yields better performance. On the other hand, for images with low correlation coefficients, e.g. $|\rho| < 0.5$, using DST yields lower bit rates [2]. Therefore, to minimise the bit rates of encoded images in transform coding, a flexible transform hardware which can adaptively perform different transform functions is inevitable.

We present a unified array design for the DCT, DST, and their inverses according to a new general formulation. The presented design provides the flexibility to adaptively select different types of transforms in transform coding according to the characteristics of images such that the bit rate can be minimised as much as possible. Compared with the dedicated DCT or DST hardware designs proposed in the literature, the presented design possesses higher flexibility with respect to different characteristics of images and different applications.

Algorithm derivation: The DCT and DST of a 1-D N-point sequence $\{y(n)\}$ can be generally expressed as

$$Y(k) = \sqrt{\frac{2}{N}}\epsilon_k \sum_{n=i}^{j} y(n)C(n,k) \quad k = i, ..., j \qquad (1)$$

and the inverse transforms can be shown as

$$y(n) = \sqrt{\frac{2}{N}} \sum_{k=i}^{j} \epsilon_k Y(k)C(n,k) \quad n = i, ..., j \qquad (2)$$

where

$$\{i, j, C(n,k)\} = \left\{ \begin{matrix} 1 & N-1 & \cos\left(\frac{(2n+1)k\pi}{2N}\right) & DCT/IDCT \\ 1 & N & \sin\left(\frac{(2n-1)k\pi}{2N}\right) & DST/IDST \end{matrix} \right\}$$

and $\epsilon_k = 1/\sqrt{2}$ if $k = 0$ (for DCT/IDCT) or $k = N$ (for DST/IDST) and $\epsilon_k = 1$, otherwise. If we neglect the scaling factor $\sqrt{(2/N)}$ and introduce a variable $x(n)$ for DCT/DST and a variable $t(n)$ for IDCT/IDST, we can formulate eqns. 1 and 2 as

$$\begin{aligned} Y(k) &= [2T(k) + \alpha(k)]\beta(k) \\ T(k) &= \sum_{n=1}^{N-1} x(n) \cos\left(\frac{nk\pi}{N}\right) \quad k = 1, ..., N-1 \\ Y(0) &= \sum_{n=0}^{N-1} y(n) \\ Y(N) &= \sum_{n=1}^{N} (-1)^{n+1} y(n) \end{aligned} \qquad (3)$$

and

$$\begin{aligned} t(n) &= 2T(n) + \sqrt{2}\delta(n) \\ T(n) &= \sum_{k=1}^{N-1} Z(k) \cos\left(\frac{nk\pi}{N}\right) \quad n = 1, ..., N-1 \end{aligned} \qquad (4)$$

respectively, where

$$\{\alpha(k), \beta(k), \delta(n), Z(k)\} = \left\{ \begin{matrix} x(0) & \cos\left(\frac{k\pi}{2N}\right) & Y(0) & Y(k)\cos\left(\frac{k\pi}{2N}\right) & DCT/IDCT \\ (-1)^k x(N) & -\sin\left(\frac{k\pi}{2N}\right) & (-1)^n Y(N) & Y(k)\sin\left(\frac{k\pi}{2N}\right) & DST/IDST \end{matrix} \right\}$$

and the variable $x(n)$ is defined as

$$\begin{pmatrix} x(N-1) = y(N-1) \\ x(n) = y(n) - x(n+1) \quad n = 0, 1, ..., N-2 \end{pmatrix} \qquad (5)$$

in the DCT case and

$$\begin{pmatrix} x(1) = y(1) \\ x(n) = y(n) + x(n-1) \quad n = 2, 3, ..., N \end{pmatrix} \qquad (6)$$

in the DST case. The relationship between the variables $t(n)$ and $y(n)$ is shown as

$$\begin{pmatrix} t(0) = 2y(0) \\ t(n) = y(n) + y(n+1) \quad n = 1, 2, ..., N-1 \end{pmatrix} \qquad (7)$$

in the IDCT case and

$$\begin{pmatrix} t(N) = -y(N) \\ t(n) = y(n+1) - y(n) \quad n = 1, 2, ..., N-1 \end{pmatrix} \qquad (8)$$

in the IDST case. There is a common 1-D transform $T(\cdot)$ in the above equations. That is, we can realise the DCT, DST, IDCT, and IDST based on a unified algorithm.

Architecture design: Based on the unified algorithm, we present an array design for the 1-D eight-point DCT, DST, IDCT and IDST. The design is composed of two parts: the array stage and the processing stage, as shown in Fig. 1*a*. The array stage, which realises the 1-D transform $T(\cdot)$, is implemented by using the distributed arithmetic (DA) scheme [7, 9], which is shown in Fig. 1*b*. The

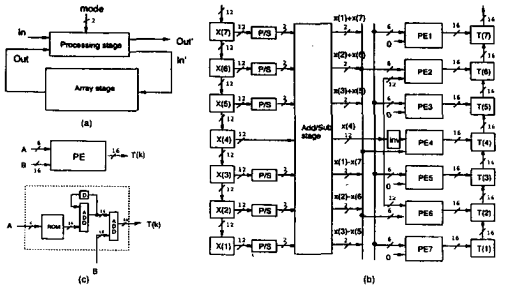

Fig. 1 *Block diagram of proposed array, architecture of array stage in proposed design and structure of PEs*

a Block diagram of proposed array
b Architecture of array stage in proposed design
c Structure of PEs

structure of the processing elements (PEs) which are composed of small ROMs and adders, is shown in Fig. 1*c*. Using the DA scheme can effectively reduce the hardware cost and give good numerical accuracy [7]. The processing stage performs all the preprocessing and postprocessing operations in the algorithm. It contains a multiplier, adder/subtractors, memory modules and multiplexing circuits, as shown in Fig. 2. The values of the control signals $\{C_i, i = 1,..., 6\}$ are summarised in Table 1. This array design has been verified through the computer simulation of VERILOG codes.

Table 1: Values of control signals in processing stage

Signal	8 consecutive values	DCT	DST	IDCT	IDST
C1	10101010		√		√
	00000000	√		√	
C2	10000000	√			
	00000001		√		
	00000000			√	√
C3	10101010		√		
	00000000	√			
C4	10000000			√	√
	00000000	√	√		
C5	10000000	√	√	√	√
C6	11111111	√			
	00000000		√		

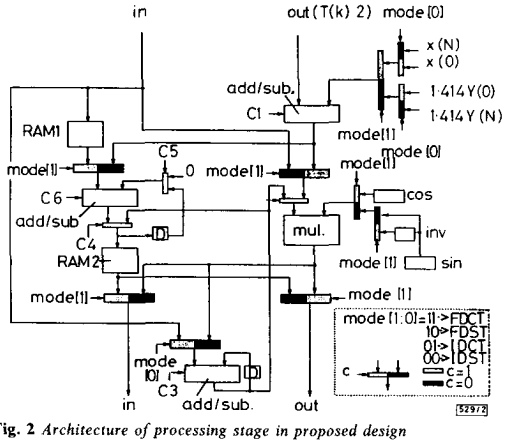

Fig. 2 *Architecture of processing stage in proposed design*

Conclusion: In the literature, there is a unified systolic array proposed for the DCT and DST [8]. The basic motivation of the design in [8] is the same as that of the presented design, but the methods are different. The design in [8] adopts a recursive algorithm to compute the DCT and DST, which eliminates the memory access time compared with the designs which store the transform kernels in memory. However, this memory access time is short since most DCT and DST designs use small memory modules. Moreover, the design in [8] should entail much hardware cost in VLSI implementation for the recursive generation of the transform kernels. In summary, the presented design not only possesses high functional flexibility, but also minimises the hardware cost.

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Jiun-In Guo (*Department of Electronics Engineering, Lien-Ho Junior College of Technology, Miao-Li, Taiwan, Republic of China*)

Chingson Chen and Chein-Wei Jen (*Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China*)

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Relative permittivity measurement of thick-film dielectrics at microwave frequencies

H. Huang, C.E. Free, K.E.G. Pitt, A.R. Berzins and G.P. Shorthouse

Indexing terms: Permittivity measurement, Cavity resonators, Thick film capacitors, Microwave measurements

A novel extension of the resonant cavity technique used to measure relative permittivity at microwave frequencies is presented. The new technique is aimed particularly at the measurement of very thin dielectric layers and has been used to measure the permittivity of a thin dielectric layer printed onto a thick substrate whose permittivity is known. Successful experimental data has been obtained for 100μm thick dielectrics at X-band.

Introduction: Multilayer transmission lines using thin dielectric layers are commonly used as part of the high density interconnection structure found in modem multichip modules (MCMs). MCM devices are increasingly used for high speed data applications, and to properly characterise these devices, the performance of the dielectric layer at high frequencies needs to be precisely established [1, 2]. Various methods have been employed for the measurement of permittivity of sheet and plate materials at microwave frequencies [3 – 5]. In most cases, the sample under test is inserted in a transmission line system and the permittivity is deduced from measurement of the reflection and transmission coefficients using a vector network analyser. These methods are