Fabrication of Low-Stress Dielectric Thin-Film for Microsensor Applications

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***Abstract*— A method of fabricating low-stress dielectric thin film as the supporting material of micromachined devices is reported. The film is processed by post thermal oxidation of silicon-rich nitride (SN) deposited on silicon substrate by LPCVD. Due to the compensation on the nitride by its top oxide, an ultra-low residual less than 10 MPa can be obtained with proper oxidation scheme. Characteristics of the oxidized nitride were analyzed by Auger electron spectroscopy (AES) and ellipsometry. Large floating membranes of 4×4 cm^2 and 400-nm thick can be made by this method with TMAH etching.**

I. Introduction

In the last two decades, researches on silicon-based microstructures have been developed rapidly with very promising results. Among various types of microsensors, dielectric films are often used as the supporting and isolating materials, either membrane or bridge structures [1]. However, the properties of these dielectric films are vital to microsensor performances [2]–[7]. For example, the hydrostatic strength of a micromachined membrane not only depends on the material strengths, but also strongly on the residual stress existed in it [8]. Although a thicker membrane with lower residual stress will have a larger hydrostatic strength, but to mechanical sensors [2], [3], their mechanical sensitivities are inversely proportional to the membrane thickness and the existed residual stress. Also, to thermal-type sensors [3]–[7], thinner structural membranes can reduce the solid thermal conductance and heat capacity of the devices, therefore provide the advantage of improving their thermal performances, such as better thermal sensitivity, higher responsive speed, and less power consumption. All of these indicate thin and low-stress dielectric membranes are very important to microelectromechanical devices.

Traditionally, dielectric films for supporting micromachined devices have been formed either by thermal oxide or by stoichiometric silicon nitride, but these materials generate large thermal stress with their silicon base that often results in device fracture. To improve it, a sandwich structure of oxide/nitride/CVD-oxide (ONO) was developed recently for stress reduction [9]. However, when the standard CMOS process compatibility is considered for integrated device fabrication, this ONO structure could be thicker and more complex by the process. An alternative is to deposit a single layer of silicon-rich nitride (SN) by LPCVD to lower down the residual stress, but a rather large stress still exists [10], [11].

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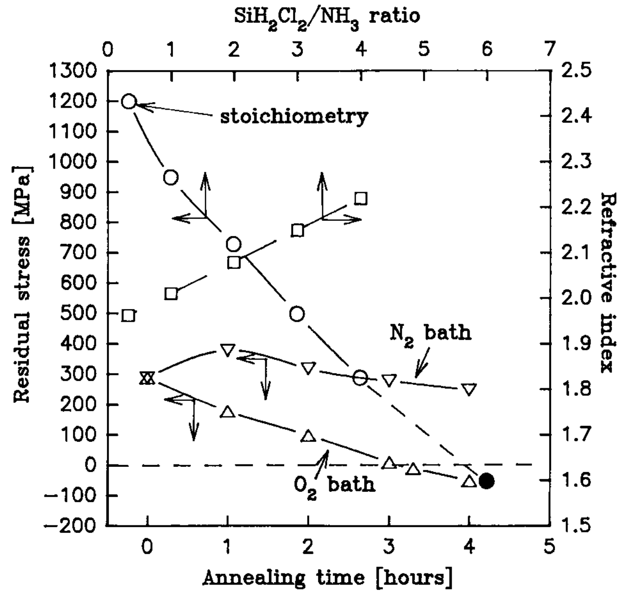


Fig. 1. Dependence of the residual stress (○) and the refractive index (□) on the reacting gas ratio (upper scale); also on the heat treatment time (lower scale) with the samples deposited in a gas ratio of four.

In the following, we describe a new method capable of producing successfully a low-stress dielectric thin film, by further employing a post oxidation step on the above-mentioned LPCVD deposited silicon-rich nitride (OSN).

II. The Experimental

P-type (100) Si wafers of 10–20 $\Omega \cdot$ cm resistivity were used for the experiment. After RCA cleaning, nitride films were deposited by LPCVD with various SiH_2Cl_2/NH_3 ratios at a 850 °C deposition temperature, by keeping SiH_2Cl_2 flow and pressure constant. The thicknesses and refractive indices of the grown films were measured by ellipsometry. The fabricated samples were then divided into two groups: one for observation of the stress change caused by the annealing effect on the film; another for characterization of the oxidation phenomena. The stress on the wafer was measured by optical reflection method using a Tencor FLX-2320 instrument. Film compositions of the processed samples were analyzed quantitatively by Auger electron spectroscopy (AES). Finally, the floating membrane structures were made by back-side etching in TMAH solution (22%) at 80 °C.

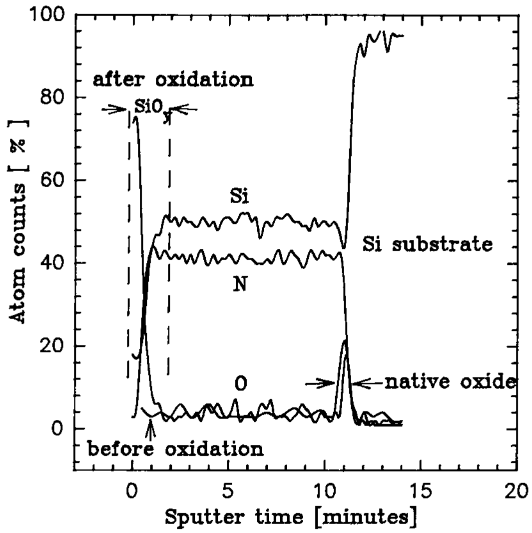


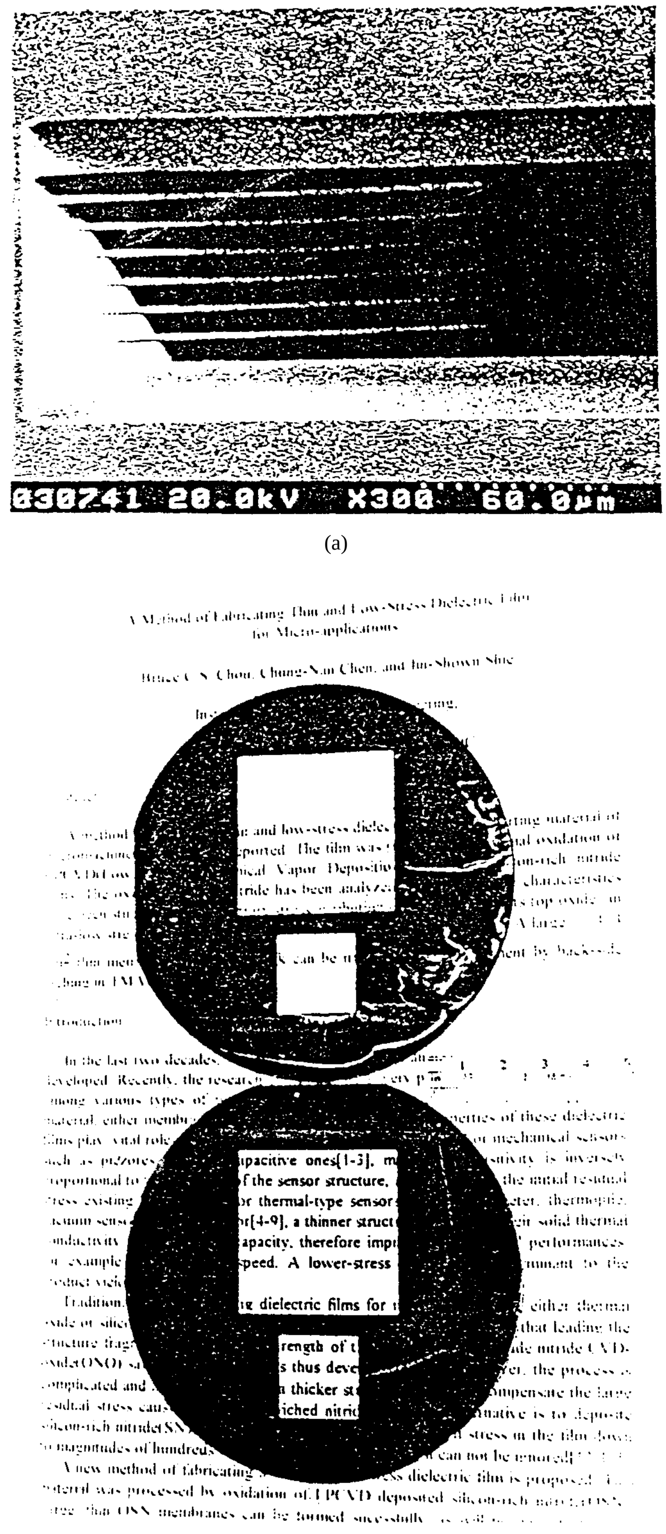
Fig. 2. AES of the nitride films, before and after oxidation.

III. Results and Discussions

In Fig. 1, (◯) represents the measured stresses in SiN films affected by various SiH_2Cl_2/NH_3 ratios. At the ratio of 0.33, the stress is as large as 1.2 GPa which is the reported value of the stoichiometric silicon nitride [11]. One observes that the film stress decreases sharply with increasing SiH_2Cl_2/NH_3 ratio. Sekimoto *et al.* [12] have reported that a ratio of six will lead the film stress to be compressive (●). However, we observed in our experiment that excessive ratio (>4) had caused extreme nonuniformity in the film thickness and refractive index. Incomplete chemical reaction between these two reacting gases might be the reason causing the problem. Fig. 1 also shows the correlation between the refractive index and SiH_2Cl_2/NH_3 ratio, the index (□) increases nearly linearly with the ratio due to the increased content of high-index Si. The correlation between the refractive index and the residual stress implies a quick and easy method to estimate the stress value in these films by ellipsometry. This is especially useful for the on-line test during factory batch production.

Annealing and oxidation of the deposited samples were treated at 1100 °C in nitrogen or oxygen bath. For the sample, in nitrogen bath, the film stress was increased during the initial annealing stage (▽ points in Fig. 1). This was interpreted by Maier-Schneider *et al.* as a result of dehydrogenation effect of the nitride material [13]. After a period of annealing, the viscous flow in the film started to compensate this effect and the stress was reduced. But the reduction was not further valid for even longer annealing. On the contrary, the sample in oxygen bath revealed a notable change of the residual stress (△ points), proving that the post-oxidation method is indeed effective. An ultra-low stress less than 10 MPa can be obtained finally with proper oxidation time, which is 3 h in our case. Minor residual stress, either tensile or compressive, can also be tuned on a SN sample by accurate timing its oxidation. The complex ONO structures that the others [9]–[12] had adopted therefore are unnecessary.

AES was used to study quantitatively the composition of the nitride films, before and after oxidation. The results are shown



(a)

(b)

Fig. 3. Demonstrations of OSN film quality: (a) cantilevers with no obvious deflection; (b) large thin membranes (the upper cracked sample had no oxidation and the lower intact sample was with post-oxidation).

in Fig. 2. Before oxidation, composition of the silicon-rich nitride layer with SiH_2Cl_2/NH_3 ratio of four was calibrated by AES to be $Si_1N_{0.85}$, be referred to the stoichiometric nitride. After 3 h of oxidation, an oxide layer had grown apparently on the surface to serve as the stress-compensation layer to the nitride underneath, which resulted in the low 10 MPa stress.

A SEM picture of micromachined cantilevers of the OSN film is shown in Fig. 3(a) to demonstrate the excellence of this method. These cantilevers show no notable deflection, even they are 160 μm long, 2 μm wide, and only 250 nm thick. This indicates the average residual stress has been sufficiently compensated in the nitride film without inducing the gradient stress [14] by the newly grown oxide. Fig. 3(b) is the picture of two 4×4 cm^2 floating membranes etched by TMAH at 80 °C. The upper SN sample, without post-oxidation, became cracked during the etching, while the lower OSN sample has remained flat and highly optical transparent (with uniform yellow color due to interference).

IV. Conclusion

In conclusion, fabrication of low-stress dielectric thin film has been achieved by post-oxidation of the LPCVD deposited silicon-rich nitride. A proper post-oxidation period will be able to tune the film stress to the lowest value, and intact membranes as large as 4×4 cm^2 with 400 nm thick can be made. Estimation of the residual stress simply by refractive-index measurement is also proposed from the experiment. The process steps of the excellent OSN membrane are fully compatible to the standard CMOS fabrication for the related integrated micromachined devices.

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