A CMOS 15-Bit 125-MS/s Time-Interleaved ADC with Digital Background Calibration

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Abstract—**A 15-bit 125-MS/s two-channel time-interleaved pipelined ADC is fabricated in a 0.18 μm CMOS technology, and achieves 91.9 dB SFDR, 69.9 dB SNDR for a 9.99 MHz input. The ADC uses a single sample-and-hold amplifier which employs a precharging circuit technique to mitigate the performance requirements for its opamp. Digital background calibration is applied to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. Excluding I/O buffers, the chip occupies an area of 4.3 × 4.3 mm^2 and dissipates 909 mW from a 1.8 V supply.**

I. INTRODUCTION

High-resolution high-speed Nyquist-rate analog-to-digital converters (ADCs) have been predominantly realized using the pipeline architecture. High-gain opamps with linear feedback are often used to ensure the linearity of sample-and-hold amplifiers and pipeline stages. To achieve more than 14-bit resolution, the opamps are required to have a voltage gain of more than 90 dB, which results in reduced speed. Thus, there are few published ADCs that can achieve both more than 14-bit resolution and more than 100-MS/s sample rate. The BiCMOS ADC of [1] achieves 75 dB SNR and 100 dB SFDR at 125 MS/s sample rate, but also consumes 1.95 W of power. The BiCMOS ADC of [2] achieves 70.2 dB SNDR and 79.9 dB SFDR at 100 MS/s sample rate by using time-interleaved architecture with foreground digital calibration. It consumes 1.4 W of power. The CMOS ADC of [3] employs digital calibration to mitigate the requirements for the opamps. But it achieves only 70 dB total harmonic distortion (THD) at 100-MS/s sample rate.

The ADC reported in this paper comprises two time-interleaving pipelined A/D channels to achieve an equivalent sample rate of 125 MS/s. A single sample-and-hold amplifier (SHA) is used to avoid the sampling phase error between the two channels. The SHA uses a precharging circuit configuration to mitigate its requirements for the opamp which has to operate at maximum clock rate of 125 MHz. Digital calibration is employed to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. The calibration is proceeded continuously without interrupting the normal A/D operations. The ADC chip was fabricated in a 0.18 μm 1P6M CMOS technology with MIM capacitors, and operates under a single 1.8 V supply.

II. ADC ARCHITECTURE

Fig. 1 shows the block diagram of the time-interleaved ADC presented in this paper. It consists of a single SHA and two identical analog-to-digital conversion (A/D) channels. The use of a single SHA avoids any sampling skew error between the two channels. The offset and gain mismatch between the two A/D channels are corrected in the backend digital domain. The final digital output is obtained by multiplexing the outputs from the two A/D channels.

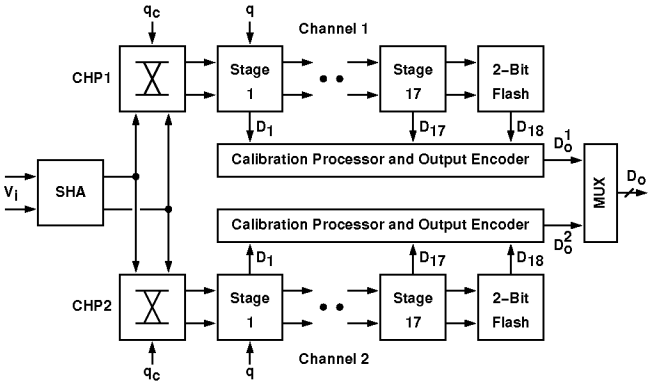

Fig. 1. ADC block diagram.

The two random choppers, CHP1 and CHP2, are placed in front of the two A/D channels respectively. The choppers can multiplex the SHA's outputs to perform time-interleaving operation. They also randomize the polarity of the sampled input seen by the two A/D channels, so that the overall offsets of the A/D channels can be calibrated [4]. The choppers are controlled by a binary-valued random sequence, q_c.

Each A/D channel consists of 17 radix-2 1.5-bit switched-capacitor (SC) pipeline stages and a final 2-bit flash stage. The pipeline employs a correlation-based digital background calibration scheme to achieve high linearity [5]. A q random sequence is injected into the pipeline to facilitate the calibration.

III. SAMPLE-AND-HOLD AMPLIFIER (SHA)

Fig. 2 shows the schematic of a precharged SHA that has been proposed for time-interleaved A/D applications [6]. During the ϕ_3 sample mode (ϕ_3 = 1 and ϕ_1 = 1), the input not only drives the C_{i1} and C_{i2} sampling capacitors but also precharges the SHA's output nodes including the input capacitive loadings of the A/D channel 1, C_{L1} and C_{L2}. During the ϕ_4 sample mode (ϕ_4 = 1 and ϕ_1 = 1), the input capacitive loadings of the A/D channel 2, C_{L3} and C_{L4}, are precharged instead. During both sample mode period, the

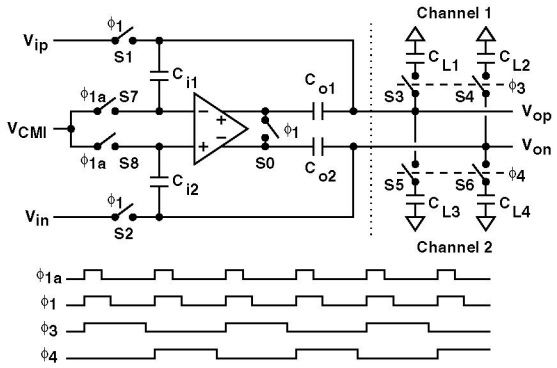

Fig. 2. Precharged sample-and-hold amplifier.

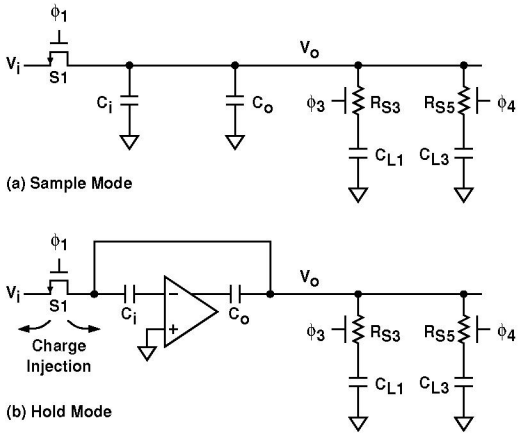

Fig. 3. Simplified SHA operation: (a) sample mode; (b) hold mode.

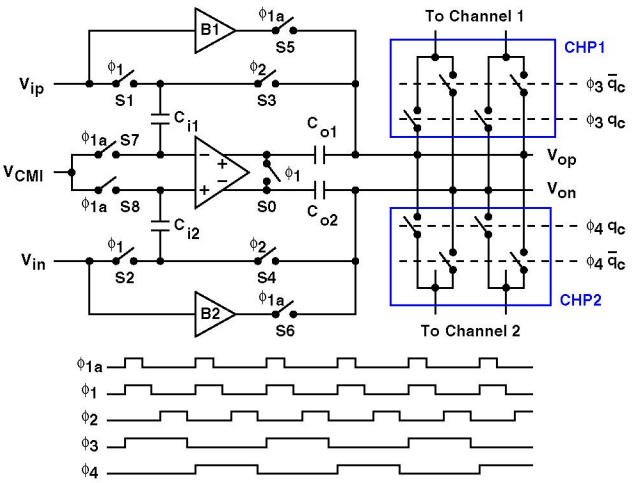

Fig. 4. Modified precharged sample-and-hold amplifier.

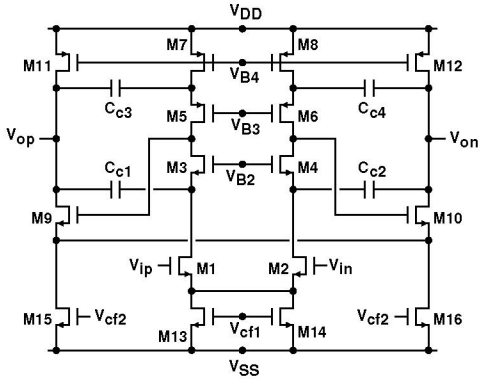

Fig. 5. SHA's operational amplifier.

opamp's outputs are equalized by the S0 switch, thus, the two output coupling capacitors, C_{o1} and C_{o2}, are added. When switching to the hold mode ($\phi_1 = 0$), the opamp's outputs can settle to their final values in a shorter time period without slewing due to the precharging. The combination of output capacitor coupling and precharging also reduces the opamp's dc gain and output voltage swing requirements so that higher speed can be achieved.

However, the linearity of the precharged SHA shown in Fig. 2 can be degraded by the mismatches between the S3-S4 output network and the S5-S6 output network. Fig. 3 shows the SHA's single-ended circuit configuration during the sample mode and the hold mode. The S3 and S5 switches are modeled as two voltage-controlled resistors, R_{S3} and R_{S5}. During the ϕ_3 sample phase, the R_{S3}-C_{L1} network is connected to the V_o node. During the ϕ_4 sample phase, the R_{S5}-C_{L3} network is connected to the V_o node. If there are mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks, the V_i-to-V_o frequency response in the sample node is varied when the SHA alternates between the ϕ_3 and ϕ_4 phases. Furthermore, when the SHA is being switched from the sample mode to the hold mode, charges are injected into the V_o node with the S1 switch being turned off. If there are mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks, the amount of V_o change due to the charge injection in the ϕ_3 phase is different from that in the ϕ_4 phase.

Fig. 4 shows the circuit schematic of the modified precharged SHA used in this ADC design. Two unity-gain buffers, B1 and B2, are added so that the V_i-to-V_o frequency response can remain the same during either the ϕ_3 sample phase or the ϕ_4 sample phase. The charge injection from the S1 and S2 switches can no longer affect the final V_o output in the hold mode. The charge injections from the additional S5 and S6 switches as well as mismatches between the output multiplexer networks have little effect on the final V_o value during the hold mode. Also shown in Fig. 4 are the CHP1 and CHP2 choppers. This SHA samples the input using the ϕ_1 clock with sampling rate at f_s = 125 MS/s. Each chopper consists of 4 analog switches controlled by either ϕ_3 or ϕ_4 clocks with frequency at $f_s/2$. Their outputs are inverted when $q_c = 0$.

Fig. 5 shows the schematic of the opamp used in the SHA. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage. Two separate switched-capacitor common-mode feedback circuits are used to generate control voltage V_{cf1} and V_{cf2} for the first and second stages of the opamp. The

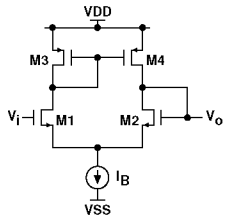

Fig. 6. SHA's unity-gain buffer.

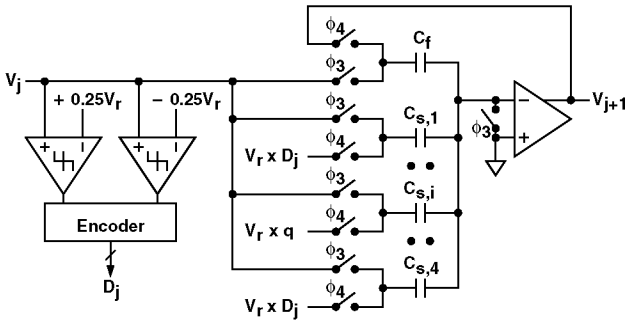

Fig. 7. SC pipelined stage for digital background calibration.

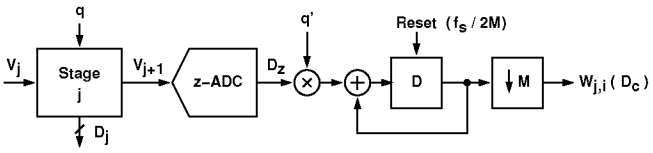

Fig. 8. Background calibration of pipeline stage.

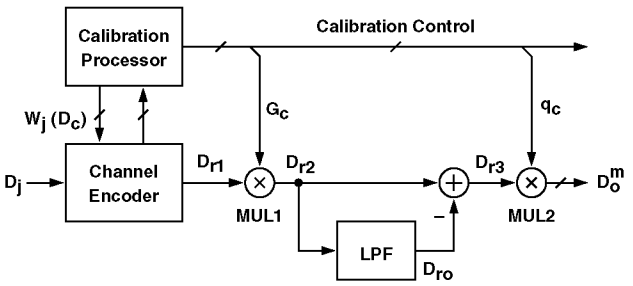

Fig. 9. Digital background calibration scheme.

input common-mode voltage is set to 0.95 V, and the output common-mode voltage is set to 1.15 V. The opamp can provide a differential output voltage range of 1.9 V. The overall dc voltage gain of the opamp is more than 90 dB. The opamp dissipates 100 mW of power and achieves a unity-gain frequency of 1.66 MHz with C_i = 4 pF, C_o = 6 pF, and C_L = 4 pF.

Fig. 6 shows the schematic of the B1 and B2 unity-gain buffers. It is a simple single-stage amplifier with an open-loop dc voltage gain of 32 dB. Each buffer dissipates 13 mW of power while driving a total output capacitive load of 7 pF, and has a unity-gain frequency of 2.3 GHz and a slew rate of 1 V/nsec. The behavior of the buffers can deviate from an ideal one due to the offset and low open-loop voltage gain of the amplifier. This non-ideal buffer behavior is not crucial, but the deviation results in a less accurate precharge operation, and demands an increase in the opamp's voltage gain to maintain the SHA's accuracy.

IV. Calibration and Digital Encoding

The digital background calibration described in [5] is used to ensure the conversion linearity of each A/D channel. To facilitate background calibration, the first six pipeline stages employ the circuit schematic shown in Fig. 7. The capacitor C_s is equally split into 4 fragments, $C_{s,1}$ to $C_{s,4}$. For an ideal radix-2 pipeline stage, $C_f = C_s = \sum_{i=1}^{4} C_{s,i}$ During the sample phase (ϕ_3 = 1), the V_j stage input is stored in C_s and C_f capacitors and is also compared with the $\pm 0.25V_r$ references to generate a D_j stage digital code, where $D_j \in \{-1, 0, +1\}$. During the hold phase (ϕ_4 = 1), all the C_s capacitors are connected to $D_j \times V_r$ except the $C_{s,i}$ capacitor which is connected to $q \times V_r$. The q random sequence alternates between +1 and 0 or between −1 and 0. By injecting a random sequence into the pipeline stage, it is possible to calibrate a pipeline stage without interrupting its normal A/D operation.

Fig. 8 shows the scheme of digital background calibration. The V_{j+1} output of the j-th pipeline stage is digitized by a backend z-ADC with a corresponding D_z digital output. The z-ADC comprises of the $(j + 1)$-th, $(j + 2)$-th, ..., pipeline stages. The D_z signal is correlated with a q' random sequence and then integrated on an accumulator. The q' signal has the same waveform pattern as the q sequence but alternates between +1 and −1. The resulting output $W_{j,i}(D_c)$ is taken only after M cycles of integration, where M is the period of the q random sequence. In one M period, the q' sequence needs to have equal number of +1 and −1. The $W_{j,i}(D_c)$ represents the magnitude of the q random sequence seen by the z-ADC, where D_c is either +1 or −1 depending on the polarity of the q sequence. The final calibration data, $W_j(D_c)$ where $D_c \in \{-1, 0, +1\}$, are assembled by letting $W_j(D_c) = \sum_{i=1}^{4} W_{j,i}(D_c)$ and $W_j(0) = 0$.

Assume there are P pipeline stages in each A/D channel, and only the first K stage are subjected to calibration. For $j > K$, we can choose $W_j(D_c) = D_c$. Calibration is preceded backward and sequentially while the ADC performing normal A/D conversion. First, the K-th stage is calibrated using the backend stages, from $(K+1)$ to P, as the z-ADC to extract the $W_K(D_c)$ data. Then, the $(K - 1)$-th stage is calibrated using the backend stages, from K to P, as the z-ADC to extracted the $W_{K-1}(D_c)$ data. The procedure continues toward the first stage to complete one calibration cycle.

Fig. 9 shows the block diagram for output encoding and correction in each A/D channel. The channel encoder calculates the raw A/D output, D_{r1}, from pipeline stage's digital outputs, D_j for all j, by applying

$$D_{r1} = \sum_{j=1}^{P} \frac{W_j(D_j)}{2^j} \tag{1}$$

The D_{r1} stream is free of nonlinearities caused by the gain

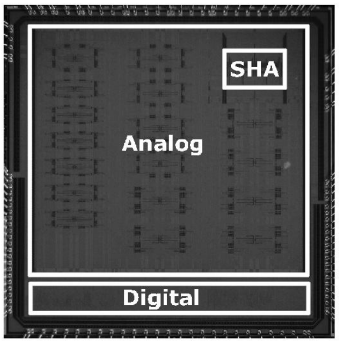

Fig. 10. Die micrograph of the prototyping ADC.

errors of the pipeline stages. To equalize the conversion gains of the two A/D channels, the MUL1 multiplier multiplies the D_{r1} with a G_c gain correction factor, and generates the D_{r2} stream. The calibration processor shown in Fig. 9 calculates the G_c factor from the acquired calibration data by using

$$G_c = \frac{2 \times \sum_{j=1}^{P} \frac{1}{2^j}}{\sum_{j=1}^{P} \frac{W_j(+1)}{2^j} - \sum_{j=1}^{P} \frac{W_j(-1)}{2^j}} \quad (2)$$

The overall dc offset of the A/D channel, D_{ro}, is extracted from the D_{r2} stream by a low-pass filter (LPF) [4]. The D_{r3} stream is the D_{r2} stream with its dc offset removed. Finally, the single channel output, D_o^m where $m \in \{1, 2\}$, is obtained by unscrambling the D_{r3} stream with the q_c sequence.

V. EXPERIMENTAL RESULTS

Fig. 10 shows the ADC's chip micrograph. Chip core area is 4.3 × 4.3 mm^2. Digital circuits occupy 11% of the total area. Operating at 125 MS/s sampling rate under a single 1.8 V supply, the analog block consumes a total of 891 mW of power, while the digital block consumes only 18 mW. In this design, the first six pipeline stages of both A/D channels are implemented with identical capacitors and opamps. The nominal values of the capacitors are C_f = 2 pF and C_s = 2 pF. The opamps are similar to the one shown in Fig. 5, and each consume 47 mW of power. The opamps and capacitors are reduced by half in the next five stages. Another scaling by half is applied to the remaining stages. This ADC prototype was not optimized for low power consumption.

Fig. 11 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC operating at 125 MS/s sample rate with 1.99 MHz sinusoidal input. Digital output codes from a single channel are collected to calculate the DNL and INL. Note that the LSB in Fig. 11 is normalized to 16-bit resolution. The number of registered output codes is approximately $(3/4) \times 2^{16}$. Before activating the calibration processor, the native DNL is +1.16/−0.61 LSB and the INL is +29.8/−29.7 LSB. After the background calibration is activated. The DNL is reduced to +0.25/ − 0.27 LSB and the INL is reduced to +5.5/−5.7 LSB.

Fig. 12 shows the ADC's measured signal-to-distortion-plus-noise (SNDR) and spurious-free dynamic range (SFDR)

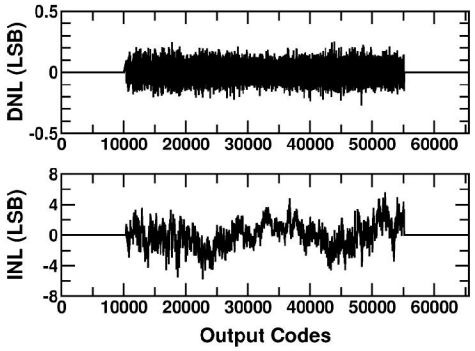

Fig. 11. Measured DNL and INL.

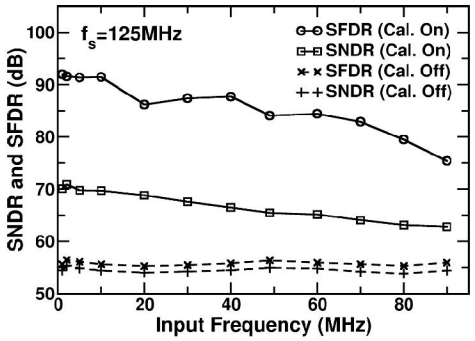

Fig. 12. Measured SNDR and SFDR versus input frequencies.

versus input frequencies at 125 MS/s sampling rate. The calibration can improve the SNDR by more than 10 dB and the SFDR about 30 dB when the input frequencies up to the Nyquist frequency.

ACKNOWLEDGEMENTS

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