# A Unified Behavior Model of Low Noise Amplifier for System-Level Simulation

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***Abstract*— This paper presents a unified RF behavior model that simultaneously predicts the effects of noise, nonlinearity, impedance matching and frequency response and that enables efficient and accurate system simulation. The proposed modeling approach allows characterizing the RF effects incrementally to reduce iteration. A Verilog-A behavior model for an ultra-wideband CMOS low noise amplifier is developed for fast and accurate system simulation. The system simulation results show that the behavior model agrees well with the transistor-level circuit with RMS error less than 0.79%. Ultimately, 87% reduction of simulation time is achieved.**

***Index Terms*— RF behavior model, low noise amplifier.**

## I. Introduction

Performance verification of wireless SOCs integrating digital and analog/RF circuitry prior to chip implementation is crucial and urgent in tight time-to-market schedule. Behavior models based on standard description language empower coverification of both digital and analog/RF subsystems. To improve verification efficiency, RF behavior models with accurate prediction are indispensable. Several behavior models were introduced to describe the RF effects: linear transfer functions represent frequency dependence [1], s-parameter data in Touchstone format characterize impedance mismatch and frequency response for linear small-signal amplifiers, and black box models in Volterra series can model nonlinear distortion [2]. Nevertheless, these models describe RF characteristics individually without considering the impact of each other and are insufficient for system simulation. Besides, the top-down design methodology is preferred to refine the specifications of the RF module circuits at the beginning stage for developing sophisticated wireless systems. The table-based or polynomial models can not support top-down design methodology due to the lack of circuit insights in these models.

This paper proposes a Verilog-A RF behavior model that simultaneously predicts the effects of noise, nonlinearity, impedance mismatch and frequency response and that enables efficient and accurate system simulation. Our unified model and modeling approach also allow top-down design. A model for a CMOS LNA was developed and agrees well with the transistor-level circuits in both RF and system performance simulation. By means of the proposed model, the system performance can be evaluated efficiently prior to full chip implementation.

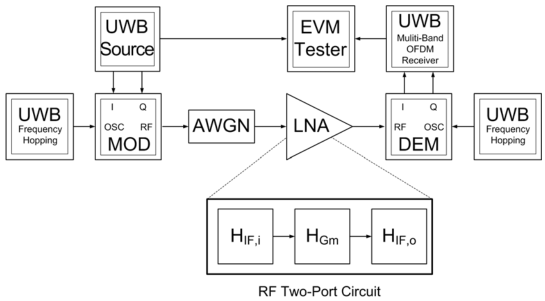


Fig. 1. UWB system simulation block diagram

## II. Unified Behavioral Model for RF Circuits

Here, we focus on the RF building blocks of two-port network, such as amplifiers and filters. Mixers and switches are, on the other hand, beyond the scope of this paper. As shown in Fig. 1, the proposed behavior model consists of three modules: input interface module ($H_{IF,i}$) for the input impedance network, core module ($H_{G_m}$) for the gain stage, and output interface module ($H_{IF,o}$) for the output load impedance. In a LTI system, the transfer function of the two-port network is represented by $H_{IF,i} \cdot H_{G_m} \cdot H_{IF,o}$ in the system simulation platform. Detailed modeling approach for each module is described in the following sections.

### *A. Modeling of Input and Output Interfaces*

The input/output impedance networks of a two-port circuit shape its frequency response and bandwidth. Though Laplace transfer function can be used to model the frequency response [3], it only defines the voltage/current transfer relation and requires additional impedance networks for the loading effect. The additional impedance networks nevertheless also shape the overall frequency response and introduce iterations in modeling. Instead of using Laplace transfer function, the proposed model employs equivalent impedance networks to portray the frequency response and the impedance matching properties of input/output interfaces at the same time.

An equivalent circuit consisting of resistors, inductors, and capacitors is established to model the input matching network and the input impedance of the active device. The capacitors and inductors are used to define the reactance of $H_{IF,i}$, while the resistors to define the loss including the resistor loss as well as the inductor loss and the capacitor loss. Physically,

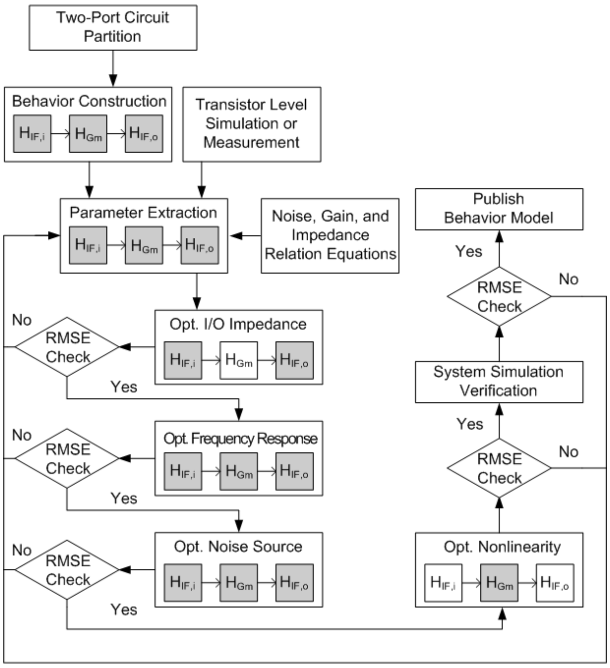


Fig. 2. Unified behavioral modeling flow

regular resistors contribute not only loss but also thermal noise. However, the equivalent resistors in $H_{IF,i}$ are not the actual thermal noise sources, and are intended to model the loss only. Similarly, the load impedance and the output impedance of the active device are modeled as a network of noiseless resistors, inductors, and capacitors.

## *B. Modeling of Gain Stage*

The gain stage can be simply modeled by a controlled signal source, depending on the input and output signal types of the active devices. For example, voltage-controlled current sources (VCCS) and current-controlled current sources (CCCS) are used for common-source and common-emitter amplifiers, respectively. Since the impedance of the controlled signal sources have been considered in the interface modules, the controlled signal source in $H_{G_m}$ is ideal and defines the input and output voltage/current relation either linear or nonlinear.

## *C. Modeling of Noise*

The noise effects are lumped into an equivalent noise source instead of a noisy resistor as [3]. Hence the RF effects are modeled incrementally with iteration reduced. The noise effects of a two-port network are modeled by three equivalent noise sources $i_{n,IF,i}$, $i_{n,G_m}$ and $i_{n,IF,o}$ for the input interface, core and output interface modules, respectively. For easy extraction of noise and model consistency, $i_{n,IF,i}$, $i_{n,G_m}$ and $i_{n,IF,o}$ are all placed at the output node of each module. The explicit input noise source of the active device, for example, is absorbed to $i_{n,IF,i}$ in the preceding module.

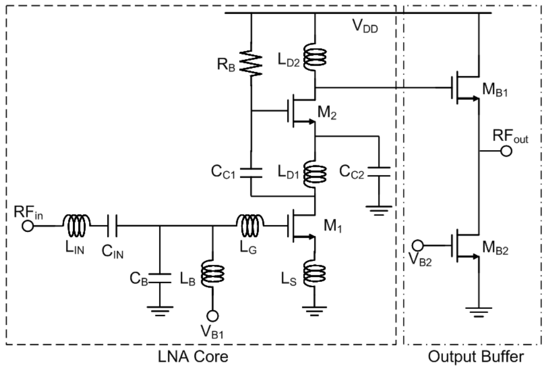


Fig. 3. The target UWB LNA circuit

## *D. Modeling Flow*

A modeling flow is developed for the proposed unified RF behavior model as depicted in Fig. 2. The two-port circuit is mapped into three behavior modules as mentioned above with RF characteristics relation equations in each module derived. This is a process of abstracting the physical circuit topology into a simplified equivalent circuit and grouping the equivalent circuit elements into each module accordingly, which has a great influence on the iterations in later optimization processes. From the results of the transistor-level simulation or measurement, the initial values for the model parameters in $H_{IF,i}$, $H_{G_m}$ and $H_{IF,o}$ are extracted. The parameter extraction is followed by four optimization processes to fit the model parameters for RF characteristics of input and output impedance, frequency response, noise and nonlinear effects in sequence. The optimization is a complex task due to the correlation among the RF characteristics, and therefore proceeded incrementally by considering the noise and nonlinear effects. That is, for small input signal condition, the two-port circuit is regarded as a noiseless linear circuit in the first two optimization procedures and then a noisy linear circuit in the noise optimization. On the other hand, the circuit is considered as a noisy weak-nonlinear network in the final optimization procedure. For reverse isolation concern, more iteration is required in the non-unilateral cases. The optimal model parameters are obtained if the root mean square error (RMSE) is smaller than a threshold value. Ultimately, a system simulation should be performed to verify the fidelity and feasibility of the RF behavior model.

# III. MODELING EXAMPLE OF AN UWB LNA

In this section, a behavior modeling example of a CMOS LNA for ultra-wideband wireless applications is presented according to the above modeling procedure.

## *A. Construction of Equivalent Behavior Model*

The targeting UWB LNA was fabricated in 0.18-$\mu$m CMOS technology and the circuit schematic is illustrated in Fig. 3. The LNA employs stagger tuning technique, which consists of two stacked common-source stages with different resonance frequencies [4]. The output buffer in Fig. 3 is for measurement

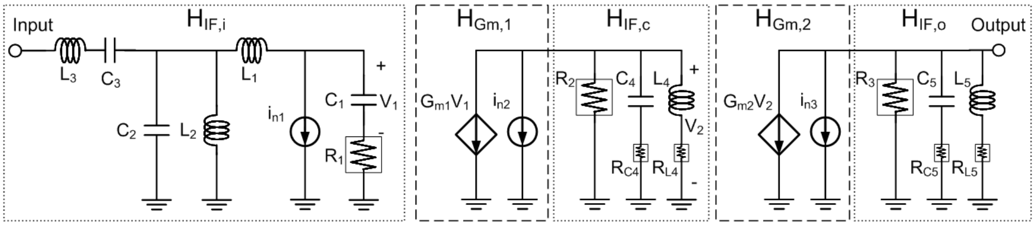


Fig. 4. The UWB LNA Model

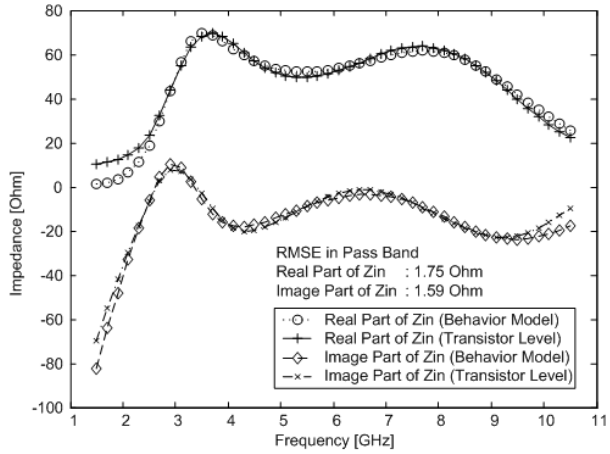


Fig. 5. Comparison of input impedance.

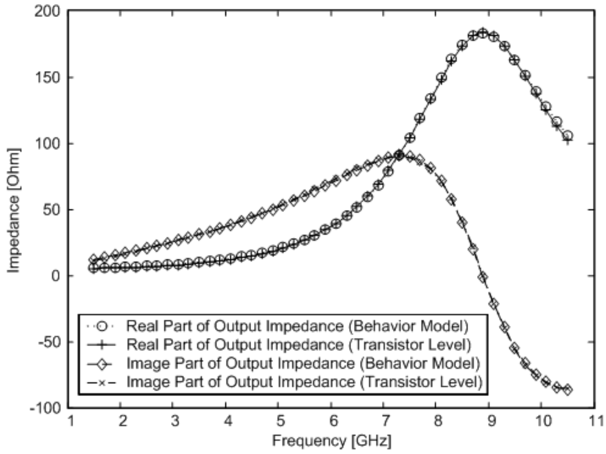


Fig. 6. Comparison of output impedance.

purpose only and omitted in the behavior model. The behavior model of the UWB LNA contains three interface modules, $H_{IF,i}$, $H_{IF,c}$ and $H_{IF,o}$, and two $G_m$-core modules, $H_{G_m,1}$ and $H_{G_m,2}$, mapping the two amplification stages as shown in Fig. 4.

### B. I/O Interface

A simple RLC parallel network can be used to model the interface modules for narrow band circuits. To model the input band-pass matching network and the input impedance of transistor $M_1$ of the UWB LNA, ideal lump elements $L_1, L_2, L_3, C_1, C_2, C_3$ and $R_1$ are used in $H_{IF,i}$. $H_{IF,c}$ and $H_{IF,o}$ add $R_{C4}$, $R_{L4}$, $R_{C5}$, and $R_{L5}$ in the RLC parallel network due to the low-$Q$ loads of the wide-band amplifier. It should be noted again that all resistors framed in Fig. 4 are noiseless.

### C. $G_m$ Core

In an $N$-stage amplifier, $N$ numbers of $G_m$-core modules are exploited regardless its topology. The partition of the RF behavior model is determined by the critical impedance components which contribute the poles or zeros in the frequency response of the RF circuits. Two $G_m$ cores $G_{m,1}$ and $G_{m,2}$, as a consequence, exist in the behavior model and their initial values are extracted from the small-signal transconductance values of transistors $M_1$ and $M_2$. Combining $H_{G_m,1}$ and $H_{G_m,2}$ with $H_{IF,i}$, $H_{IF,c}$, and $H_{IF,o}$, the frequency response is optimized to portray the noiseless linear characteristic of the UWB LNA.

### D. Noise Sources

The noise sources considered in the RF behavior model are only thermal noise contributed by the resistors and transistors of the RF amplifier while the flicker noise of MOSFET devices is not critical. The thermal noise of a MOSFET device includes gate noise and drain current noise [5]. For calculation simplicity, the drain current noise source stays in the $G_m$-core module and the gate noise source is, on the contrary, placed in the preceding interface module. The noise of $H_{IF,c}$ and $H_{IF,o}$ is also merged into the preceding $G_m$-core modules. Consequently, three noise sources $i_{n1}$, $i_{n2}$ and $i_{n3}$ are adopted to describe the noise performance.

### E. Nonlinearity

The UWB LNA is assumed weakly nonlinear and then modeled with Taylor series for its transfer function [6]. In addition, the nonlinear effect is dominated in the second stage of the UWB LNA. Therefore, the nonlinearity is simply related to the third order coefficient ($\alpha_3$) of Taylor series in $H_{G_m,2}$ and its initial value is set to be $\alpha_3 = \frac{4}{3}\frac{A_v}{A_{IIP3}^2}$.

## IV. Comparison of Transistor-Level Circuit and Behavior Model

The simulation results of input/output impedance, noise figure, voltage gain, input 1-dB compression point and IP3 of the RF behavior model agree well with those of the transistor-level UWB LNA as shown in Fig. 5–9.

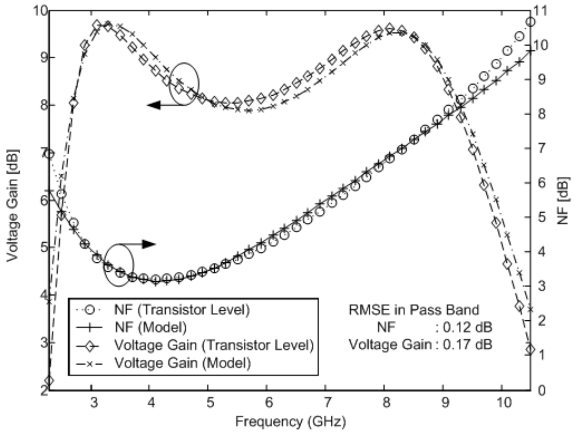


Fig. 7. Comparison of voltage gain and $NF$.

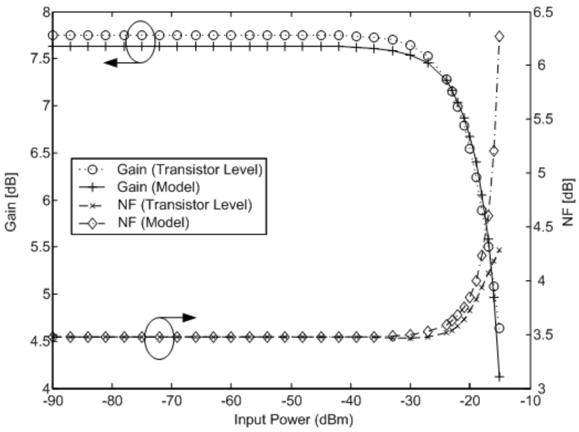


Fig. 8. Comparison of NF and power gain with sweeping RF power.

Error vector magnitude (EVM) simulation based on multi-band OFDM UWB design library in Agilent ADS platform is performed to validate the unified RF behavior model. With the circuit envelope simulator, the platform allows co-simulating of baseband algorithms and RF Verilog-A models. The input signal is 480-Mbps OFDM modulated at 5.016 GHz with power level sweeping from −72.8 to −27.8 dBm. The simulation results shown in Fig. 10 agree well with those of the transistor-level LNA with EVM RMS error less than 0.79% and the simulation time for all power sweeps is reduced 87%. The simulation results verifies the accuracy of the unified RF behavior model and demonstrates great efficiency.

## V. Conclusion

An RF behavior model has been presented to predict RF effects of noise, impedance mismatch, frequency response, and nonlinear distortion of two-port RF circuits for system simulation. The proposed modeling approach allows modeling the RF effects incrementally with iteration reduced. The accuracy of the model is verified with both RF simulations and system EVM simulation. The model provides convincing prediction capability and great efficiency in system simulation compared with transistor-level circuit.

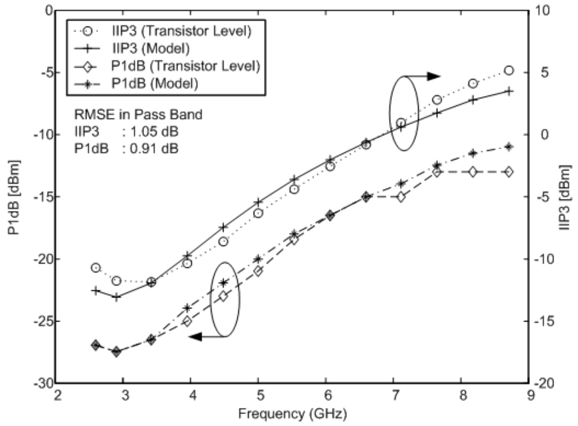


Fig. 9. Comparison of input IP3 and 1-dB compression point in the frequency band of interest.

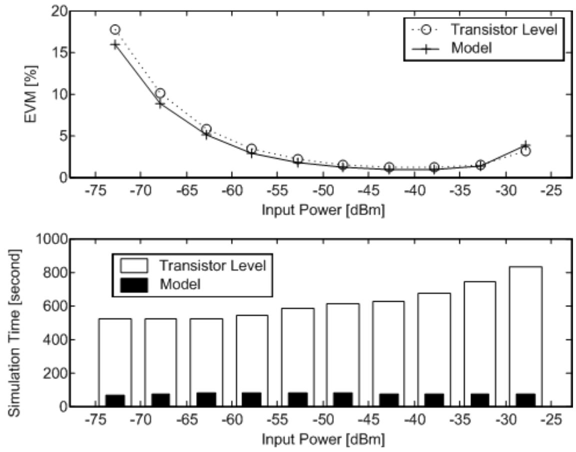


Fig. 10. Comparison of UWB system EVM simulation results.


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