Process-Variation- and Random-Dopant-Induced Static Noise Margin Fluctuation in Nanoscale CMOS and FinFET SRAM Cells

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Abstract

In this study, a three-dimensional "atomistic" coupled device-circuit simulation approach is advanced to investigate the process-variation-effect (PVE) and random dopant fluctuation (RDF) induced characteristic fluctuations in planar metal-oxide-semiconductor field-effect-transistor (MOSFET) static random access memory (SRAM) from 65-nm to 16-nm gate length. Our preliminary results show that the RDF dominates the fluctuation of static noise margin (SNM). As the gate length of the planar MOSFETs scales from 65 nm to 16 nm, the normalized RDF-induced SNM fluctuation increases from 4% to 80%. To reduce the device variability induced fluctuation in circuit, a device with vertical-doping-profile and raised V_{th} is employed. The SNM is 3 times larger than the original 16-nm-gate SRAM. Moreover, the normalized RDF-induced SNM fluctuation is reduced by a factor of 2.67. Additionally, a 16-nm-gate silicon-on-insulator fin-type field-effect-transistor is used to further improve the SNM of SRAM. Due to the superior electrostatic integrity and larger effective device width than planar MOSFETs, the SNM of 16-nm-gate FinFET SRAM is six times larger than the original 16 nm SRAM with five times smaller SNM fluctuation. The study investigates the roll-off characteristics of SNM and provides an insight into design of fluctuation resistant nanoscale SRAM.

1. Introduction

As the dimension of complementary metal-oxide-semiconductor (CMOS) devices shrunk into sub-65nm scale, the threshold voltage (V_{th}) fluctuation is pronounced and become crucial for the design window, yield, noise margin, stability, and reliability of ultra large-scale integration circuits [1-4]. Various randomness effects resulting from the random nature of manufacturing process have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) devices and circuits. The fluctuation of short channel effect includes process-variation-induced gate length deviation and line edge roughness (PVE) are growing worse due to serious short-channel effect when the dimension of device is further scaled [5]. Besides the process variation induced threshold voltage fluctuation ($\sigma V_{th,PVE}$), the double-digit channel dopants in scaled channel size make transistor behaviors more complicated to be characterized with conventional "continuum modeling" because every "discrete" dopant has its significant weight impacting the resulting transistor performance. The random nature of discrete dopant distribution results in significantly random fluctuations, such as the fluctuation of threshold voltage ($\sigma V_{th,RDF}$). The random dopant fluctuation (RDF) is unpredictable and caused by random uncertainties in the fabrication process such as microscopic fluctuations in the number and location of dopant atoms in the channel region [4-7] and therefore is hard to be characterized. Static random access memory (SRAM) scaling is a major driver in microprocessor development. However, the intrinsic parameter fluctuations limit the performance and functionality of SRAM due to the significant component mismatch in circuits. The stability of a SRAM cell is often related to the static noise margin (SNM) in the read operation [3], defined as the maximum DC noise voltage tolerance to avoid the cell state been flipped. Various approaches have been proposed to investigate the process-variation effect [5] and random dopant fluctuation [4-7], and the influence upon SRAM performance [1, 2]. However, the dependence of SNM and its fluctuation on transistor's gate length is not clear yet. Thus, this study employed a experimental validated three-dimensional "atomistic" coupled device-circuit simulation approach [4] investigate the process-variation and random dopant induced characteristic fluctuations in planar MOSFET SRAM from 65-nm- to 16-nm-gate length. Two approaches are proposed to reduce the device variability induced fluctuation of SRAM circuit. The first one is to raise the V_{th} of device and use the vertical-doping-profile to suppress the SNM fluctuation. Then a silicon-on-insulator (SOI) fin-type field-effect-transistor (FinFET) is used to replace the conventional MOSFET structure. The proposed approaches are then compared with 16 nm planar SRAM to show its promising characteristics.

2. Simulation Methodology

The nominal channel doping concentrations are $1.48\text{x}10^{18}$ cm^{-3} and the V_{th} are calibrated for 16 nm gate MOSFETs. For RDF, to consider the random fluctuation effect of the number and location of discrete channel dopants, 758 dopants are randomly generated in a large cube ($80 \times 80 \times 80$ nm^3), in which the equivalent doping concentration is $1.48\text{x}10^{18}$ cm^{-3}, as shown in Fig. 1(a). The large cube is then partitioned into 125 sub-cubes of ($16 \times 16 \times 16$ nm^3). The number of dopants may vary from zero to 14, and the average number is 6, as shown in Figs. 1(b) and 1(c), respectively. Similarly, we can obtain the distribution of dopant number for the 32- and 65-nm-gate transistors, in which the dopant number may vary from 10 to 40 and 70 to 130 as shown in Fig. 1(d). These sub-cubes are device simulation is performed by solving a set of 3D density-gradient equations coupling with Poisson equation as well as electron-hole current continuity equations [8, 9]. Figure 1(f) shows the studied SOI FinFET with aspect ratio equal to two. Without losing generality, the SOI FinFET

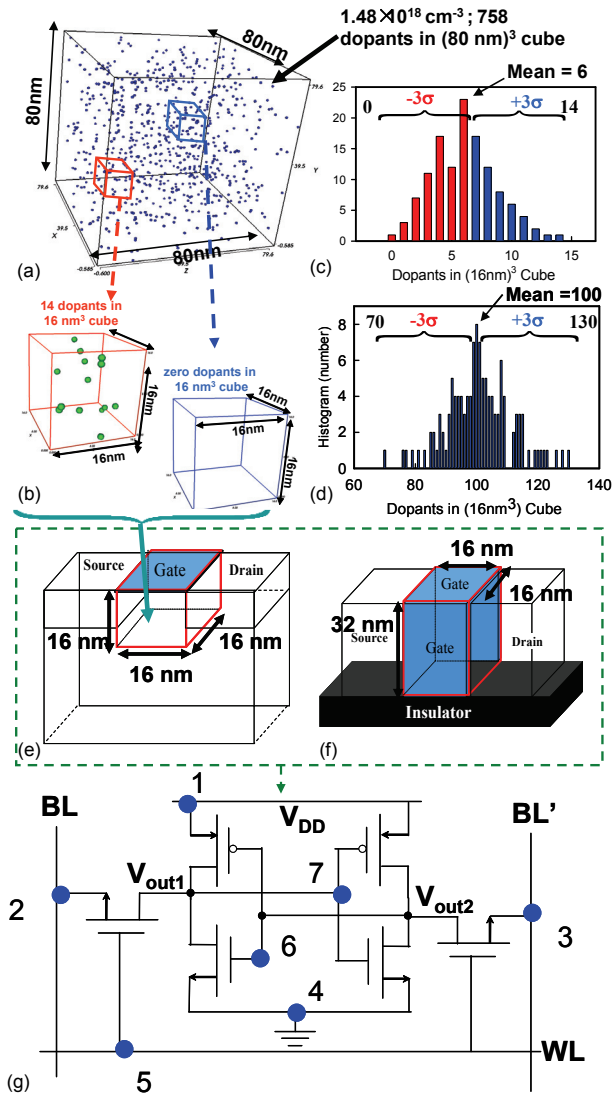

Figure 1: (a) Discrete dopants randomly distributed in the large cube with the average concentration of 1.48 x 10^{18} cm^{-3}. For 16 nm gate devices, 758 dopants are within the cube. The large cube is then partitioned into sub cubes of $(16\ nm)^3$, in which dopants varies from 0 to 14 (average:6) [(b),(c)]. For 65 nm gate devices, dopants varies from 70 to 130 (average: 100) (d). The sub-cubes are equivalently mapped into device channel region [(e),(f)] for "atomistic" device and coupled device-circuit simulation (g).

is with 16-nm-gate and 1.48 x 10^{18} cm^{-3} equivalent channel doping concentration. The explored SRAM circuit is illustrated in Fig. 1(g). The voltage level of BL, BL', WL and V_{DD} will be charged to applied voltage to gather the static transfer characteristics, where the applied voltages of 16 nm and 32nm devices are both 1.0 Volt, and 1.2 Volt of 65 nm devices. The physical model and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [4, 5]. Similarly, we can generate 125 discrete-dopant-fluctuated cases for PMOSFET through the flow of Figs. 1(a)-1(d). Then, 125 pairs of NMOSFETs and PMOSFETs are randomly selected and are used for the examination of circuit characteristics fluctuations. Furthermore, we apply the statistical approach to evaluate the effect of PVE, in which the magnitude of the gate length deviation and the line edge roughness follows the projections of the ITRS 2007 [10]. The 3σ for process variation induced gate length deviation and line edge roughness are 1.5 nm, 3.0 nm and 4.3 nm for the 16 nm, 32 nm and 65 nm devices, respectively. Since no well-established compact model of ultrasmall nanoscale devices is available, to capture the transient characteristic of circuit, a coupled device-circuit simulation approach [4] is employed. The characteristics of devices of test circuit are first estimated by solving the device transport equations and using as initial guesses in the coupled device-circuit simulation. The circuit nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics [4]. Notably, the accuracy of the simulation has been confirmed by using the experimentally calibrated transistor physical model [5].

3. Results and Discussion

Figures 2(a) and 2(b) show the RDF and PVE induced threshold voltage (V_{th}) fluctuations for the 16 nm to 65 nm gate n-type planar MOSFETs, respectively. The nominal value of threshold voltage is rolled-off as the gate length decreased, where the nominal V_{th} for 16, 32, and 65 nm devices are 140, 220, and 280 mV. Based upon the independency of the fluctuation components, the total V_{th} fluctuation ($\sigma V_{th,total}$) is given by:

$$(\sigma V_{th,total})^2 = (\sigma V_{th,RDF})^2 + (\sigma V_{th,PVE})^2, \quad (1)$$

where $\sigma V_{th,RDF}$ and $\sigma V_{th,PVE}$ are RDF and PVE induced threshold voltage fluctuations, respectively. As the gate length scales from 65 nm to 16 nm, the V_{th} fluctuation increases significantly from 16 mV to 64 mV. The RDF induces 15.8 mV, 30 mV and 61 mV V_{th} fluctuations are in 65 nm, 32 nm and 16 nm devices, respectively. The V_{th} fluctuation of 16 nm MOSFET is 4 times larger than that of 65 nm, which follows the trend of analytical shown in below[7].

$$\sigma V_{th,RDF} = 3.19\times10^{-8}\frac{t_{ox}N_A^{0.401}}{\sqrt{WL}}\ [\mathrm{V}], \quad (2)$$

where t_{ox} is the thickness of gate oxide; W and L are the width and length of the transistor. Additionally, as shown in Fig. 2, the RDF dominates the total V_{th} fluctuation in the explored device dimensions. The RDF induces 5 and 3.5 times larger V_{th} fluctuation than PVE for 65- and 16-nm-gate device, respectively. The increasing fluctuations of such extreme small components may cause critical issue of stability. Figure 3 shows the static transfer characteristics of 65 nm planar SRAM cells include process variation effect and random dopant fluctuation. The dashed lines represent the cases with PVE and RDF fluctuation; the solid line stands for the nominal case with continuous channel doping profile of 1.48x10^{18} cm^{-3}. The nominal SNM for the 65 nm planar MOSFET SRAM is 138 mV. The RDF and PVE induce

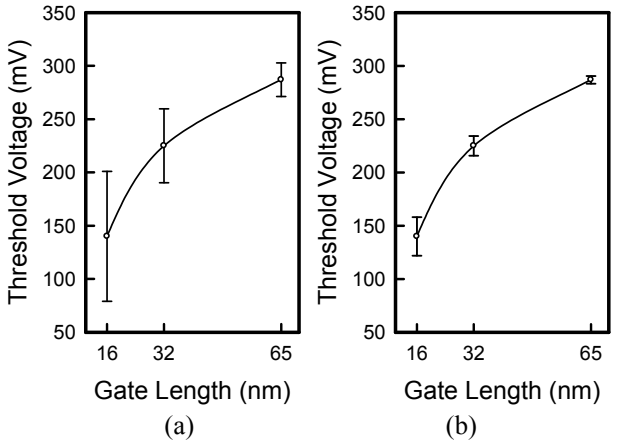

Figure 2: V_{th} fluctuation induced by (a) RDF and (b) PVE for different gate lengths of n-type planar MOSFETs.

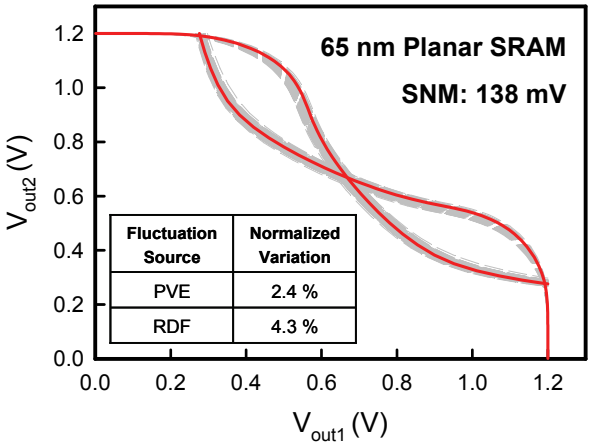

Figure 3: Nominal and fluctuated static transfer characteristics of 65 nm planar SRAM cells.

2.38% and 4.3% normalized SNM fluctuation, respectively. Since the random dopant fluctuation induces larger device variability in threshold voltage, the SNM fluctuation of SRAM is dominated by random doping fluctuation. Similarly, we can obtain the RDF and PVE induced SNM fluctuation for the 16 and 32 nm planar SRAM, as shown in Figs. 4(a) and 4(b), respectively. As gate length scales from 65 nm to 16 nm, the SNM decreases significantly from 138 mV to 20 mV. Moreover, the RDF dominates the SNM fluctuation. Figure 5 summaries the normalized SNM fluctuations. The SNM fluctuation induced by RDF is two to four times larger than the PVE induced fluctuation in different gate sizes. For 16nm SRAM, the RDF and PVE induce as much as 80% and 30%, which is much higher than that in 32 and 65 nm technologies. The result shows that the fluctuation of SRAM is highly dependents on the gate size of transistors. Moreover, the RDF becomes more significant in scaled SRAM circuits. The small SNM of scaled SRAM may cause the malfunction of SRAM. The shrinking of the device size can increase the density of memory; however, the decreased SNM and increased SNM fluctuation are crucial issues and may limit the usage of such small device.

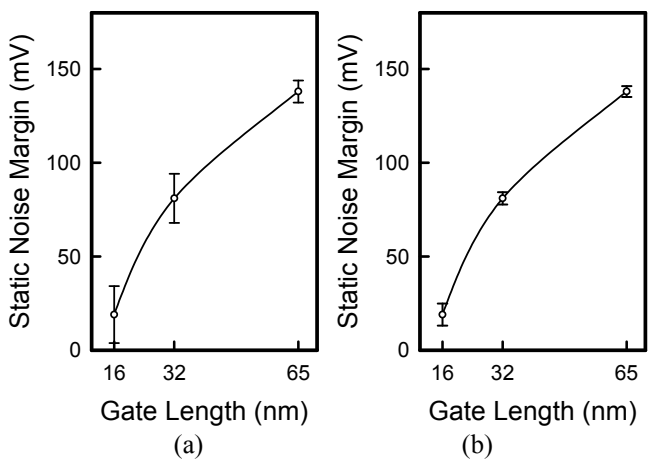

Figure 4: Static noise margin fluctuations induced by (a) RDF and (b) PVE for different gate lengths of SRAM cells.

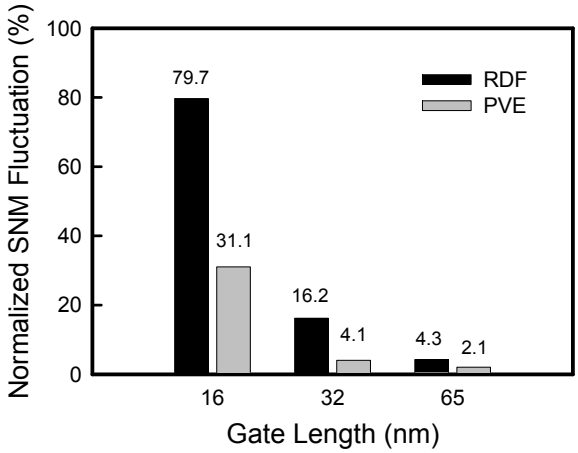

Figure 5: Normalized PVE and RDF induced SNM variation for 16 nm to 65 nm planar SRAM.

There have been several approaches to increase the SNM, such as the use of larger V_{DD} and cell ratio or increase the V_{th} of transistors. This study examined two approaches to reduce the device variability induced fluctuation of SRAM circuit. The first one is to raise the V_{th} of device and use the vertical-doping-profile to suppress the SNM fluctuation. The other is to use SOI FinFETs to replace the conventional MOSFET structure. Figure 6 shows static transfer characteristics of the first approach. The V_{th} of transistor is raised to 350 mV to enlarge the SNM and a vertical doping profile engineering, as shown in the inset of Fig. 6, is been implemented to reduce the discrete dopant induced fluctuations. As in the original doping profile, the numbers of channel dopants in vertical doping profile engineering vary from zero to 14; the average in each case is six. The doping profile from the device surface to the substrate follows a normal distribution. The aim of vertical doping profile engineering is to locate fewer dopants near the current conducting path to suppress the device characteristic fluctuations. With the high V_{th} and vertical doping profile engineering, the SNM of the investigated SRAM cell is increased from 20 mV to 71mV and normalized random dopant induced fluctuations is decreased from 80% to 30.5%. Notably, process variation

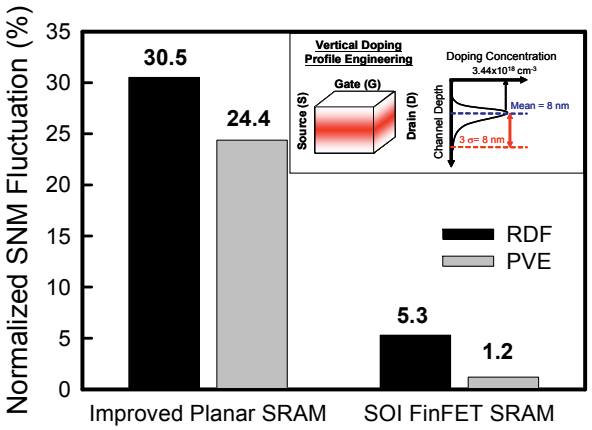

Figure 6: Normalized RDF and PVE induced fluctuations for 16 nm Planar SRAM with improved techniques and SOI FinFET SRAM cells.

induced fluctuation does not reduce much because of the enhanced SCE for vertical doping profile devices. Though the high V_{th} and vertical doping profile engineering can enlarge the SNM and reduce SNM fluctuation. The increased V_{th} also increases the power consumption and slow down the operation speed. Therefore, a 16-nm- gate SOI FinFETs with an aspect ratio (effective fin width/ fin height) of two is then adopted to replace the planar MOSFETs to examine associated fluctuation resistivity against RDF and PVE. To compare the device characteristics on a fair basis, the nominal threshold voltages of SOI FinFETs are calibrated to 140 mV, which is the same nominal threshold voltage as in the original cases. The normalized of RDF and PVE induced SNM fluctuation are shown in Fig. 6, where the nominal SNM is 125 mV. Comparing with conventional 16 nm SRAM, the FinFET SRAM has five times smaller SNM fluctuation and provides sufficient SNM almost as large as that of 65 nm planar SRAM due to the well control of device channel, which reduces both effects of RDF and PVE and shows the promising characteristics in next generation nanoscale transistor. The high SNM, small SNM fluctuation, and low V_{th} of the SOI FinFET SRAM shows the promising characteristics in read / write speed of SRAM.

4. Conclusion

This study for the first time investigated the process-variation-effect and random-dopant-induced SNM roll-off characteristics in nanoscale SRAM circuits by an experimental validated coupled device-circuit simulation. The dependence of SNM and its fluctuation on gate size of transistor has been explored. The RDF dominates the SNM fluctuation than the PVE by a factor of two to four. As gate length scales from 65 nm to 16 nm, the SNM decreases significantly from 138 mV to 20 mV. Moreover, the RDF induced fluctuation is increased by 3 times. To reduce the device variability induced fluctuation in circuit, vertical-doping-profile devices with high V_{th} have been proposed. The SNM is enlarger to 70 mV with a 30.5% SNM fluctuation. Furthermore, to examined the impact of device architecture in improvement of SNM, 16-nm-gate SOI FinFETs are used to examine its capability in SRAM operation. With low V_{th} (140 mV), the SNM of SOI FinFETs SRAM is six times larger than that of the original 16 nm planar MOSFETs due to the superior electrostatic integrity and larger effective device width than planar MOSFETs. Moreover, the SNM fluctuation is reduced by a factor of five. The high SNM, small SNM fluctuation, and low V_{th} of the SOI FinFET SRAM shows the promising characteristics in read / write speed of SRAM. The study investigates the roll-off characteristics of SNM and provides an insight into design of fluctuation resistant nanoscale SRAM. The impact of stain effects enhanced PVE on devices and circuits reliability will be addressed in our future work.

5. Acknowledgment

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-97-2221-E-009-154-MY2 and Contract NSC-96-2221-E-009-210, and by the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan under a 2007-2009 grant.

6. References

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