DC-RF Performance Improvement for Strained 0.13 μm MOSFETs mounted on a Flexible Plastic Substrate

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Abstract — **By applying 0.7% tensile strain to the flexible die of a 0.13 μm thin-body (40 μm) Si MOSFET mounted on plastic, both the DC and RF performance have been improved. The current $I_{d,sat}$ was 14.3% higher, and f_T increased from 103 to 118 GHz with NF_{min} decreasing from 0.89 to 0.75 dB at 10 GHz. These improvements are comparable with those for SiN-capped 90 nm strained-Si nMOS and consistent with device simulations. The approach has the advantages of better RF passive devices on the insulating plastic substrate and low cost.**

Index Terms — **RF Noise, associated gain, MOSFET, plastic.**

I. INTRODUCTION

The major technology challenges for Si RF ICs compared with their III-V counterparts are the lower performance of the active RF transistors [1]-[8], and large loss and noise from the passive devices [9]-[13]. One method to overcome the large RF loss from the passive devices is to integrate RF ICs on insulating plastic. This provides lower RF loss than the poorly isolating VLSI-standard Si substrates, and at a lower cost [1]-[3]. Thin-body Si ICs on plastic can be used for Flexible Electronics, RF ID, wireless Displays and System-on-Plastic [2]-[3], [14], since no practical flexible polymer or organic transistors have been demonstrated for the RF regime. Additionally, the RF performance of 0.18 μm thin-body (30 μm) Si MOSFETs can be improved by applying mechanical strain, which narrows the performance gap between them and III-V transistors [2]-[3]. Here we report the DC to RF performance of 0.13 μm thin-body (40 μm) Si MOSFETs on plastic, aiming to improve the RF performance. Using a microstrip line layout, to shield the RF noise from the low resistivity Si substrate [2]-[4], good performance, in terms of the minimum noise figure (NF_{min}), associated gain and cut-off frequency (f_T) was measured for the 0.13 μm MOSFETs mounted on plastic. The data were close to those for control 0.13 μm devices, indicating little process-related degradation. The DC-RF performances were enhanced by applying 0.7% tensile strain. The improvement of the saturation drain current ($I_{d,sat}$) in the mechanically-strained 0.13 μm device (14.3%) was higher than that for SiN-capped, 90 nm node, strained-Si nMOS (11%) [15], and had a low NF_{min} (0.75 dB at 10 GHz) due to the microstrip line layout [4]. The improved DC-RF performance was confirmed by T-Supreme and Medici simulations (TMA). The improvements arise from the thin body thickness (t_b) and high flexibility, since the surface strain increases with $1/t_b^2$ [16]. The RF noise improvement fits an analytical NF_{min} equation well [8], and it is due to the increase in g_m and the RF gain under strain.

II. EXPERIMENTAL PROCEDURE

Multiple-gate-finger (8, 16, and 32) 0.13 μm MOSFETs [6]-[8] with a novel microstrip line layout [2]-[4] were used in this study. The multiple-gate-finger structure was used to reduce the gate-resistance-generated thermal noise and the microstrip line layouts were designed using Metal-1 as the ground plane to reduce the RF noise from the lossy Si substrate [3]. To achieve integration onto plastic, we first thinned down the Si substrate from 500 μm to 40 μm by using a Chemical Mechanical Polish (CMP) procedure. The thinned die was then glued onto a 180 μm thick light-transparent polyethylene terephthalate (PET) plastic as shown in Fig. 1(a). The plastic had a resistivity of 10^9 Ω-cm. Figure 1(b) shows the 40 μm Si substrate under a large surface strain. Thus, it is possible to apply a large mechanical strain to the flexible Si substrate devices on plastic and not crack the Si substrate. We have calculated the surface strain by using ANSYS 8.0 simulation software and the device characteristics, under various applied tensile strains, using TMA process-device simulation software.

The device characteristics were measured using an HP4155C for DC, HP8510C network analyzer for S-parameter and ATN-NP5B for noise measurements [6]-[8].

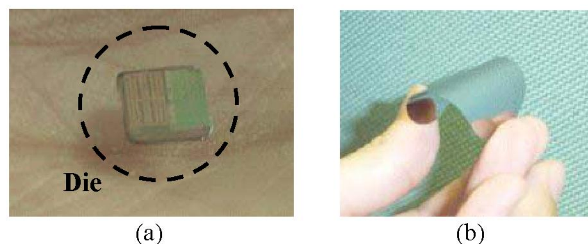

Fig. 1. (a) Image of a die with multiple-gate-finger 0.13 μm RF MOSFETs on transparent plastic (hand-held). (b) Image showing the flexibility of the ~40 μm-thick Si substrate (t_b) under mechanical strain (which is proportional to $1/t_b^2$).

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III. Results and Discussion

A. DC-RF Performance on plastic:

Figure 2 shows a comparison of DC I_d -V_g and I_d –V_d characteristics for the 16-gate-finger n-MOSFET on a VLSI-standard substrate and on plastic with the 40 μm Si. The measured I_d-V_g and I_d–V_d of the 0.13 μm devices, before and after thinning and mounting on plastic, is almost identical. Thus there is little degradation resulting from the thinning-down process and mounting on plastic. Similarly, little change appeared in the measured $|H_{21}|^2$ RF gain for the 0.13 μm MOSFETs, before and after thinning down and mounting, as depicted in Fig. 3. These results represent an improvement over the previous ICP etching and thinning process [2]-[3] since the CMP technique avoids plasma damage. Good device performance is indicated by a f_T of 103 GHz for the 0.13 μm RF MOSFETs.

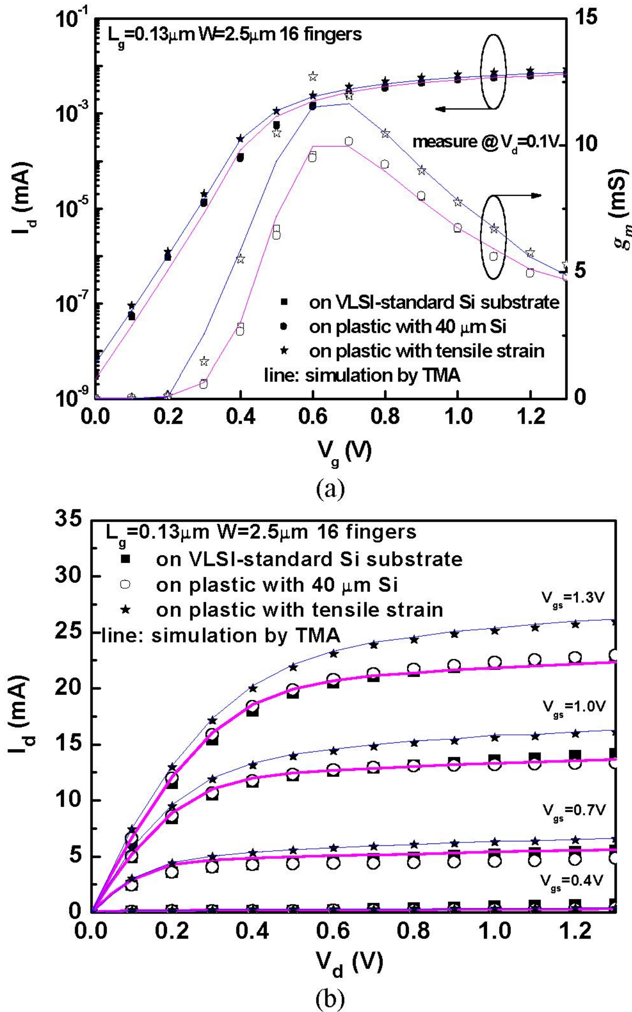

Fig. 2. (a) Measured and simulated I_d-V_g characteristics and (b) I_d-V_d for 16-gate-finger 0.13 μm RF MOSFETs on a VLSI-standard substrate and on plastic with 40 μm Si, with or without tensile strain. The solid lines are the TMA-simulated data for a VLSI-standard Si substrate and on plastic under ~0.7% tensile strain.

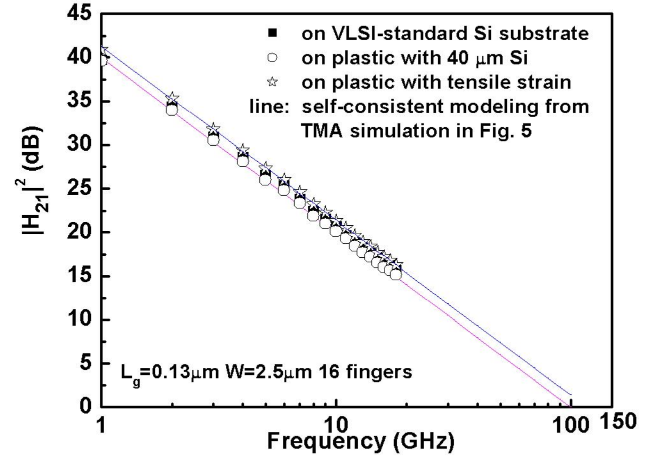

Fig. 3. Measured and simulated $|H_{21}|^2$ as a function of frequency for 16-gate-finger 0.13 μm RF MOSFETs on a VLSI-standard substrate and on plastic with 40 μm Si with or without tensile strain. The line is the modeled data.

B. DC characteristics enhancement by strain:

By exploiting the flexibility of the thin substrate, we have applied a tensile stress to the MOSFETs die on plastic. The large surface strain (ε=3aF/bt$_b^2E$) [15] results from the applied force (F) associated with the bending distance (a) and width (b). Figure 4 shows the thin Si substrate under an applied longitudinal tensile strain, as calculated using ANSYS 8.0 simulation software. The bending distance was 0.17 cm when using 0.8 GPa stress on 40 μm thick Si substrate. This condition gives a tensile strain of 0.7% (= 0.8GPa /115GPa), assuming that the Young's Modulus of Si is 115GPa.

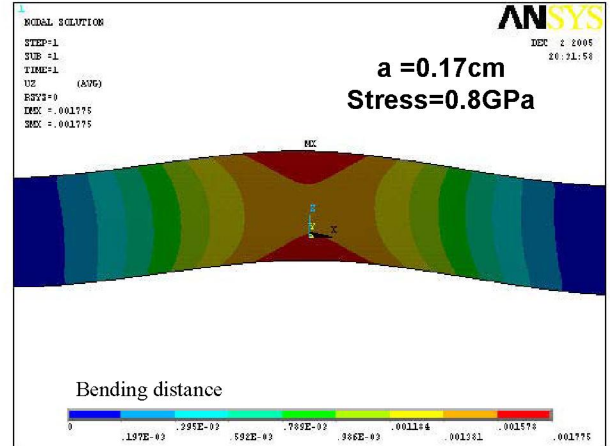

Fig. 4. The mechanical stress calculated by using ANSYS 8.0 simulation software.

Under the same conditions, the experimental data of the effect of strain on the DC characteristics are also shown in Figs. 2(a) and 2(b). After applying a ~0.7% tensile strain, the thin-Si body MOSFETs on plastic showed a 0.045V lower threshold voltage (V_{th}) and a 14.3% higher $I_{d,sat}$.

To understand the improvements, we have used TMA process-device simulation software to simulate the effect of strain on the 0.13 µm MOSFETs. The simulated stress distribution is shown in Fig. 5. A good match between the measured and simulated I_d -V_g and I_d –V_d results were first achieved for the unstrained case to show the accuracy of the TMA simulation and they are included in Figs. 1(a) and 1(b), respectively. Then effect of strain on 0.13 µm transistors themselves was simulated. Figure 6 summarizes the measured and simulated $I_{d,sat}$ improvement as a function of strain. The strain lowers V_{th} ($=\phi_{MS}-Q_{ox}/C_{ox}+2\phi_F+Q_{dpl}/C_{ox}$) because it reduces the energy band-gap (E_G) and thus ϕ_F and Q_{dpl}. A significant $I_{d,sat}$ improvement (14.3%) was seen compared with SiN-capped 90 nm strained-Si nMOS, where the increase was 11% [15]. The effect arises from the $1/t_b^2$ dependence of the strain for thin-body Si. This shows that both the lower RF loss for the passive devices and a higher transistor drive current can be obtained simultaneously using the mechanical strain made possible by using highly-insulating plastic substrates.

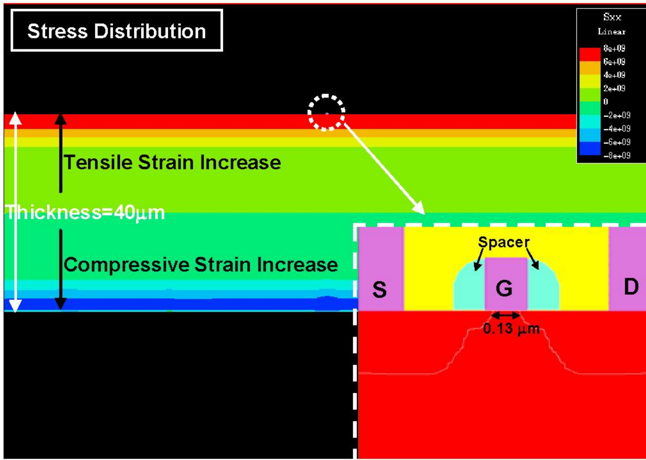

Fig. 5. TMA device simulation of a 40 µm Si-body 0.13 µm RF MOSFETs under applied mechanical strain.

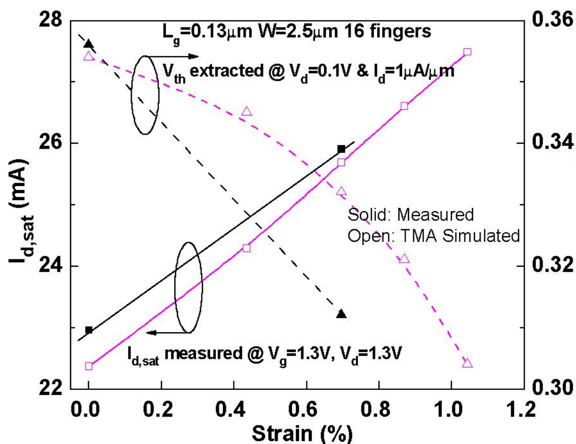

Fig. 6. Simulated (shown red) and measured (shown black) $I_{d,sat}$ and V_{th} versus strain. The strain increases $I_{d,sat}$ but decreases V_{th}.

C. Enhancement of the RF characteristics by strain:

Fig. 3 includes the dependence of the RF current gain $|H_{21}|^2$ with frequency, for a 16-gate-finger 0.13 µm device with tensile strain, was. $|H_{21}|^2$ follows the typical -20 dB/decade slope with increasing frequency. After applying a 0.7% tensile strain to the 40 µm thinned-body Si of the 0.13µm RF MOSFETs, f_T increased from 103 GHz to 118 GHz. These improvements were consistent with the simulations, which are included in Fig. 3.

We also investigated how strain affects the RF noise. Figure 7 shows NF_{min} and the associated gain of the 0.13µm transistors under tensile strain. For the unstrained case, a good NF_{min} of 0.89 dB and associated gain of 14.2 dB at 10 GHz was observed. Under the applied 0.7% tensile strain, better RF characteristics were achieved, such as a lower 0.75 dB NF_{min} and a higher 15.3 dB associated gain at 10 GHz. This is related to the larger g_m, smaller V_{th} and higher $I_{d,sat}$ arising from the strain, as shown in Fig. 2. The lower NF_{min} arises because [2]-[3]:

$$NF_{min} \cong 1 + 2\gamma\,(1 + g_m R_g/\gamma)^{0.5} f/f_T \quad , \tag{1}$$

and that the strain improved the f_T. The close agreement between the measured and simulated NF_{min} also appears in Fig. 7. The detailed device parameters we used are summarized in Table I. The improved NF_{min} and associated gain values are comparable with those for 90 nm node SiN-capped strained-Si nMOS [5], and also depicted in Fig. 7. The large DC-RF improvements with tensile strain are the main advantages of thin-Si-body flexible electronics on plastic, in addition to the improved RF passive device performance [1]-[3].

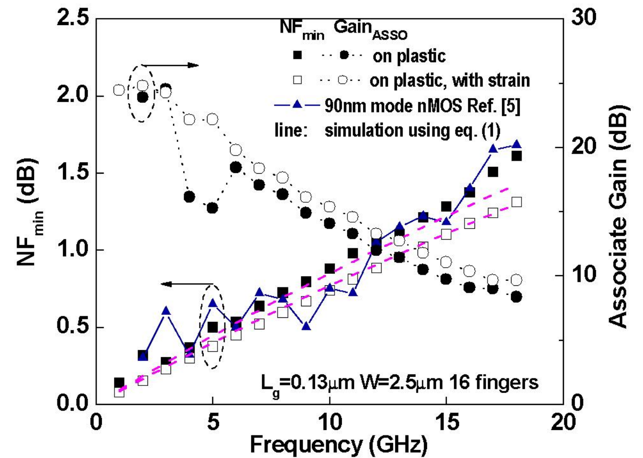

Fig. 7. Measured and modeled NF_{min} and associated gain of 16-gate-finger 0.13 µm RF MOSFETs on plastic and 40 µm Si, with or without tensile strain. The line is the TMA-modeled data and derived from the NF_{min} equation.

Table I. Important device parameters of body-thinned 16-gate-finger 0.13 μm RF MOFSETs, before and after strain.

	before strain	after strain
f_T (GHz)	103	118
γ	1.0	1.0
g_m (S)	0.025	0.032
R_g (Ω)	9.6	9.6

IV. Conclusions

We have successfully demonstrated high DC and RF performance for 0.13 μm RF MOSFETs on 40 μm Si substrates mounted on a flexible plastic base. These devices showed excellent DC and RF performance after applying tensile strain to the thinned-down substrate. The high performance RF transistors are suitable for low-noise ultra-wide band (UWB) (3.1-10.6 GHz) applications.

Acknowledgement

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References

[1] R. Dekker, K. Dessein, J.-H. Fock, A. Gakis, C. Jonville, O. M. Kuijken, T. M. Michielsen, P. Mijlemans, H. Pohlmann, W. Schnitt, C. E. Timmering, and A. M. H. Tombeur, "Substrate transfer: enabling technology for RF applications," *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 371-374, Dec. 2003.

[2] H. L. Kao, A. Chin, C. C. Huang, B. F. Hung, K. C. Chiang, Z. M. Lai, S. P. McAlister and C. C. Chi, **"**Low Noise and High Gain RF MOSFETs on Plastic Substrates,**"** *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 295-298, June 2005.

[3] H. L. Kao, A. Chin, B. F. Hung, J. M. Lai, C. F. Lee, M.-F. Li, G. S. Samudra, C. Zhu, Z. L. Xia and J. F. Kang, "Strain-Induced Very Low Noise RF MOSFETs on Flexible Plastic Substrate," *Symp. on VLSI Tech.*, pp. 160-161, June 2005.

[4] H. L. Kao, A. Chin, J. M. Lai, C. F. Lee, K. C. Chiang and S. P. McAlister, "Modeling RF MOSFETs After Electrical Stress Using Low-Noise Microstrip Line Layout," *RF IC Symp. Dig.*, pp.157-160, June 2005.

[5] K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoom and I. Young, "A comparison of state-of-the art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications," in *Symp. On VLSI Tech.*, pp. 224-225, 2004.

[6] C. H. Huang, K. T. Chan, C. Y. Chen, A. Chin, G. W. Huang, C. Tseng, V. Liang, J. K. Chen, and S. C. Chien, "The minimum noise figure and mechanism as scaling RF MOSFETs from 0.18 to 0.13 μm technology nodes," in *IEEE RFIC Symp.*, pp. 373-376, 2003.

[7] M. C. King, M. T. Yang, C. W. Kuo, Y. Chang, and A. Chin, "RF noise scaling trend of MOSFETs from 0.5 μm to 0.13 μm technology nodes," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 6-11, 2004.

[8] M.C. King, Z. M. Lai, C. H. Huang, C. F. Lee, M. W. Ma, C. M. Huang, Y. Chang and A. Chin, "Modeling finger number dependence on RF noise to 10 GHz in 0.13 μm node MOSFETs with 80nm gate length," *IEEE RF IC Symp. Dig.*, pp. 171-174, 2004.

[9] D. S. Yu, K. T. Chan, A. Chin, S. P. McAlister, C. Zhu, M. F. Li, and Dim-Lee Kwong, "Narrow-band band-pass filters on silicon substrates at 30 GHz," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1467-1470, June 2004.

[10] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, S. P. McAlister and D. L. Kwong, "RF passive devices on Si with excellent performance close to ideal devices designed by electro-magnetic simulation," in *IEDM Tech. Dig.*, 2003, pp. 375-378.

[11] K. T. Chan, A. Chin, Y. B. Chen, Y.-D. Lin, D. T. S. Duh, and W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-Quartz," in *IEDM Tech. Dig.*, 2001, pp. 903-906.

[12] K. T. Chan, A. Chin, C. M. Kwei, D. T. Shien, and W. J. Lin "Transmission line noise from standard and proton-implanted Si," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 763-766, June 2001.

[13] Y. H. Wu, A. Chin, K. H. Shih, C. C. Wu, S. C. Pai, C. C. Chi, and C. P. Liao, "RF loss and cross talk on extremely high resistivity (10K-1MΩ-cm) Si fabricated by ion implantation," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 221-224, June 2000.

[14] T. Takayama, Y. Ohno, Y. Goto, A. Machida, M. Fujita, J. Maruyama, K. Kato, J. Koyama, and S. Yamazaki, "A CPU on a plastic film substrate," *Symp. on VLSI Tech.*, pp. 230-231, June 2004.

[15] T. Ghani, M. Armstron, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. Mclntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 11.6.1-11.6.3, Dec. 2003.

[16] W. Zhao, J. He, R. E. Belford, L.-E. Wernersson, and A. Seabaugh, "Partially depleted SOI MOSFETs under uniaxial tensile strain," *IEEE Trans. Electron Devices,* vol. 54, pp. 317-323, March 2004.