An Image Combiner and Acquisition Interface for Space Remote Sensing Applications

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***Abstract*—high resolution image combination and processing plays an important role in today's satellites' remote sensing applications. This paper presents an image recombination and processing circuitries (ICAI) for one-dimensional multi-strip CMOS image sensors. The proposed system take advantage of the satellites' linear moving property to control the expose time of CMOS image sensor and provides the realtime ability to continuous generate 12,000 × N high-resolution image for space remote sensing applications. The ICAI chip contains an image sensor control logics, image combiner, and host interface, one-dimensional pixel is combined to form a two-dimensional image by proposed circuitry. A prototype chip of ICAI was designed and fabricated with TSMC 0.18 µm CMOS 1P6M technology. The die size is 2.91 mm by 2.91 mm, and the power consumption is 20 mW operating at 8MHz under a 1.8 V supply voltage.**

I. INTRODUCTION

Image sensors play an important role in today's satellites' remote sensing applications, such as forest monitoring, disaster area evaluations, environment monitoring, climate monitoring, etc. Traditionally, charge-coupled devices are utilized in satellite's applications [1]-[4]. Recently, several satellites have adopted both one-dimensional and two-dimensional CMOS image sensors as their components. Satellites' linear moving property [5][6] to control [7][8] the expose time of CMOS image sensor and provides the realtime ability to continuously generate 12,000 × N high-resolution image for space remote sensing applications.

The systems integrated 16 strip CMOS image sensors [9] , 4 ICAIs and a host computer to build a high-resolution multiple-aspect two-dimensional images. To form a high-resolution image, these stripe image sensors are arranged in an interleaved form to avoid the spatial discontinuous. Thus, there is a one-pixel gap between top sensor line and bottom ones. Four strip image sensors are controlled by one ICAI and ICAIs are connected to a host computer for the final image processing. Based on above setup, the propose system provides the real time capability to capture the satellites' remote sensing applications.

In this paper, an interface circuit is proposed, which is applied on the image sensor system for space and remote sensing, which is composed of 16 CMOS image line sensors, 4 proposed interface circuits and 1 host computer. The proposed circuit is designed to provide a super-high resolution image by acquiring image from bundled image sensors and combining line image to a two-dimension image. In addition, the architecture of the proposed circuit can improve the package problem arise from bundling.

The rest of this paper is organized as following. In Section II, the architecture of image sensor system utilized on satellite's remote sensing is described. Section III discusses architectures of the proposed circuit and its specification. In Section IV, implementation result of proposed circuit is presented. Following is the conclusions in this paper (Section V.)

II. THE IMAGE SENSOR SYSTEM FOR SATELLITES' REMOTE SENSING

The architecture of the image sensor system (ISS) for space and remote sensing is shown in Figure 1. To form a super-high resolution image, a total of sixteen image sensors are used. Four image sensors are bundled and collocated with one image combiner and acquisition interface (ICAI), which is a programmable interface between the interleaved image sensor line (IISL) and the host computer, as one group. Due to the package technology, these image sensors should be arranged in an interleaved form, and one-pixel gap between top sensor line and bottom one. ICAI and IISL are designed to be a slave device in the image sensor system. The processed image from ICAI forwards to the host computer for further image processing.

There are three blocks in ICAI – image sensor (IS) control logic, image combiner and host interface. Image sensor control logic activates IISL and acquires image data periodically. One-dimension image is combined to form a two-dimension image by image combiner. Images are stored in the 11k byte SRAM located in image combiner. The host interface receives and parses commands from the host computer. In addition, the host interface wraps the processed image data, and then transmits it back to the host computer for further image processing.

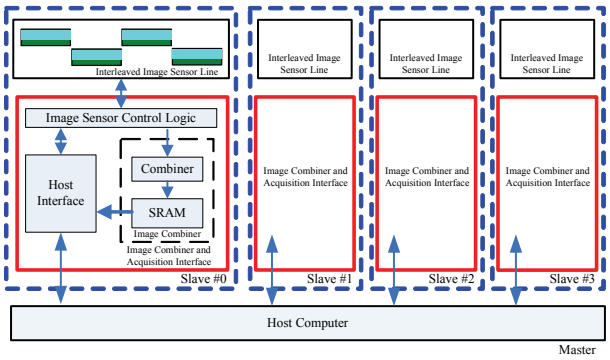

Figure 1: The architecture of the proposed image sensor system.

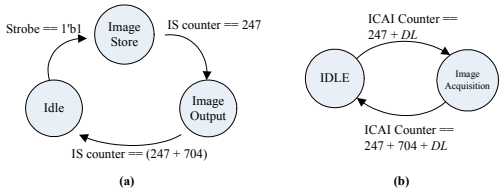

Figure 2: (a) State machine of the CMOS image sensor. (b) State machine of IS control logic.

III. IMAGE COMBINER AND ACQUISITION INTERFACE

In this section, architectures of each block in ICAI and the specification will be discussed.

3.1 Image sensor control logic

In the proposed image sensor system, IISL is utilized 0.18 μm CMOS image sensor technology. There are a total of 704 pixels in one CMOS image sensor, and three states in the image sensor – image store, image exposure and idle state. The state machine of the image sensor is shown in Figure 2(a). Once the image sensor is enabled and activated, image store, image exposure and idle state will be entered in sequence. IS counter in the image sensor increases every 1 clock cycle and auto reset every 1000 cycles; it defines transition condition. The image sensor takes 247 clock cycles to store image and outputs image data for 704 cycles, 1 pixel per cycle.

In ICAI, IS control logic is in charge of acquiring image data from the image sensor. The state machine of IS control logic is shown in Figure 2(b). ICAI counter increases every 1 clock cycle and auto reset every 1000 cycles. Because ICAI only cares about when does image data output, only two states in IS control logic should be needed - image acquisition and idle state. Note that the variable *DL* fine tunes the start point of sampling image data.

3.2 Image combiner

Because of IISL space arrangement, the image data should be rearranged by the image combiner. The process flow of combining image is shown in Figure 3.

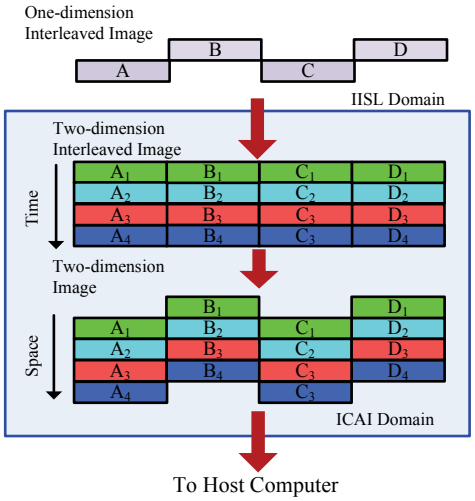

Figure 3: Process flow of combining image.

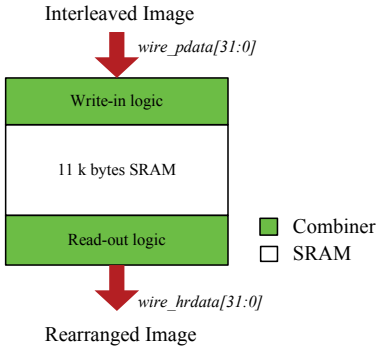

Figure 4: Architecture of the proposed image combiner.

The symbols, A, B, C and D, represent the four image sensors. The subscript in these symbols means their acquisition time index. Due to the acquisition timing, A_1, B_1, C_1 and D_1 are acquired by ICAI at the same time. However, A_1, B_2, C_1 and D_2 should be on the same line. The image combiner is proposed to rearrange image and its architecture is shown in Figure 4. Write-in logic and read-out logic are grouped as combiner part. The most part in CIS image combiner is SRAM. The write-in logic interleaves image data to SRAM and the read-out logic read image data in order. In RTL-level design, CIS interleaved image is denoted by *wire_pdata[31:0]* and rearranged image is denoted by *wire_hrdata[31:0]*.

The SRAM part is configured as Figure 5. A total of 4 banks and 4 blocks in each bank are in the SRAM part. All blocks are the same size, 704 words and 8 bit in a word. Because one ICAI is designed for four CMOS image sensors, 704 pixels and 8 bit resolution for each sensor, four blocks and 704 words in each one is needed. Furthermore, to provide sufficient time to combine image, four banks is preferred.

The process flow of combining image can be mapped to the SRAM configuration. One stage is defined as 1000 clock cycles and a total of four stages of combining behavior are shown in Figure 6. The legend of slash box is the block being written and the legend of hook box is the block begin read. In the stage0, the images from A_1 to D_1 are written into block0, block13, block2 and block15, respectively, and the data in memory bank2 are read out to the host computer. In the stage1, the images from A_2 to D_2 are written into block4, block1, block6 and block3, respectively. Note that A_1, B_2, C_1 and D_2 are in the same memory bank after stage1. In stage2, the A_1, B_2, C_1 and D_2 located in the memory bank0 are read out and the combining of first line is finished. When the stage3 is completed, the ICAI will enter stage0 and repeat the same sequence until a full two-dimension image is outputted.

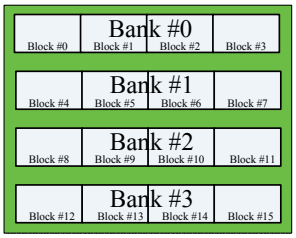

Figure 5: SRAM configuration of the image combiner.

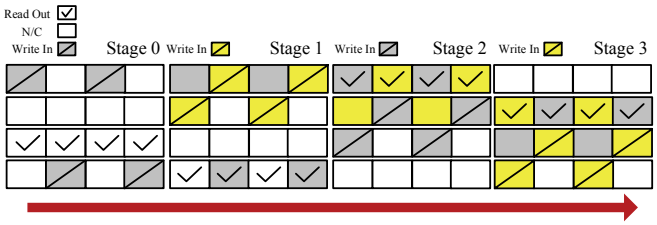

Figure 6: Mapping combining image flow to the SRAM.

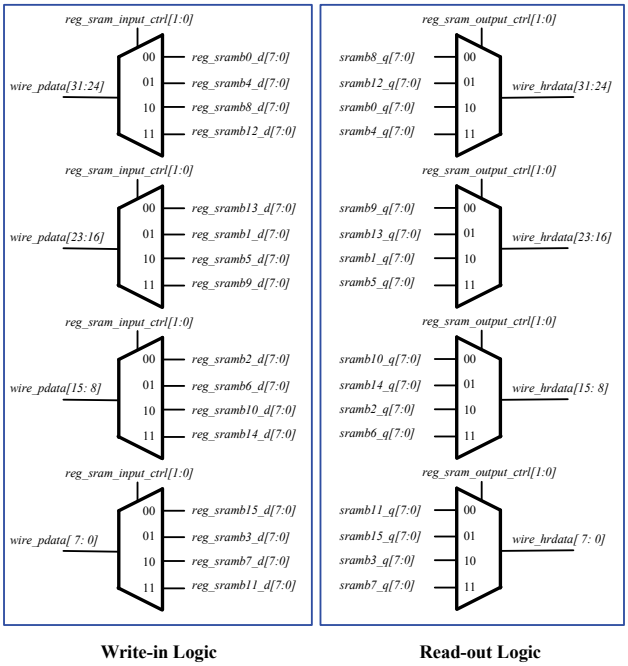

Figure 7: Combination circuit for write-in logic and read-out logic.

The combinational circuits for write-in logic and read-out logic are shown as Figure 7. The stage index is denoted by *reg_sram_input_ctrl[1:0]*. To simplify the design of write-in logic and read-out logic, the *reg_sram_outputt_ctrl[1:0]* represents the stage index as well. SRAM data input and SRAM data output are represented by $reg\_sramb_x\_d[7:0]$ and $sramb_x\_q[7:0]$, respectively. The memory block index is denoted by the subscript "x".

3.3 Host interface

The ICAI to host computer interface is shown in Figure 8. The signal of *HSELx* enables ICAI. The signal of *HWRITE* and *HTRANS* define the states of ICAI. The logic table is listed in Table 1.

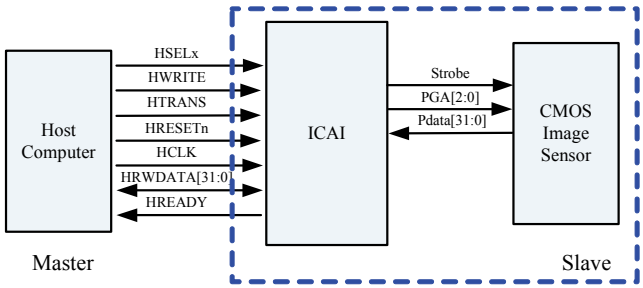

Figure 8: ICAI to host computer interface.

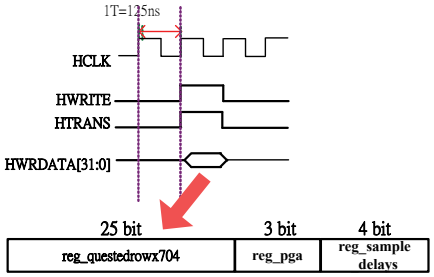

Figure 9: Timing Diagram of configuring ICAI.

The signal of *HCLK* and *HRESETn* provides the clock and reset signal for ICAI respectively. The bus of *HRWDATA* is used to transfer data in and out of ICAI. The signal of *HREADY* indicates if the value on the HRWDATA bus is valid.

The timing diagram of configuring ICAI is shown in Figure 9. The ICAI should be programmed before reading image from the image sensor. A total of 3 registers can be programmable – *reg_pga, reg_sample_delays* and *reg_questedrowx704*. The functions of these registers are described in Table 2.

The timing diagram of reading one-line image data is shown in Figure 10. The ICAI will output image data in the read image state every 1000 clock cycles until the last line of requested image is reached. The value of reg_sample_delays is denoted by variable *DL* in Figure 10. Although the image data is outputted every 1000 clock cycles, only 706 clock cycles are occupied. The output packet includes 2816 pixels, the value of line index and the symbols of *End of Line* or *End of File*. The symbol of *End of File* will only be outputted when the last line of requested image is reached.

A timing diagram of reading full two-dimension image is shown in Figure 11. Note that the ICAI will response the configuration value in first 1000-cycle duration. In the following two 1000-cycle duration, the ICAI will not output any image data because there are 3000 clock cycles latencies for ICAI. The value of reg_questedrowx704 is denoted by variable *N* in Figure 11.

Table 1: Logic table of ICAI.

HSELx	HTRANS	HWRITE	State of ICAI
1	1	1	Configuration
1	1	0	Read Image
1	0	1	Idle
1	0	0	Reserved
0	N/C	N/C	Disable

Table 2: Function of programmable registers.

Register Name	Function
reg_pga	This is a 3-bit width register. It defines the value of programmable gain amplifier (PGA) in the image sensor.
reg_sample_delays	This is a 4-bit width register. It defines the latency of PGA and analog to digital converter (ADC.)
reg_questedrowx704	This is 25-bit width register. It defines the requested multiple of 704-line image. ICAI will stop transferring image out until the last line of requested image is reached.

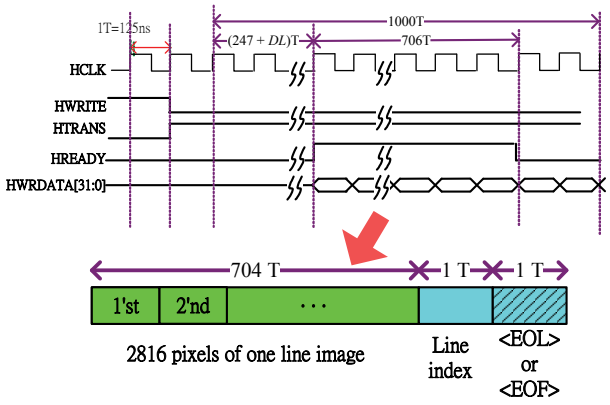

Figure 10: Timing Diagram of reading one-line image data.

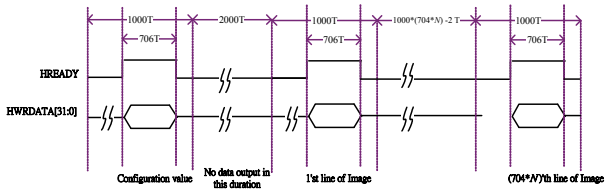

Figure 11: Timing Diagram of reading full two-dimension image.

IV. Implementation Result

The summary of circuit characteristics of this work are listed in Table 3. TSMC 0.18 um CMOS process and Artisan design kit are utilized for the implementation. The post-layout operation frequency is 8MHz. The chip size, core size and power dissipation are about 2.91 mm^2, 1.8 mm^2 and 19.85 m watt, respectively. The sixteen 704 × 8 single port SRAM are the data memory, which is stored the required data for program execution. The physical layout of ICAI is depicted in Figure 12. The core utilization is close to 52.7%. A total of 100 pads are utilized in this work, where 37 input pads, 5 output pads, 32 bi-directional pads and 26 power pads.

Table 3: Circuit summary.

Technology	TSMC 0.18 Logic 1P6M CMOS Process
Clock Rate	8 MHz
Chip Size	2.91 × 2.91 mm^2
Core Size	1.80 × 1.80 mm^2
Power Dissipation	19.85 m watt (post-layout simulation)
On-Chip Memory	16 single-port 704 × 8bit SRAM

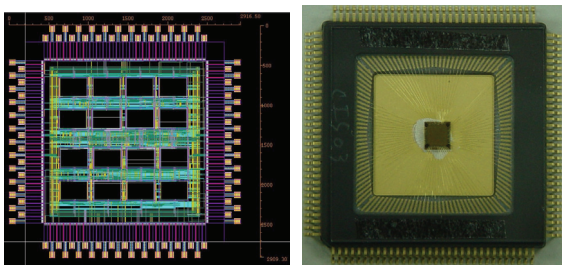

Figure 12: Chip layout of ICAI and photograph of packaged ICAI.

V. Conclusion

A circuit for super-high resolution remote sensing is designed in this paper; it acquires image from bundled image sensors and combine line image to a two-dimension image. Furthermore, the proposed circuit can improve the package problem arise from bundling. The combined image will be wrapped and forward to the host computer for further image processing. This work is manufactured in TSMC 0.18 μm CMOS 1P6M technology and operates at 8MHz; its area is 2.91 mm^2 and it consumes 20 mW under a 1.8 V supply voltage.

Acknowledgment

This research is supported by Chip Implementation Center, Taiwan and National Science Council, Taiwan. (contract numbers: NSC-97-2220-E-009-042, NSC-97-2220-E-009-005, NSC-98-2220-E-009-002)

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