2009 Asian Test Symposium

A Low-Cost Output Response Analyzer for the Built-in-Self-Test Σ-Δ Modulator Based on the Controlled Sine Wave Fitting Method

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***Abstract*—This paper proposes a low-cost output response analyzer (ORA) for the built-in-self-test (BIST) Σ-Δ ADC based on the controlled sine wave fitting (CSWF) method. The ADC under test (AUT) is composed of a design-for-digital-testability (DfDT) second-order Σ-Δ modulator and a decimation filter. The CSWF BIST procedure requests an ORA to accept the output of the AUT and calculates the offset, the amplitude of the stimulus tone response, and the total-harmonic-distortion-and-noise (THD+N) power in three successive BIST steps respectively. Each BIST step needs an accumulator to conduct the specified BIST function. By sharing an accumulator for every BIST step, the proposed ORA design contains only 1.9k gates without loss of computational accuracy. The hardware is only 34% of the original design. Simulation results show that the proposed ORA presents accurate SNDR results for the 1 kHz tests.**

I. Introduction

Testing analog and mixed-signal (AMS) circuits is very costly and troublesome because of the requirements of high-quality analog stimuli and ultra-low noise testing environment. Furthermore, the numbers of testing parameters for AMS products are usually quite large [1] which considerably increase the test time. The too high test cost shrinks profit margins of high-end AMS products such as high-resolution Σ-Δ ADCs. Making testing Σ-Δ ADC cheaper and simpler without compromise of the testing accuracy thereby becomes an important issue for industry. Built-in-self-test (BIST) and design-for-digital-testability (DfDT) techniques can help to address high testing cost [2], [3], [4], [5].

The DfDT structures for Σ-Δ modulators are very appealing approaches [6], [7], [8]. With a few additional analog switches, the DfDT structures can reconfigure the Σ-Δ modulator to accept Σ-Δ modulated bit-streams as the test stimuli in the test mode. The single-bit feature of the digital stimuli ensures the generated test stimuli are purely linear. The digital stimuli also have very high in-band signal-to-noise-and-distortion ratio (SNDR) owing to the noise shaping and oversampling nature of Σ-Δ modulation. Hence, expensive AMS automatic testing equipment (ATE) is no longer necessary. Since the DfDT structures reuse most of the circuit components of the ADC under test (AUT) in both the normal mode and the test mode, they provide many additional benefits such as high fault observability, high measurement accuracy, and the capability of conducting at-speed tests [8].

To further reduce the test cost, making the DfDT Σ-Δ modulator built-in self-testable is preferable. This can be done by integrating the digital stimulus generator (DSG) and the digital output response analyzer (ORA) with the DfDT AUT. Such a BIST design needs no ATE at all. Hence, the only test cost is the added BIST circuitry.

The digital resonator embedded with a digital Σ-Δ modulator well suits for implementing the required DSG for the DfDT Σ-Δ AUT [9]. The hardware cost is low since the design eliminates the need for parallel multiplier. Besides, the amplitude and frequency of the generated Σ-Δ modulated bit-stream are well controlled if the stimulus frequency is not too high [9].

With respect to the ORA, a conventional approach is to analyze the output of the AUT in frequency domain using Fast Fourier Transform (FFT) analysis [10]. However, performing FFT is too costly because conducting FFT requires lots of hardware resources such as bulky memory and a complex CPU/DSP. Alternatively, Mattes et. al. proposes a controlled sine wave fitting (CSWF) method that calculates the SNDR of the AUT in time domain [11]. The CSWF method benefits from no output waveform has to be temporarily stored. As a result, the BIST circuitry can be made much smaller.

In [12], we proposed a BIST Σ-Δ ADC prototype based on the CSWF method. The same DfDT second-order Σ-Δ modulator in [8] is used as the modulator under test (MUT), and an FPGA board implements the decimation filter and the BIST circuitry. Experimental results show that the BIST design can accurately calculate the test parameters such as the offset, the gain error, the SNDR, and the dynamic range of the Σ-Δ AUT for the 1kHz tests. Yet the hardware overhead can be further reduced.

This paper presents a low-cost ORA design for the CSWF BIST Σ-Δ ADC in [12]. By sharing the accumulator for every BIST step, the proposed ORA requires only one accumulator instead of three. As a result, the overall hardware of the proposed ORA contains only 1.9k gates. Compared with the design in [12], the gate count is only 34%. The proposed

1081-7735/09 $26.00 © 2009 IEEE
DOI 10.1109/ATS.2009.88

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ORA design provides the same ORA functions with the same resolution. Hence, the test accuracy is kept the same. This paper is organized as follows: Section II reviews the CSWF BIST Σ-Δ ADC in [12]. The circuit design of the proposed ORA are depicted in Sec. III. Section IV shows the simulation results. Finally, Section V concludes this work.

II. Review of the BIST System

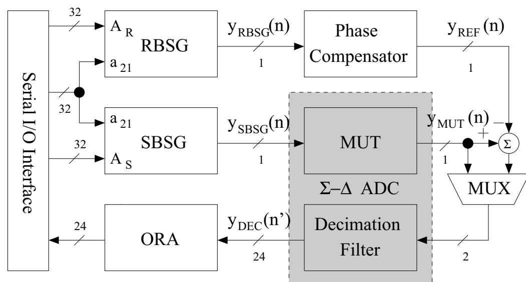

Figure 1. Block diagram of the CSWF BIST system

The idea of the CSWF method is that the signal and the total-harmonic-distortion-and-noise (THD+N) powers can be calculated separately in time domain. In practice, the digital output of an ADC consists of the stimulus tone, the offset, and the THD+N parts. The stimulus tone response may experience a gain error and a phase error induced by the AUT. If we can generate an error-free digital reference signal which is identical to the stimulus tone part of the output response, then the THD+N signal can be obtained by subtracting the error-free digital reference signal and the offset from the digitized output waveform.

The block diagram of the CSWF BIST system in [12] is shown in Fig. 1. The whole BIST system consists of the Σ-Δ ADC, two bit-stream generators (BSGs) as the DSG, the ORA, the phase compensator, and an optional serial I/O interface. Since the phase shift for the Σ-Δ modulator is almost a constant due to its over-sampling nature, the transfer function of the phase compensator is as simple as z^{-2}.

Two identical BSGs are used in Fig. 1. The first one is the stimulus bit-stream generator (SBSG) for generating the digital stimuli for the AUT. The second one is the reference bit-stream generator (RBSG) for generating the aforementioned digital reference signals. The amplitudes of the generated stimulus tones can be well controlled [9]. In particular, we use A_S to represent the amplitude of the stimulus tone generated by the SBSG, and A_R for that by the RBSG. The input parameter a_{21} sets the frequency of the generated stimulus tone.

The ORA calculates the offset, the amplitude of the stimulus-tone response, and the THD+N power in three BIST steps respectively [12]. Every BIST step conducts a coherent test and acquires N decimated output samples for analysis, where N is selected to be a power of two to simplify the hardware implementation. The ORA functions are discussed as follows.

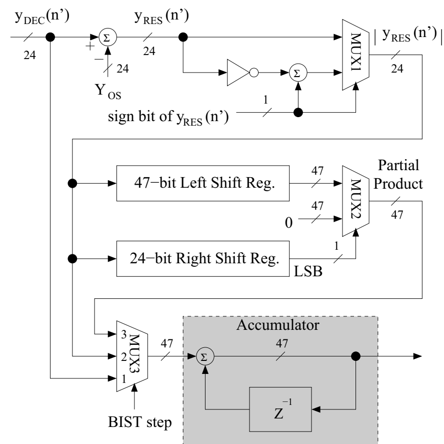

Figure 2. Schematic of the Proposed ORA

1) BIST Step 1: Calculating the Offset: In the first BIST step, the ORA estimates the offset Y_{OS} of the AUT by

$$Y_{OS} = \frac{1}{N}\sum_{n'=1}^{N} y_{DEC}(n'). \tag{1}$$

Since N is a power of 2, the division can be realized by wiring. A simple accumulator is used to implement (1).

2) BIST Step 2: Calculating the Amplitude of the Response: The ORA removes the estimated offset Y_{OS} from the decimated response $y_{DEC}(n')$ first, and calculates the amplitude of the offset-free response $y_{RES}(n')$ according to

$$Y_{AMP} = \frac{1}{N}\sum_{n'=1}^{N} |y_{RES}(n')|. \tag{2}$$

An additional accumulator with an absolute function circuitry are used to implement (2) in [12].

3) BIST Step 3: Calculating the THD+N Power: The ORA first derives the THD+N signal, $y_{RES}(n')$, by subtracting the offset and the reference signal ($y_{RBSG}(n)$) from the output of the AUT. Then, the ORA conducts the following function to calculate the THD+N power in the passband:

$$P_{THDN} = \frac{1}{N}\sum_{n'=1}^{N} |y_{RES}(n')|^2. \tag{3}$$

Since $y_{RES}(n')$ is decimated by a factor of 128, the ORA has sufficient time to condcut the only multiplication by a simple serial multiplier. In [12], Equation (3) is implemented with the other accumulator, an absolute-value translator, and a serial multiplier.

III. The ORA Circuitry

The ORA design in [12] is composed of three independent blocks including the offset estimator, the amplitude estimator, and the power estimator. According to Sec. II, the three estimators work successively and each estimator consists of an accumulator. In addition, the power estimator for the last BIST step needs a serial multiplier which contains the fourth

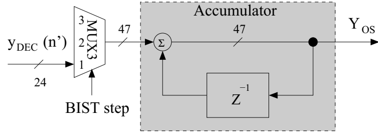

Figure 3. BIST Step 1: Calculating the Offset

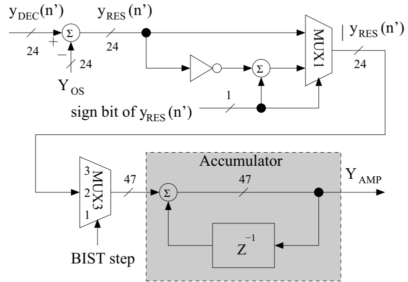

Figure 4. BIST Step 2: Calculating the Amplitude of the Response

accumulator for summing up the partial products. Since only one of the accumulators is working at a time, the ORA functions can share the same accumulator using the time-multiplexing technique to save the hardware.

Based on the above discussion, we propose a new ORA design as shown in Fig. 2. The ORA contains only one accumulator to perform all the necessary ORA functions. The only accumulator is shared between every BIST step. Fig. 3 to 5 illustrate the reconfigured ORA in every BIST step.

In the first BIST step, the output of the decimation filter passes through the multiplexer MUX3 and the accumulator calculates the offset according to (1). In the second BIST step, the same accumulator accepts the absolute value of $y_{RES}(n')$ and estimates Y_{AMP} according to (2). In the last BIST step, the only accumulator sums up the partial products and accumulates the square terms as shown in Fig. 5.

The synthesis results using a 0.18 μm cell library shows that the proposed ORA reduces the gate count from 5.6k to 1.9k, saving 66% hardware. In addition, Since the proposed ORA provides the same functions as (1), (2), and (3) with the same resolution, there is no loss of computational accuracy. Table I summarizes the hardware cost of the BIST design using the proposed ORA. 23% of the BIST circuitry belongs to the proposed ORA while the ratio of the design in [12] is 47%.

IV. Simulation Results

Behavioral simulations are used to verify the BIST system. The MUT itself is simulated with the fully-settled-linear-behavior-plus-noise (FSLB+N) model [13]. This model has been shown being able to well predict the performance of the DfDT Σ-Δ modulator. The necessary model parameters are set according to the practical design in [8]. The OPAMPs have an offset voltage of 0.41 mV, an open-loop gain of 75 dB, and an output swing of $\pm$2.8 V. The FSLB+N model assumes all transient responses are fully settled. The sampling capacitors of the first integrator stage have -50 dB mismatch and the

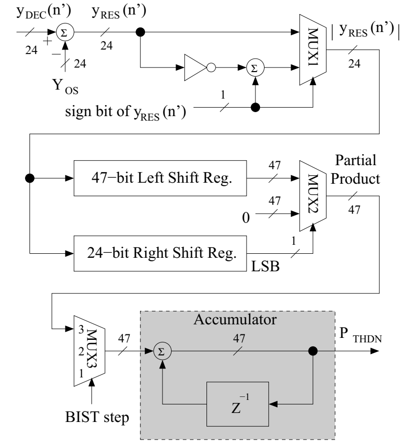

Figure 5. BIST Step 3: Calculating the THD+N Power

Table I
Summary of the BIST Hardware Cost

Block	BIST design in [12]	BIST design with the proposed ORA
	Gate counts	
ORA	5.6k	1.9k
BSG	2.35k×2	2.35k×2
Serial I/O	1.6k	1.6k
Total BIST Circuitry	11.9k	8.2k

KT/C noises of the switched capacitors are considered.

The sampling frequency is 6.144 MHz while the OSR is set to 128. The ORA respectively analyzes 2^{18} and 2^{11} samples of $y_{MUT}(n)$ and $y_{RES}(n')$ for every BIST step. To fulfill the coherent test requirement, the stimulus frequency is set to $43/2^{18}$ times the sampling frequency which is around 1 KHz.

Figure 6 depicts the output spectra in the last BIST step of the -6 dBFS, 1kHz test. The BIST design successfully reduces the offset and the stimulus tone of the MUT's response, $y_{MUT}(n)$, from -75.8 dBFS and -6.0 dBFS to -110.1 dBFS and -114.5 dBFS respectively. Apparently, the decimated residue signal, $y_{RES}(n')$, is almost the same as the noise floor of $y_{MUT}(n)$. The spectra prove that the proposed ORA executes the BIST functions correctly. The BIST SNDR result and the one obtained by using conventional FFT analysis are 75.8 dB and 75.9 dB for this test. The two analysis methods have only 0.1 dB SNDR difference. The subtle difference comes from that conventional FFT analysis ignores the noise power on the offset and the stimulus tone frequency bins while the BIST takes them into account.

Figure 7 shows and compares the simulation results of the dynamic range tests using the two analysis methods. The stimulus amplitude is swept from -60 dBFS to -4 dBFS while the stimulus frequency is keeping at 1 kHz. The SNDR differences between both methods are no more than ±1.2 dB.

Figure 8 shows SNDR results vs. stimulus frequency. The stimulus amplitude is the same -6 dBFS. The corresponding SNDR differences of the two analysis methods are within 1.5 dB for the stimulus frequency less than 8 kHz, but are

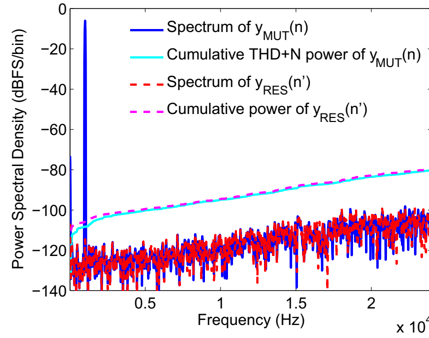

Figure 6. Spectra and cumulative THD+N power plots of $y_{MUT}(n)$ and $y_{RES}(n')$ in the last BIST step of the same -6 dBFS, 1 kHz test

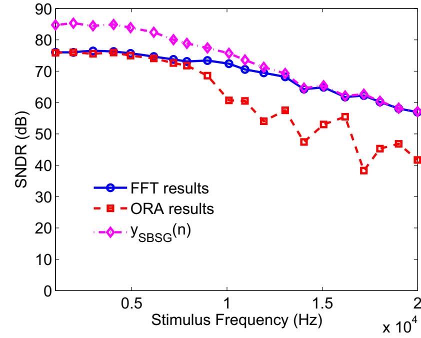

Figure 8. SNDR results of the proposed ORA design, the FFT analysis, and the corresponding $y_{SBSG}(n)$ at different stimulus frequencies

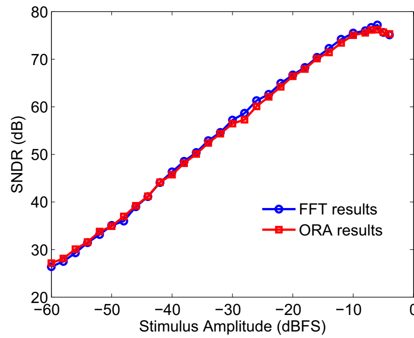

Figure 7. SNDR results of the dynamic range tests

larger for the stimulus frequency higher than 8 kHz. Note that the limited test bandwidth is due to the design of the BSGs, not the ORA. The test accuracy degradation is because the high-frequency digital stimuli have poor in-band SNDRs as shown in Fig. 8. The noisy stimulus causes the stimulus tone of $y_{MUT}(n)$ can not be completely removed. Since the ORA calculates the residue stimulus tone as a part of the desired THD+N signal, the BIST SNDR results become worse. Table II summarizes the simulated BIST results with the proposed ORA design.

Table II
BIST RESULT SUMMARY

Test item	Analysis method		
	Conventional FFT	With the ORA in [12]	With the proposed ORA
Peak SNDR	75.9 dB	75.8 dB	75.8 dB
Dynamic range	86.4 dB	87.1 dB	87.1 dB
Offset	−75.8 dBFS	−75.8 dBFS	−75.8 dBFS
Test bandwidth	10 kHz	8 kHz	8 kHz
Hardware cost	CPU/DSP/memory	5.6k gates	1.9k gates

V. CONCLUSIONS

This paper proposes a low-cost ORA for the BIST Σ-Δ ADC based on the CSWF method. The ORA calculates the offset, the amplitude response, and the THD+N power successively in three BIST steps. Each step needs an accumulator as a building block. By sharing the same accumulator for every BIST step, the proposed ORA contains only 1.9k gates according to the synthesis results. The gate count is only 34% that of the original design. Furthermore, the proposed ORA does not sacrifice the computational accuracy. Simulation results verify that the BIST ADC with the proposed ORA provides accurate SNDR results as the conventional FFT analysis does.

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