A Low-Voltage CMOS LNA Design Utilizing the Technique of Capacitive Feedback Matching Network

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***Abstract*— In this paper, a CMOS low noise amplifier (LNA) with a new input matching topology has been proposed, analyzed, and measured. The input matching network is designed through the technique of capacitive feedback matching network. The proposed LNA which is implemented in a 0.18-μm 1P6M CMOS technology is operated at the frequency of 12.8 GHz. It has a gain S21 of 13.2 dB, a noise figure (NF) of 4.57 dB and an NF_{min} of 4.46 dB. The reverse isolation S12 of the LNA can achieve -40 dB and the input and output return losses are better than -11 dB. The input 1-dB compression point is -11 dBm. This LNA drains 10 mA from the supply voltage of 1 V.**

I. Introduction

In the design of RF CMOS LNAs, it is known that the key performance parameters are power gain and noise figure (NF), besides stability, linearity and isolation. The goal of LNA design is to achieve maximum power gain and minimum NF simultaneously at any given amount of power dissipation. To reach this goal, the input impedance Z_{in} of a LNA must be kept close enough to the optimum source noise conjugate impedance $Z^*_{n,opt}$.

Conventionally, the inductive source degeneration technique is used to achieve this goal. However, this inevitably decreases the equivalent transconductace of the LNA at high frequencies, which reduces the power gain [2]. To retain the power gain, the power dissipation has to be increased significantly. For the LNAs operated above 10 GHz, an accurate and small source degeneration inductor value is required. The variations of the inductance makes Z_{in} not close enough to $Z^*_{n,opt}$. To realize the accurate and small source degeneration inductance, microstrip line can be used at frequencies higher than 20 GHz. But it is chip area consuming if used at frequencies below 20 GHz.

So far, many high frequency RF CMOS LNAs have been proposed [3]-[7]. Among them, the proposed LNA structure at 17 GHz and 24 GHz [3] uses microstrip line to realize accurate source degeneration inductor. But the chip area is still large. The multistage common-source amplifiers are used in the LNAs in [4]-[6]. Each stage is designed with inductive source degeneration. To reach sufficient gain and good stability at frequencies from 8 GHz to Ku-band, high power dissipation is needed [4]-[6]. Although power gain match can be achieved by utilizing the input microstrip line in the LNA design [7], but Z_{in} is not equal to $Z^*_{n,opt}$ in this case. Thus the minimum NF and maximum power gain cannot be achieved simultaneously.

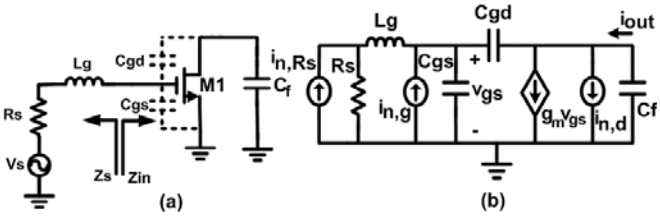

Fig. 1. a) The common-source amplifier as the input stage, b) The small-signal equivalent circuit for noise calculations.

In this paper, a new LNA design technique is proposed, which uses the gate-drain capacitance and output capacitance of the input MOSFET to form the capacitive feedback matching network and bring the input impedance Z_{in} close to the optimum source noise conjugate impedance $Z^*_{n,opt}$. The current of the input MOSFET is then amplified by a RF current-mirror amplifier. It is shown that the proposed LNA has a high power gain of 13.2 dB, a high reverse isolation of $-40\ dB$, and a good linearity with the input 1-dB compression point at $-11\ dBm$. The NF and NF_{min} of the proposed LNA are 4.56 dB and 4.46 dB, respectively. Therefore, the LNA has good noise performance because NF and NF_{min} are very close to each other. Besides, the proposed LNA has a small power consumption of 10 mW under the low power supply voltage of 1 V.

The details of design methodology and the designed CMOS circuit of the LNA are presented in Section II. Section III describes the experimental results. Finally, conclusion is given in Section IV.

[0]this work was supported by National Science Council (NSC) Taiwan, under the Grant NSC-94-2215-E-009-043

II. Operational Principles and Circuit Implementations

The common-source amplifier as the input stage is shown in Fig. 1(a), where Z_s is the impedance seen from the right node of the input matching inductor L_g, Z_{in} is the input impedance of M1, C_{gd} is the gate-drain capacitance, C_{gs} is the gate-source capacitance, C_f is the output loading capacitance which is the input capacitance of the next stage, R_s is the signal-source resistance, and V_s is the input signal voltage source. By using Millers theorem on C_{gd}, the input impedance Z_{in} can be derived as

$$Z_{in} = \frac{R_f}{(Q_f^2+1)} + \frac{1}{j\omega_o(C_{gs}+C_{gd})(\frac{1}{Q_f^2}+1)} \quad (1)$$

where $Q_f = \omega_o(C_{gs}+C_{gd})R_f$, $R_f = \frac{1}{g_m}\frac{C_f}{C_{gd}}$, g_m is the transconductace of M1, and ω_o is the operating angular frequency. As may be seen from the above equations, both C_{gd} and C_f with g_m together provide a real term R_f which contributes to the real input impedance in Z_{in}. They are called the capacitive feedback matching network.

Fig. 1(b) shows the small-signal model of the input stage for noise calculation. Three noise sources have been considered in Fig. 1(b). They are the thermal noise of the source resistance i_{n,R_s}, the thermal noise of the channel current $i_{n,d}$, and the gate induced current noise $i_{n,g}$.

The noise factor F is defined as the total output noise power divided by the noise power at the output due to the input source. F can be expressed as

$$\begin{aligned} F &= 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_s}\Bigg\{\Big(|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\Big)^2 \\ &+\big(R_s^2 - s^2L_g^2\big)\Big(\frac{1}{R_f^2} - \frac{\alpha^2\delta}{5\gamma}(1-|c|^2)s^2C_t^2\Big) \\ &-\big(sC_tR_s\big)^2\Big[1+|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\Big]^2 + \frac{2R_s}{R_f}\Bigg\} \end{aligned} \quad (2)$$

where $C_t = C_{gs}+C_{gd}$, g_{d0} is the zero-bias drain conductance, γ is thermal noise coefficient, δ is the gate induced current noise factor, $\alpha \equiv g_m/g_{d0}$, and c is a correlation coefficient theoretically equal to $j0.395$ [8]. By taking the derivatives of (2) with respect to R_s and L_g and let the derivatives equal to zero, optimum source noise impedance $Z_{n,opt} = R_{s_{n,opt}} + j\omega L_{g_{n,opt}}$ corresponds to minimum noise figure can be written as

$$\begin{aligned} Z_{n,opt} &= \frac{\sqrt{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}} + j\Big(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\Big)}{\Bigg\{\alpha^2\frac{\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}+\Big(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\Big)^2\Bigg\}} \\ &\times\frac{1}{\omega(C_{gs}+C_{gd})}. \end{aligned} \quad (3)$$

Using (1), (3) can be re-expressed in $Z^*_{n,opt}$ as

$$Z^*_{n,opt} = Re[Z_{n,opt}] + \beta Imag[Z_{in}]. \quad (4)$$

$$\beta = \frac{\Big(1+\frac{1}{Q_f^2}\Big)\Big(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\Big)}{\Bigg\{\alpha^2\frac{\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}+\Big(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\Big)^2\Bigg\}} \quad (5)$$

From (4), the imaginary part of $Z^*_{n,opt}$ is nearly the same as the imaginary part of Z_{in} and expressed as $\beta Imag[Z_{in}]$.

For the circuit in Fig. 1(a), the condition for maximum input power transfer (thus power gain) is $Z_{in} = Z_s^*$ and that for the minimum noise figure is $Z_s = Z_{n,opt}$. Ideally, we have the condition for maximum power gain and minimum noise figure is $Z_{in} = Z^*_{n,opt}$. From (1), (3), and (4), this condition can be satisfied if β is close to 1 and

$$\frac{1}{g_m(Q_f^2+1)}\frac{C_f}{C_{gd}} = R_{s_{n,opt}}. \quad (6)$$

In the proposed technique of capacitive feedback matching network, the value of β is more close to 1 as compared to the inductive source degeneration technique. Moreover, (6) can be satisfied by designing suitable device parameters g_m, C_{gd}, and C_{gs} of the device M1, which are related to gate-source voltage V_{gs} and transistor size W/L. In other words, the proposed design technique and input stage in Fig. 1(a) helps to maximize the power gain and to minimize the noise figure simultaneously by bringing Z_{in} close to the optimum source noise conjugate impedance $Z^*_{n,opt}$.

It can be seen from (1) that without the feedback gate-drain capacitance C_{gd}, the input impedance of the common-source amplifier would have no real part. However, the optimum source noise impedance $Z_{n,opt}$ in (3) has a real part. Then it is impossible to satisfy the condition $Z_{in} = Z^*_{n,opt}$. In the proposed technique, C_{gd} and the capacitive feedback matching network are used to satisfy the condition. Thus the technique is called the technique of capacitive feedback matching network.

The complete circuit of the proposed LNA with the output stage is shown in Fig. 2 where in the LNA stage, M1 with the input amplifier transistor and M2/M3 forms the current-mirror amplifier as the second amplifier stage. The effective transconductance of the two stages is given by

$$|G_{eff}| = \frac{1}{2R_s}\Big(\frac{\omega_T}{\omega_o}\Big)\frac{g_{m3}}{\omega_o C_f} \quad (7)$$

where ω_T is unit gain angular frequency, g_{m3} is the transconductance of M3, C_f is the total capacitance at the drain of M1 which is dominated by C_{gs} of M2 and M3. M2 is used as the master transistor of the MOS current-mirror amplifier along with the slave transistor M3. The size of M2 is chosen to be very small as compared to M1 and M3 to obtain a higher current gain. Since the cascode structure is not adopted, the proposed LNA can be operated at a low supply voltage.

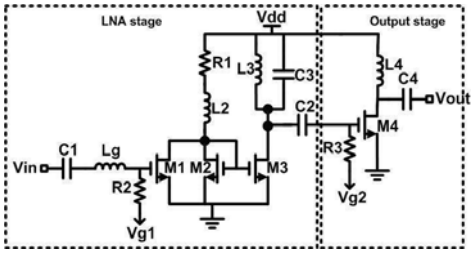

Fig. 2. The complete circuit diagram of proposed LNA.

In order to make the parallel resonance circuit behave like a capacitive load, a parallel resonance circuit composed of L2 and the parasitic capacitance at the drain of M1 resonates at the frequency below the operating frequency of the LNA. R1 is used to ensure stability. C1 and C2 are dc blocking capacitors. The tank L3 and C3 is used to resonate with the parasitic capacitances of the gate M4. R2 is used to provide the gate dc bias of M1 and chosen large enough that its equivalent noise current is small enough to be ignored.

In the output stage, the output buffer composed of M4, L4, C4, and R3, is designed for the measurement purpose. R3 is used to provide the gate dc bias of M4, C2 and C4 is the dc blocking capacitor. The output inductor L4 is used to resonate with the parasitic capacitances at the drain of M4. The voltage gain of the buffer is unity.

Form (5) and under the condition of the short channel devices, the expected noise parameters of device are $\alpha = 0.6$, $\delta/\gamma = 2$, $|c| = 0.5$ and $Q_f = 2$. In the proposed LNA, the β is 0.87, while the β of the of the LNA with source degenerative method is equal to 0.82.

It is important to notice that some amount of mismatch in the input matching $Z_{in} = Z_s^*$ has negligible effect on the LNA performance, while the mismatch in $Z_s = Z_{n,opt}$ directly affects the NF [9]. Thus $Re[Z_{in}]$ is designed to be equal to the calculated $R_{s_{n,opt}}$ which is equal to 48Ω.

III. Experimental Results

Based upon the proposed technique of capacitive feedback matching network and LNA structure, an experimental chip of a LNA operated at 13 GHz was designed and fabricated in 0.18-μm CMOS technology. The chip photograph is shown in Fig. 4 and the total die area is $746.5\mu m \times 884.6\mu m$ including all testing pads and dummy metals. The performance of the fabricated LNA circuit was tested through on-wafer probing technique. Fig. 3(a) shows the measured S21 of 13.2 dB at 12.8 GHz and a low input return loss S11. Fig. 3(b) shows the measured output return loss S22 and reverse isolation S12. As seen from Figs. 3(a) and 3(b), the measured reverse isolation S12 of the LNA achieves -40 dB whereas the input and output return losses are better than -11 dB. The frequency shift from 13 GHz to 12.8 GHz is due to the inaccurate modeling of planar inductor at high frequency.

The fabricated LNA has a NF of 4.57 dB and the minimum noise figure NF_{min} of 4.46 dB at 12.8 GHz as shown in Fig. 3(c). As may be seen from Fig. 3(c), NF and NF_{min} are very close to each other over a large frequency range. Thus the proposed LNA is insensitive for operating frequency variations. The measured output power versus the input power is shown in Fig. 3(d) where the input referred 1-dB compression gain is -11 dBm.

The measured performance parameters are summarized in Table I where comparisons with other published works are also listed. A figure of merit (FOM) [10] used for comparisons is defined in the following

$$FOM = \frac{[10^{(S_{21}+IIP3)/10}] \times \frac{f_c}{10^9}}{[10^{NF/10} - 1] \times \frac{P_{DC}}{10^{-3}}}. \quad (8)$$

This FOM takes into account the operating frequency f_c, NF, S21, and IIP3 of LNA. Based upon Table I, it is clear that the proposed LNA outperform all the other LNAs with a higher value of FOM. As expected, the proposed LNA with the technique of capacitive feedback matching network has high power gain and low noise figure under low power dissipation. It can be operated at a low supply voltage of 1 V since the cascode structure is not adopted. However, it still has a high reverse isolation.

IV. Conclusion

A new LNA structure with the technique of capacitive feedback matching network is proposed and analyzed. An experimental chip of 13-GHz LNA has been successfully designed and fabricated. The measurement results have shown that the proposed LNA can achieve minimum noise figure and maximum power gain simultaneously. Moreover, the NF is insensitive to the large operating frequency shift.

Future research will be conducted to design LNAs at frequencies below 24-GHz or higher using the technique of capacitive feedback matching network and integrated them with mixers. Since the proposed LNA can be designed in transconductance mode with an output current to drive the current-mode mixers, the designed transconductance LNA (TLNA) will be explored in the future.

Acknowledgment

The authors would like to thank the National Chip Implementation, National Applied Research Laboratory, Taiwan, for the fabrication of the testing chip.

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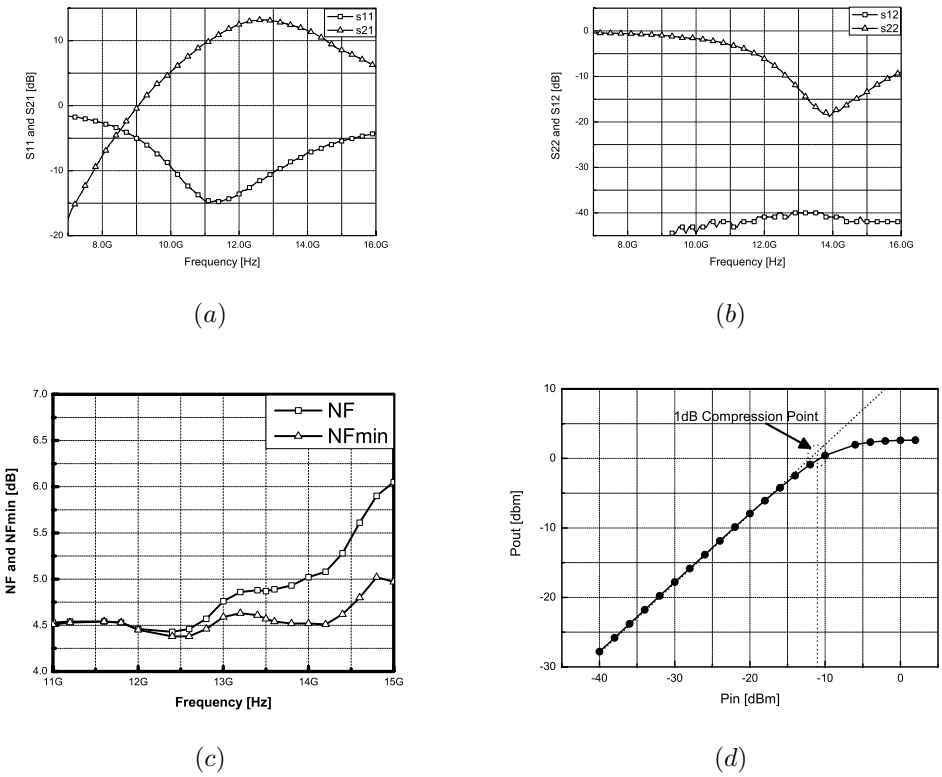

(a) (b) (c) (d)

Fig. 3. LNA measurement results: (a) S_{11} and S_{21}, (b) S_{22} and S_{12}, (c) noise figure NF and minimum noise figure F_{min}, and (d) P_{in} versus P_{out}.

TABLE I

THE MEASURED PERFORMANCE PARAMETERS OF THE FABRICATED LNA AND COMPARISONS WITH OTHER PUBLISHED LNAS.

	This work	***[5]***	***[6]***	***[6]***	***[7]***
Tech.	$0.18\mu m$ $CMOS$	$0.18\mu m$ $CMOS$	$0.18\mu m$ $CMOS$	$0.18\mu m$ $CMOS$	$90nm$ $CMOS$
Topology of Input matching	Capacitive Feedback	Source Degeneration inductor			Microstrip Line
Freq.(GHz)	12.8	14	8	9	20
Gain(dB)	13.2	10.71	13.5	12.2	5.8
NF(dB)	4.57	3.16	3.2	3.7	6.4
IIP3(dBm)	-1*	1.6	-3.2*	-1.3*	5.2
Power(mW)	10	28.6	22.4	19.6	10
Supply (V)	1	1.3	1	1	1.5
S11(dB)	-11	-10	-5.8	-5.4	–
Chip Size (mm^2)	$.746 \times .885$	$.88 \times .77$	–	$1 \times .9$	$.7 \times .8$
FOM	11.6	7.2	3.5	4.2	7.4

*The IIP3 is predicted by input P1dB+10dBm

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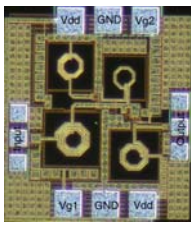

Fig. 4. The chip photograph of the proposed LNA.