An Implementation of Integrable Low Power Techniques for Modern Cell-Based VLSI Designs

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***Abstract*—Recent research has proposed several low-power design techniques for VLSI circuitry in nano-scale CMOS era. However, these techniques always involve custom layout design or novel EDA flows. In this paper essential low power techniques such as voltage separation, body bias and power switch are implemented in existent place and route (P&R) tools. These techniques enable the possibility to integrated low power techniques into standard Cell-Based physical design flow. The result of these research shows a little overhead in design procedure equally area overhead compare with fully custom design flow. The proposed low power design techniques can be cooperated with modern power management system to enable the power reduction in targeting circuitry with small implementation overheads.**

I. INTRODUCTION

Power dissipation has become an important design concern in modern VLSI design. High power dissipation incurs expensive package and significant cooling cost. At the same time, the power-aware devices such as laptops, mobile phones, and handhelds devices, have limited battery capacity. Therefore, make the reduction and control of power dissipation in high performance digital designs almost a necessity. However, to maintain performance at the lower supply voltage, the transistor threshold voltage (V_T) must decrease as well. Because of the exponential relationship between V_T and transistor leakage current, this leakage power is becoming a larger fraction of total power consumption, approaching 40% of the total in today's chip power dissipation [1]. Therefore, how to control the leakage power in modern VLSI design is becoming an important topic.

These leakage control methods can be categorized into two main categories: static techniques and dynamic techniques [2]. In order to obtain flexible leakage control ability, the dynamic techniques have been adopted. Dynamic techniques allow the dynamic control of certain functional blocks of the design during functional operation. Power switch, a popular dynamic technique, is commonly used to disconnect power supply of functional block. This is achieved by connecting a transistor in series with the power supply of the block [3]. In practice, a network of power switch may be necessary to efficiently control and reduce leakage power. Another dynamic technique, body bias, needs dynamically changing the body bias applied to the block [4]. During active mode, forward body bias (FBB) is applied to increase the operating frequency. Alternately, reverse body bias (RBB) can be applied during idle mode for further leakage savings. This body bias technique can be combined with a power switch to provide even further leakage power savings.

However, the majority of low power design circuits are implemented with Fully-Custom design. In order to automate design phase and satisfy the demand of Time-To-Market requirement, integrating low power techniques into Cell-Based physical design flow is essential. In order to apply the benefits offered by low leakage techniques into Cell-Based design, some physical design issues must take into considerations. Therefore, the general physical design flow must be modified for the integrating low power techniques into physical design.

In this paper, a low power physical design methodology is presented. By using this low power design methodology, a Cell-Based design circuit with low power techniques features is available. Our goal is to create a regular physical design flow utilizing existent EDA tool. The rest of the paper is organized as follows: The low power physical design methodology is presented in Section II. The implementation results are presented in Section III. Finally, the conclusion is discussed in Section IV.

II. LOW POWER PHYSICAL DESIGN METHODOLOGY

A. Preliminary and Test Vehicle

During entire implementation process, TSMC 0.18um CMOS technology and Artisan's SAGE-X standard cell library is adopted. The APR EDA tool for physical design is Synopsys Astro. The tool for physical verification is Cadence Virtuoso-XL. The benchmark circuit for proposed physical design flow is a Single-Instruction-Multiple-Data Multiply-and-Accumulate Unit (SIMD MAC).

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B. *Voltage Separation*

In order to provide block-level power optimization ability, the Voltage Separation technique is introduced first. The concept of Voltage Separation technique is to partition circuit into several groups and draw power source via individual power grid [5]. Therefore, each group can be powered off completely via switch, eliminating both active and standby components power. However, some peripheral circuit, such as level converter, may be used for translating voltage level among mixed voltage system. In our paper, we assume the level converter is added when Logic Synthesis.

Compare with general physical design flow, the difference parts of physical design flow for Voltage Separation is floorplanning. According to the demand of system, designer has to partition design circuit into several groups which are supplied with difference voltage level, respectively. At the same time, the core area will be increase result of individual voltage grid and dead space from floorplanning of groups. In order to increase the design flexibility and decrease the area penalty caused by Voltage Separation, each group can adjust island's aspect and core utilization by some design parameters tuning. After groups partition, the Floorplanning of groups has to implement. According to the pre-plan of power grid, designer can place groups to any region in the core individually.

C. *Body Bias*

Body bias is a dynamic technique that has been used to for leakage power reduction by dynamically changing the body bias applied to the circuit block. In general, the forward body bias (FBB) is applied to increases the operating frequency when active mode. When block enter the idle mode, the forward bias is withdrawn, reducing the leakage. In addition, reverse body bias (RBB) can be applied during idle mode for advanced leakage savings. Compare with power switch, the body bias can provide leakage reduction without any performance degradation [1]. In following section, there are two body bias design method based on different type of standard cells. We will introduce them respectively.

1) *Body Bias with Dual Supply Cell*

Fig.1 shows the layout outline of general and dual supply cell. The body and source terminals of MOSFET in general cell are tied together. In order to realize body bias, the voltage level of body terminal has to change dynamically according to system requirement. Therefore, separating body from source is necessary. As shown in Fig.1 (b), the dual supply cell has additional power and ground ports, VDDB and VSSB. Therefore, voltage level of body and source terminal can be assigned to differential voltage value.

Besides isolated ports, the remaining part of dual supply cell is almost the same with general cell. However, the extra gap existed in the dual supply cell will result in area overhead. Therefore, the implementing body bias with dual supply cell needs larger area compared with general cell.

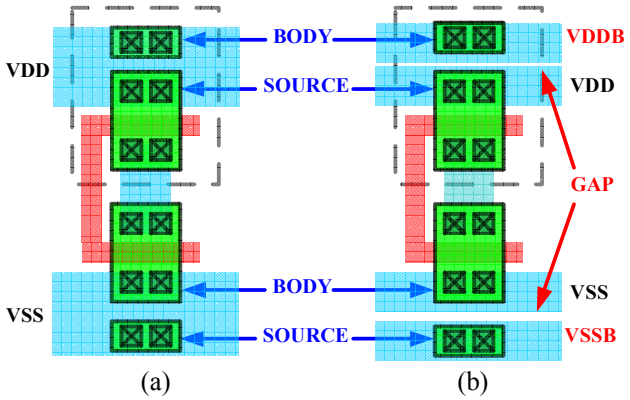

Figure 1. The layout outline for (a) general cell and (b) dual supply cell.

2) *Body Bias with General Cell*

The body bias design principle with general cell is shown in Fig.2. With simple pattern modification, the body bias can be integrated into Cell-Based physical design flow. The key points of design are respectively removing body from power grid, adding extra power straps for body terminal voltage controlling and sticking body terminal on power straps.

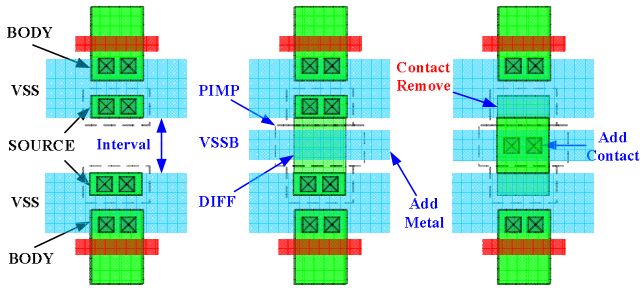

Figure 2. The design concept of body bias with general cell. In this figure the body of NMOS is biasing.

In order to create extra metal liens for VSSB, the standard cells are placed at appropriate intervals, which can be done by using the conventional P&R EDA tool with appropriate parameters. Next, PIMP and DIFF patterns are added to the interval between cells. The patterns overlap to the cell can be changed by design parameter. According to characteristic of cells, this method can adjust the degree of overlap to fit the layout style of cell. Finally, the removing contact located on VSS line and adding contact on the VSSB line is implemented. Besides the contact modification on metal lines, other design steps can be implemented with existent EDA tool command. It makes the design phased more efficiently and avoids error which may create by hand.

3) *Double Deep N-well Isolation Structure*

The deep N-well (DNW) can be respectively added to each group for decreasing substrate noise coupling [6]. The DNW isolates the P-well, which is the noise source and P-substrate with each other. The characteristic of device is not affected by DNW impact because DNW implant peak is deep enough, about 2 um. Therefore, if there are two or more

than two groups in the design and body bias techniques is applied on NMOS, the Double Deep N-well isolation structure can be used to separate p-well layer of each group and diminish the coupling noise.

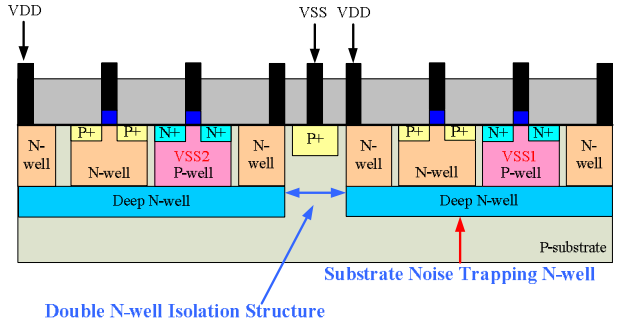

Figure 3. Double deep N-well isolation structure.

D. Power Switch

Power switch is achieved by connecting a transistor in series with the power supply. The connecting transistor between power supply and virtual power lines can be accurately modeled as linear resistors. For a turned-on NMOS transistor sized large enough to ensure performance for requirement, the virtual ground voltage will be close to actual ground. Therefore, the power switch sizing is a key design parameter that affects the performance of circuit. If sized too large, the silicon area would be wasted and switching energy overhead between idle and active modes would be increased. If sized too small, then the circuit would be too slow because of increased resistance to ground. Besides incurring a little performance penalty, power switch is a very attractive technique for leakage suppression.

In order to insert power switch into Cell-Based design without modifying core design, the appropriate arrangement for power switch is important. Fig.4 shows the power connection between power grid and standard cell. In our implementation, the power switch is inserted below the power delivery grid between metal-1 and metal-2. The power switches are distributed throughout the power ring in two columns in order to avoid any current crowding issues. The power switches are designed as large as possible to avoid the sizing impact on performance.

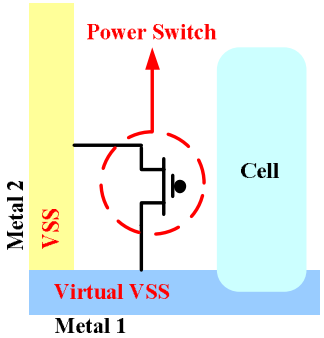

Figure 4. The power connection between power switch and cell.

III. IMPLEMENTATION RESULTS

During integrating low power techniques into Cell-Based physical design flow, some extra step and pattern are used to satisfy the demand of design. Therefore, it often incurs area overheads. In the following section, we discuss the area penalty and some effect during design implementation.

A. Floorplanning Issue of Voltage Separation

The use of Voltage Separation permits operating different groups of the design at different voltage level in order to optimize the power dissipation. But the Voltage Separation definitely makes the design process even more complicated with respect to static timing, power routing and floorplanning. The cells belongs to each island are only placed in the limited area. The limited placed area restricts the flexibility of cell moving space which may be used to resolve wiring congestion problem.

Besides, the groups need to be placed close to the power pads in order to minimize the power routing complexity and the IR drop. Since each group requires its own power grid, it may have additional area overhead due to potential dead spaces if two or more power rings can not packed perfectly. However, core form of each group can be determined by some design parameter. Therefore, the dead space can be control via better-choose core form and floorplanning. The area overhead is not a critical issue if the power ring can not packed imperfectly.

B. Area Penalty of Body Bias

The layout type of dual supply cell library is proposed for body bias. Because each rail of dual supply cell sinks less current than rail of the general cell that is powered from single VDD (VSS). Thus, the width of power rails can be shrunk. Meanwhile, VDDB of the dual supply cell is further scaled because current magnitude of body is less than source. The cell height of general cell, which is provided by Artisan for TSMC 0.18um process, is 5.84um. The cell height of dual supply cell is 6.3 um, which accounts to 7.9% area overhand compared to general cell. For the body bias implementation with dual supply cell, the advantage is routing can be directly performed after placement. The existed APR tool can be used to automate the placement and routing.

During the body bias implementation with general cell, an interval must be left between cells for strap and well pattern insertion. The width of interval can be controlled by design parameter. Therefore, the area overhead depends on how large the interval area occupied between cells. According to SIMD MAC experiment result, it accounts to 17% area overhead compared with SIMD MAC without applying body bias. The layout diagram for body bias with general cell is show in Fig.5. The white block shows straps are inserted into the intervals betweens cells.

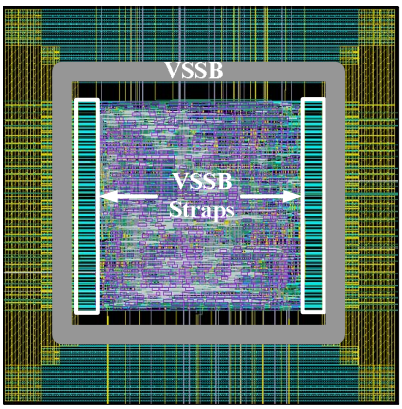

Figure 5. The layout diagram for body bias with general cell.

C. *Power Switch Placement*

If designer want to add power switch into the design circuit, the architecture of power grid and placement of power switch have to take into consideration. In our implementation, the NMOS power switches are inserted into the power delivery grid between the metal-1 and metal-2. The power switches are distributed through the layout in two columns in order to reduce any current crowding issues in the power delivery grid. At the same time, the power switch is not implemented by APR EDA tool. So the cut-off signal routing which drives the gate of the power switches has to realize by designer. Because the power switches are placed below the power grid, the area overhead created by power switches is negligible. The layout diagram of power switches placement is shown in the Fig.6.

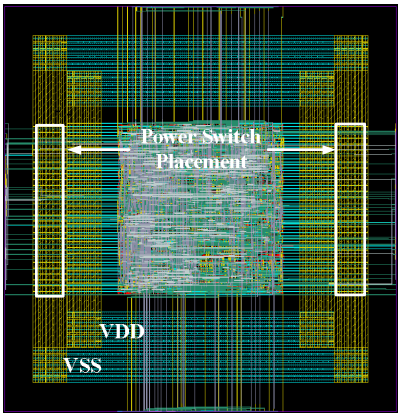

Figure 6. The layout diagram of power switches placement.

D. *Summary of Implementation*

Table I shows the summary of the low power techniques implementation in this paper. Because of dual supply cell is not available; the area overhead indicates the star mark and the meaning of the number represent the increase percentage per cell which is compared with general cell. Besides the method using dual supply cell for body bias, other design methods need extra pattern to realize these low power techniques. The semi-automation represents that some design steps have to be realized by designer. The area overhead of combining three low power techniques is estimated via area penalty of individual low power technique, which accounts about 19.1%.

TABLE I. SUMMARY OF LOW POWER TECHNIQUES IMPLEMENTATION.

Technique type		Area overhead	Extra pattern	Implementation style
Voltage Separation		--	DNW	Semi-automation
Body Bias	Dual Supply cell	*7.9%	none	Fully-automation
	General Cell	17.4 %	Contact / DIFF	Semi-automation
Power Switch		--	none	Semi-automation
Combine 3 Techniques		*19.1%	DNW/Contact/DIFF	Semi-automation

IV. CONCLUSION

To meet the power requirement of advanced VLSI design, several simple yet effective physical design flows using existent commercial APR EDA tool have been presented. By integrating low power techniques into physical design flow. A design circuit with low power technique feature is available. Therefore, this thesis provides a basic design flow to realize low power techniques via Cell-Based design method. Although some simple low power techniques are realized, several enhancements, such as partition islands, sizing of power switch and physical design considerations, still need to be improved on the EDA tool. Further, creating an industry-wide design flow with robust capability is essential. These include functional partitioning, synthesis, timing analysis, power analysis, test, simulation and physical design.

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