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Characterization of the Chemical-Mechanical Polishing Process Based on Nanoindentation Measurement of Dielectric Films

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ABSTRACT

To better understand variations in the rate at which material is removed from a wafer during chemical-mechanical polishing (CMP), knowledge of the mechanical properties of the wafer surface is required. The nanoscale mechanical properties of undoped dielectric films were investigated using the nanoindentation technique. Crack resistance examined from the loading curve suggested that precursor cracks for SiH_4-atmospheric pressure chemical deposition films with a tensile stress, as compared with other dielectric films with compressive stresses, appeared in the earlier stage of indentation. The hardness of dielectric films determined from the unloading curve could be considerably dependent on the film's preparation methods. Correlation between the Si-O bond densities and hardness were also studied. Experimental results showed that there was a linear relationship between the surface hardness and the removal rates of the undoped dielectric films under a well-controlled CMP process.

Introduction

As device dimensions are scaled down to subhalf-micron levels, local and global planarization assumes increasing importance for device fabrication and interconnection.[1-6] If planarization is not performed, metal circuit lines become coated with an intermetal insulative layer such that the upper surface of the interlayer dielectric comes to exhibit nonplanar "steps." These step variations are undesirable for several reasons: they limited the depth of focus (<1 μm) of the high numerical aperture lenses used in the latest generation of wafer steppers,[1,2] and metal can thin over steep topographies.[1] Therefore, to decrease these effects, it is necessary to planarize the top surface of the deposited dielectric. Processes used for surface smoothing include spin-on glasses, resists, or other polymers with etchback, and new dielectric-deposition techniques such as tetraethylorthosilicate (TEOS)-ozone at (sub)atmospheric pressures, electron-cyclotron resonance chemical vapor deposition (CVD), and deposition-etch-deposition sequences. However, spin-on coatings and etchback only planarize over distances in the tens-of-microns range, and global planarization cannot presently be achieved with any of the CVD technologies.[1,3] Today, only chemical-mechanical polishing (CMP) technology has the ability to planarize dielectrics both locally and globally from the micron range up to 20 mm across the step-image field.

CMP has been a part of silicon technology for many years, since it was introduced as a necessary step for obtaining a smooth damage-free silicon wafer surface.[7] However, it was difficult to transfer directly CMP-process results from development laboratories to manufacturing sites. The major drawbacks for adopting CMP in manufacturing are lack of knowledge about process variations related to the material properties of polished film, slurry distribution, slurry chemistry, physical characterization of the pad and good end-point technology to avoid over or under polishing.[1] Because the material removal rate varies on dielectric thin films that are polished, there is a need for an analysis of the surface mechanical properties of these films. However, so far, information about the surface mechanical properties of the dielectric films used for microelectronics is still lacking.

The simplest and fastest way to measure the mechanical properties of a thin film on a substrate is to deform it in a very shallow subsurface region. Because indentation testing with a sharp indenter is one convenient way to accomplish this, nanoindentation has become one of the most widely used techniques for measuring the mechanical properties of thin films. Other reasons for the acceptance of nanoindentation stem from the ease with which a wide variety of mechanical properties can be measured without removing the film from its substrate, and the ability to probe a surface at numerous points and spatially map its mechanical properties.[8]

Nanoindentation systems measure mechanical properties in much the same way as conventional mechanical testing systems; properties can be obtained from simple measurements of load, displacement, and time. The load-displacement data derived are very similar to and contain much the same information as those obtained from a conventional compression test. However, the classic hardness measurement method is often insufficient for estimating elastic modulus and plastic properties in near-surface regions, where the mass volume available for experimental investigation is very small (*e.g.,* materials with surfaces modified by energetic ion implantation, small volume crystals for microelectronics, etc.).[9] The reason for the difficulty is that in order to affirm that the substrate does not influence the measurement, the size of the contact impression must be kept small relative to the film thickness. The hardness impressions for films with micron dimensions must be so small that their areas cannot be accurately determined due to the limitations on resolution and efficiency of the optical system attached to the hardness tester.[9]

These difficulties are overcome in nanoindentation testing by obtaining the properties from analyses of the in-

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Table I. Process conditions and film characterization for various dielectric films.

Dielectric film	System	Gas used	Deposition temperature (°C)	Film thickness (μm)	Refractive index	Residual stress (MPa)	Hardness (GPa)
Thermal oxide	ASM/LB45	H_2, O_2	980	0.62	1.46	−22.8	35.9
SRO-PECVD	Novellus	SiH_4, N_2, N_2O	400	1.10	1.53	−28.5	32.2
SiH_4-APCVD	WJ999	SiH_4, O_2	400	1.10	1.46	+150	27.2
TEOS-PECVD	AMT/P5000	TEOS, O_2	390	0.99	1.46	−112	29.0
SiH_4-PECVD	AMT/P5000	SiH_4, O_2	400	1.03	1.46	−46.9	24.2

dentation load-displacement data, thus, no imaging is required. Nanoindentation loads are typically applied through a coil and magnet assembly, in which the load is determined from the current flowing to the coil, or by the use of piezoelectric drives, for which a load cell is needed in the load train. Displacement is almost always measured by capacitive sensors. Load and displacement resolutions of better than 0.01 μN and 0.1 nm have been achieved in some of the better instruments. Tests are most commonly conducted at constant rates of load or displacement, creep tests (*i.e.,* constant load), stress relaxation tests (*i.e.,* constant displacement), and a host of others are possible.[8]

Some recent studies include research into the properties of ion-implanted layers on metals such as nickel and gold,[10] direct observations and analyses of the propagation of indentation cracks in glasses and ceramics,[11] studies of the electrical resistance of metallic contacts on semiconductors during indentation involving phase transformation,[12] observation of structural changes in nanoindented sapphire by means of high resolution electron microscopy,[13] determination of the Young's modulus, hardness of ion-beam-sputtered TiN_x [14] and ultrahigh strength carbon nitride[15] thin films, and observations of the fracture patterns within and around the indentations in carbide-on-silicon systems.[16]

Dielectric thin-film polishing has much in common with traditional glass polishing. From a thermodynamic point of view, energy is applied to the system both mechanically and chemically. This results in deformation, chemical change, and heat generation. The slurry particles add a chemical "tooth" to the polishing process, and the bond strength between the slurry particle and wafer surface determines the effective kinetic coefficient of friction during polishing.[2] This indicates that the strength and hardness of the polished films have a great influence on the wear mechanism in the CMP process. The purpose of the present study is to investigate the mechanical properties of the dielectric films by means of nanoindentation measurement and to explore quantitatively the relationships between hardness of dielectric films and removal rate. The hardness of undoped dielectric films is closely related to their microstructure, which is in turn significantly dependent on the film's fabrication techniques. Hence, Fourier transform infrared (FTIR) absorption spectroscopy was used to characterize the oxide films prepared by different methods. The relation between hardness and the Si-O bond density of undoped oxide films has also been determined.

Experimental

Sample preparation and film characterization.—All test samples in the present study were prepared on p-type (100), 150 mm silicon wafers. Process conditions are reported in Table I. Thermally grown films of silicon dioxide were accomplished by wet oxidation (ASM/LB45 furnace system), in which the silicon was exposed to the oxidizing ambient H_2, O_2 at 980°C. Films of atmospheric pressure chemical vapor deposition (APCVD) and plasma-enhanced chemical vapor deposition (PECVD) oxide were deposited by reacting SiH_4 and O_2 at a temperature of 400°C. SiH_4-APCVD oxides were deposited in the WJ999 system, SiH_4-PECVD oxide films by the AMT/P5000 system. TEOS and O_2 at 390°C were used as a reactant gas for TEOS-PECVD films; Silicon-rich oxide (SRO-PECVD) films were obtained in ambient SiH_4, N_2, and N_2O with Novellus reactor.

The refractive index of the dielectric films, as measured by ellipsometer, is given in Table I. Previous work[17] reported that the deviation of the CVD silicon dioxide film's refractive index, n, from that of the thermal SiO_2 value of 1.46 is often used as an indicator of film quality. A value of n greater than 1.46 indicates a silicon-rich film, while smaller values indicate low-density, porous films. Most major undoped silica films have refractive indices in the range of 1.45 to 1.47. SRO-PECVD film, with an index of 1.52, is an exception, and is the only silicon-rich film.[17]

Residual stress measurements of dielectric films were performed using the FSM 8800 system and the stress values are listed in Table I. The residual stress of undoped PECVD films and thermal oxide films is compressive, while the undoped SiH_4-APCVD is tensile. All specimens were deposited to a thickness of about 1 μm, except thermal oxide, which was 0.62 μm.

Polisher setup.—CMP was carried out on a Westech Model 372M wafer polisher using an IC 1000/Suba IV pad. During the polishing experiment, the wafer was mounted on a template assembly for a single 6 in. diam wafer. The Teflon retaining ring is recessed from the wafer surface by 7 mils. Pressure at the wafer slurry pad interface is controlled via an overhead mechanism which allows pressure to be applied to the wafer holder. Both the carrier and table (with the IC 1000/Suba VI pad fixed to the table) were rotated independently. The thickness of dielectric film was measured with Nanometrics 2100XP by tracing the surface from the location at a distance of 10 mm away from the edge toward wafer center, and was averaged over nine different locations on the wafer to determine the polish rate. The cross-wafer nonuniformity of the dielectric polish rate was less than 10%. The polish slurry (SC-1 slurry available from Rippey Corporation) was a suspension of fumed silica dispersed in aqueous potassium hydroxide.

Pad conditioning.—New polish pads were used for each experiment; however, maintaining a stable removal rate and uniformity over time is still an issue of polishing because the pad surface tends to glaze with use.[2] Pad conditioning techniques were used to refurbish the surface to maintain the removal rate without sacrificing the uniformity. In our experiment, the pad conditioning with Rotating Pad Conditioner II was performed between each wafer to clean the pad of old slurry and lift the pad fibers for further processing. Without this procedure, the polish rate decreased substantially after only several wafers.

Nanoindentation test.—Nanoindentation experiments on the undoped dielectric thin films were performed using a commercially available ultralow load indentation system, the NANOTEST 500 from Micro Materials, Ltd., UK. This highly sensitive mechanical properties testing instrument is capable of sensing both load and displacement continuously as indents are being made in a sample. The following loading/unloading sequence was used in this work: (*i*) Gentle, elastic contact with the surface to preclude initial surface damage. (*ii*) Acquisition of load *vs.* depth data at the initial load, as the load was increased, reversed, and decreased back to zero, then at the final load. Data may also be collected during a dwell period at maximum load. (*iii*) Identification of the starting point of the load ramp and hence the zero of depth. (*iv*) Extraction of the hysteresis curve. (*v*) Correction for elastic recovery to determine the plastic depth, and then the hardness could be calculated. The physical processes involved are shown schematically in Fig. 1.[8] As the indenter is first driven into the film, both

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elastic and plastic deformation occur. The plastic deformation results in the formation of a permanent hardness impression that conforms to the shape of the indenter to some contact depth, h_c. The elastic processes result in an additional component of displacement, one manifestation being that the surface displaces downward at the edge of the contact by an amount, h_s. The key to the analysis procedure is that as the indenter is withdrawn, the elastic displacements are recovered, and an analysis of the elastic unloading data can then be used to relate experimentally measured quantities to the projected contact area and an effective elastic modulus.[18]

Samples were mounted on a fixture which permits shifting them about the vertical axis to any desired position. All tests were carried out at ambient temperature (22.7°C) and humidity with the instrument inside a thermally lagged enclosure in an air-conditioned room. The resultant thermal was better than 0.1°C over periods of several hours. All tests were performed at a nominal constant loading rate of 1.18 mN/s of the maximum set displacement. For each sample, ten separated indents, spaced 15 μm from each other, were made on the investigated surface.

The hardness, H, is given by

$$H = L_{max}/A_f \quad [1]$$

where L_{max} is the load corresponding to the total displacement, A_f is the projected contact area determinated by the geometry of the indenter. Pharr and Oliver[8] proposed that the area function of a Berkovich indenter with a perfect triangular pyramid geometry is given by

$$A_f = 24.5d^2 \quad [2]$$

where d is the distance from the tip of the indenter, but for real indenters, A_f must be corrected due to rounding at the tip. The projected contact area of a Berkovich indenter we used is proposed by the manufacture[19]

$$A_f = 23.897d^2 \quad [3]$$

Fourier transform infrared (FTIR) analysis.—Room temperature IR transmission measurements were performed in the wave number range from 4400 to 400 cm^{-1} using a Biorad QS300 FTIR spectrometer with a CsI beam splitter. 256 scans were performed for every sample and the obtained spectra were averaged to increase the signal-to-noise ratio. Instrumental resolution was 4 cm^{-1}. A prime, unprocessed substrate was used as the background to ensure that the spectra obtained was solely due to SiO_2 films.

Results

Nanoindentation measurement of undoped dielectric films.—The nanoindentation technique is a powerful tool for examining both the deformation response and deformation mechanism transition exhibited by ceramic materials in response to fine-scale surface contacts.[13] The remarkable change of mechanical properties due to different film deposition processes is best illustrated by examples like Fig. 2. The same maximal displacement (300 nm) was applied in all cases, but the final loads for harder coatings were larger than those for softer coatings.

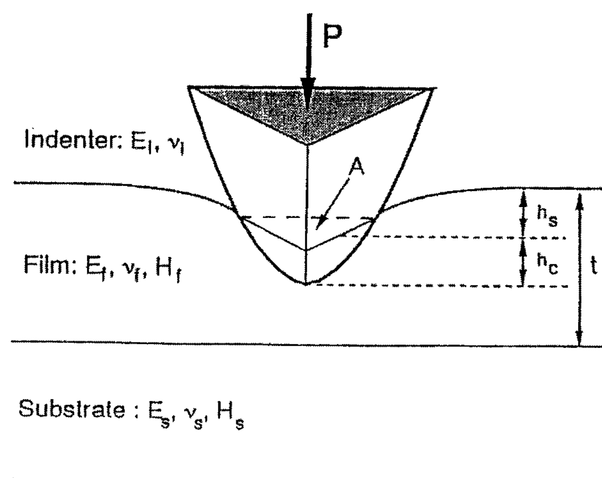

Fig. 1. The physical processes involved in the indentation of a thin film on a substrate.[8]

Crack resistance estimation from the loading curve.—For the brittle coatings on silicon, the deformation of the coating often has a large elastic component. Indeed, for indenter displacements up to about 50 nm the deformation can be purely elastic and therefore totally reversible.[16] In Fig. 2 the loading curve exhibits small steps and plateaus. These are not thought to be related to difference in elastic modulus between the coating and the substrate as they are too sudden. The most likely interpretation of these events is that they represent the propagation of various types of cracks, either through the coating ("through-thickness cracks," caused by flexure of the coating) or along the coating-substrate interface (caused by shear stresses across the interface), away from the immediate contact zone where the coating is flexed into conformity with the surface of the indenter.[16]

The precursor cracks for SiH_4-APCVD films, as compared with other dielectric films, appeared at an earlier stage of indentation, and this event demonstrated that a discontinuous increase in penetration depth clearly occurred as the plastic flow was initiated. In order to interpret observations in crack initiation of studied dielectric films, a crack resistance (CR) proposed by A. K. Sinha *et al.*[19] was used as a criteria. A dielectric film with a lower CR value tends to crack at lower applied stress. The CR is defined as[19]

$$CR = \frac{\rho}{\rho_o}\sigma_u - \sigma_m \quad [4]$$

where ρ and ρ_o are structurely "imperfect" and "perfect" dielectric film density, respectively, σ_u is the ultimate tensile stress of a structurely "perfect" dielectric film, and σ_m is the measured residual stress of the studied film.

Calculation of relative CR of various dielectric films could be made for SiO_2. Since the density of various SiO_2 films are all around 2.2 g/cm^3 which is assumed as a reference density value for amorphous SiO_2, the CR of SiO_2 films is determined solely by the residual stress term. The residual compression stress suppresses cracks initiating during the loading cycle[11] and vice versa. Therefore the occurrence of cracks was seen during low-load indentation as SiH_4-APCVD film (Fig. 2e) had a residual tensile stress. As shown in Fig. 2a-d, the SiO_2 films with compressive residual stress do have a higher load at the initiation of cracks than a film with tensile stress.

Hardness calculation from the unloading curve.—The hardness values were determined from the slopes of the first 20% of the unloading sections. It was clearly observed from Table I that the hardness of thermal oxide film was higher than that of the CVD films. This demonstrates that the hardness of dielectric films is closely related to the film's preparation methods. Although SiO_2 films, whether grown by the oxidation of silicon or deposited by CVD processes, have an amorphous structure with a random network of polyhedral,[17] CVD silicon dioxide, depending on the deposition conditions, may have a lower density and slightly different stoichiometry from thermal oxide, causing changes in mechanical and electrical films properties (such as hardness, stress index of refraction, etch rate, dielectric constant, and high electric-field breakdown strength).[17] The direct parameter affecting those properties to be considered is then the Si-O bond density (N_{Si-O}), as discussed in the following section.

Relationship between hardness and Si-O bond density of undoped oxide films.—In order to correlate the studied undoped SiO_2 films' mechanical properties to their microstructures, FTIR was used to analyze oxide films prepared by different methods, including thermal oxidation, SiH_4-

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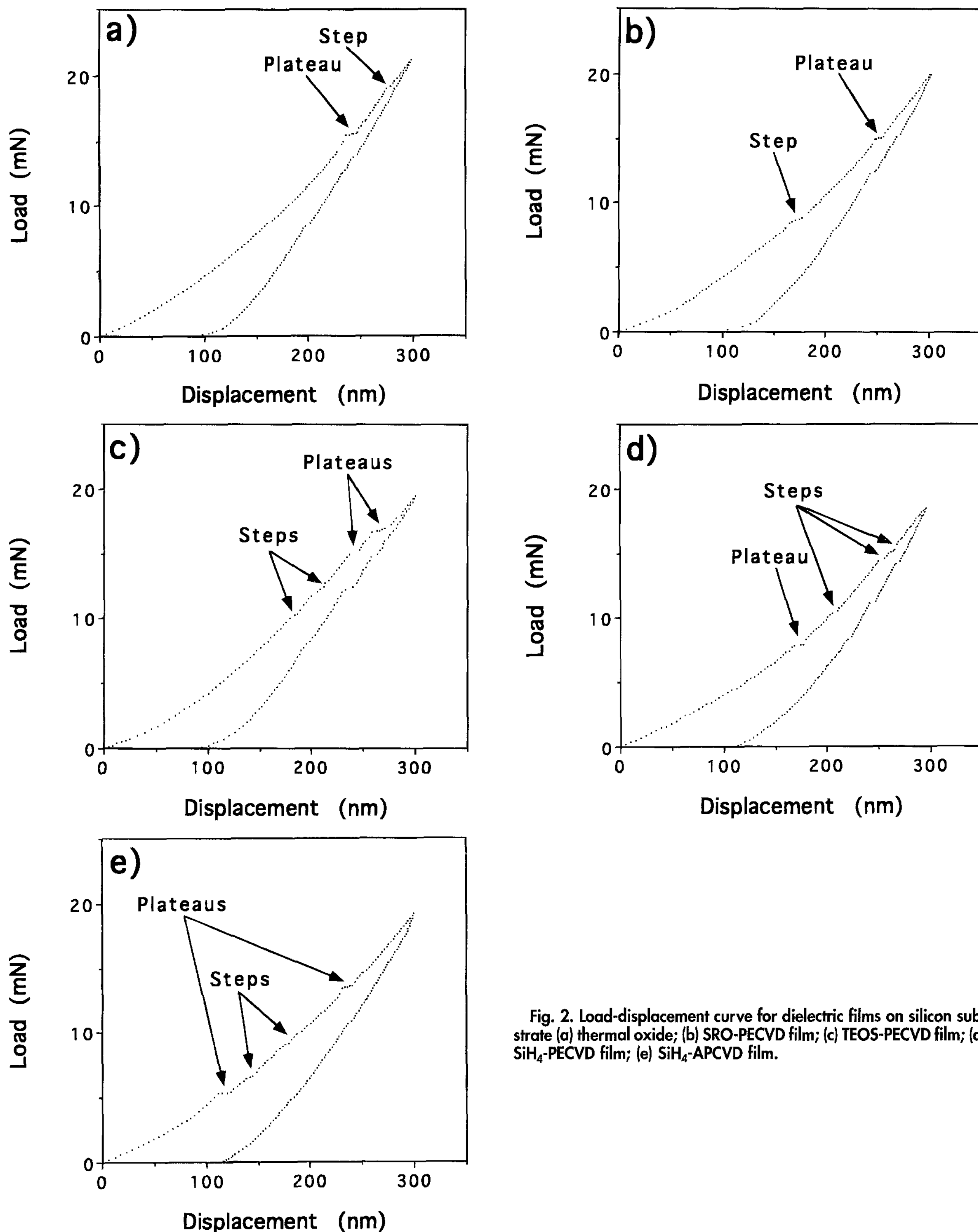

Fig. 2. Load-displacement curve for dielectric films on silicon substrate (a) thermal oxide; (b) SRO-PECVD film; (c) TEOS-PECVD film; (d) SiH_4-PECVD film; (e) SiH_4-APCVD film.

PECVD, TEOS-PECVD, and SiH_4-APCVD. Figure 3 is a stacked plot of the transmission spectra obtained for the various undoped SiO_2 films. The bands due to the asymmetric Si-O-Si and Si-OH stretching vibration are normally in the range 1100 to 1000 cm^{-1} and 3200 to 3700 cm^{-1}, respectively.[20] The peak position of these two bands were influenced by bonding environment, stoichiometry, density and porosity of the SiO_x films. The O-H bond stretching in Si-OH structures giving rise to absorption bands at about 3600 cm^{-1} is observed for CVD films, but it is absent in thermal oxide films. On the other hand, the Si-O absorption peak of the thermal oxide film is located at 1091.9 cm^{-1}, while the Si-O absorption peak for TEOS-PECVD and SiH_4-APCVD films appear at lower wave numbers, 1076.6 and 1078.4 cm^{-1}, respectively, and that of SiH_4-PECVD films appears in an even lower wave number, 1059.5 cm^{-1}. Estimates of the density of oxygen bonded to silicon have been obtained from the integrated absorbencies of the Si-O stretching modes. According to Ref. 22 and 23, the concentration values were estimated as follows

$$N_{\text{Si-O}} = \frac{2.303Bs}{<v>t} \int A(v)dv \quad [5]$$

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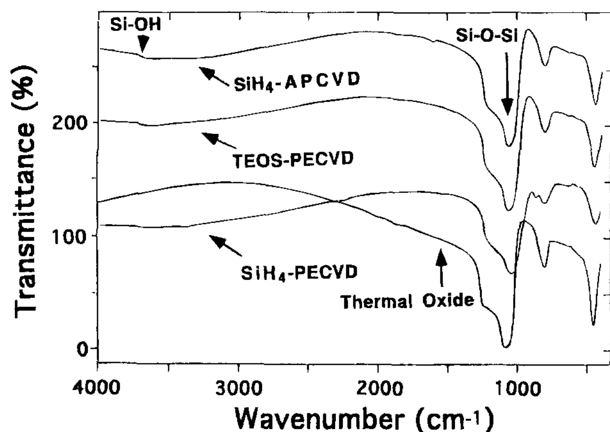

Fig. 3. Stacked plot of the transmission spectra for thermal oxide, SiH_4-PECVD, TEOS-PECVD, and SiH_4-APCVD films.

where N_{Si-O} is the number of Si-O bonds per cubic centimeter, Bs (the inverse cross section) used for Si-O(s) mode is 1.5×10^{19} cm^{-2}, v is the wave number of the incident radiation, <v> is the wave number at which the Si-O stretch is at a maximum, A(v) is the absorbance, and t is the thickness of the films. The N_{Si-O} of PECVD films made from silane is about 2.92×10^{22} bonds/cm^3, and PECVD films obtained from TEOS is about 4.42×10^{22} bonds/cm^3. For thermal oxide and SiH^4-APCVD films, the N_{Si-O} is 8.82×10^{22} and 4.38×10^{22} bonds/cm^3, respectively.

The higher N_{Si-O} value of thermal oxide films compared to CVD films can be explained by the hydrogen incorporation in the CVD films. Indeed, hydrogen atom impurities incorporated into CVD films form Si-OH hydrogenated bonds, as evidenced by FTIR analysis, and consequently reduce the total Si-O bond density. In addition to the hydrogen incorporation, the presence of defects, microvoids, clustering, and dangling bonds could affect the Si-O bond density. Furthermore, Fig. 3 shows changes of the maximum Si-O absorption peak for CVD films. The possible contributor to the shift in the Si-O asymmetric stretching frequency is related to a continuous shift in the Si-O-Si bond angle.[24] The Si-O-Si bond angle is influenced by π bonding interactions between nonbonding oxygen p states and empty Si d states. The Si-O-Si bond angle increases as the average number of oxygen atoms bonded to a given silicon atom is increased, and this contributes to the observed shifts in the frequency of the asymmetry stretching vibration for the CVD SiO_x films.

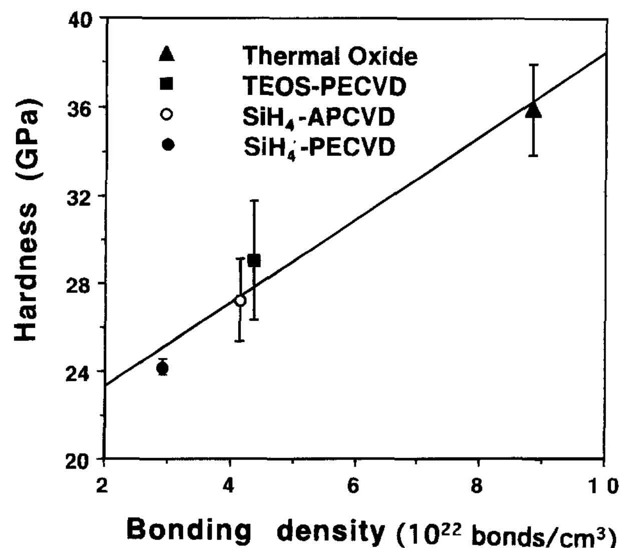

Fig. 4. Linear relationship of the hardness on the Si-O bond density for oxide films.

Figure 4 indicates that the hardness scale up with the Si-O bond density of the various undoped SiO_2 films. By fitting the various undoped SiO_2 film data, the hardness, H, could be expressed as a linear function of the Si-O bond density in the studied range, as follows

$$H = 19.518 + 1.8886 \times N_{Si-O} \quad [6]$$

where H and N_{Si-O} are with units in GPa and 10^{22} bonds/cm^3, respectively. This linear dependence of hardness on bonding density correlates well with the results of the study by El Khakani *et ál.*[24] who found the same trend for a-SiC thin films. An increase of the Si-O bond density will lead to an enhancement of the cross-linkage of Si and O atoms, resulting in a strengthened amorphous SiO_2 material frame and ultimately an improved hardness. It is worth noting that the upper limit of the Si-O bond density is reached in crystalline (ordered form) SiO_2 films, which consequently present the highest hardness. In amorphous SiO_2 films that are structurally disordered, the fundamental cell ("elemental spring") in the amorphous network, from a mechanical viewpoint, is the Si-O bonds. Thus, the hardness of the amorphous network is directly related to the density of the Si-O bonds.

The relation between hardness and removal rate of various dielectric films.—A more complete removal model, proposed by Runnels and Eyman,[6] would be of the form removal rate ($R.R.$) $R.R. = f(\sigma, \tau)$, where σ and τ are the magnitudes of the normal and shear stresses, respectively, on the wafer surface. They considered this model be an analogy to Preston's equation[25]

$$R.R. = \hat{k} \times \sigma \times \tau \quad [7]$$

The development and use of such models requires the determination of stress distributions. Although the complex change in stress distribution is not realized, it can be inferred that both normal and shear stress dominate abrasion of the wafer surface. Because the variation in pad wear conditions and slurry distribution during polishing at different runs causes the abrasive contact change, the removal rate of the dielectric material therefore fluctuates during different runs regardless of whether the same polishing conditions are present. Consequently, in order to eliminate removal rate variation from run to run, the removal rate ratio ($R.R.$ ratio) is defined as

$$R.R.\ \text{ratio} = \frac{\text{Removal rate of dielectric film}}{\text{Removal rate of thermal oxide}}$$

The role of the slurry particles is to add a chemical "tooth" to the polishing process,[2] and the bond strength between the slurry particle and wafer surface will determine the mechanical cutting efficiency of the dielectric film surface. Thus, the strength and hardness of the polished films have a great influence on the wear mechanism in the CMP process. Since the surface mechanical properties of the various dielectric films are different, it is obvious that different dielectric films will exhibit different material removal behavior at the same run. This suggests a potentially important relationship between the removal rate and the surface mechanical properties of the wafer. Figure 5 clearly shows that the polishing rate of the various dielectric films is inversely proportional to its hardness

$$R.R.\ \text{ratio} = 1.94 - 0.94 \times \text{hardness ratio} \quad [8]$$

where

$$\text{Hardness ratio} = \frac{\text{hardness of dielectric film}}{\text{hardness of thermal oxide}}$$

The above relation indicates that high hardness results in a low removal rate for the undoped oxide film. Similar relationships were observed for removal rates *vs.* the microhardness of the leached surface in Izumitani's study.[27] Furthermore, Cook[26] has reviewed the mechanics and chemical process of glass polishing. He proposed that removal rate is inversely proportional to the modulus, E, of

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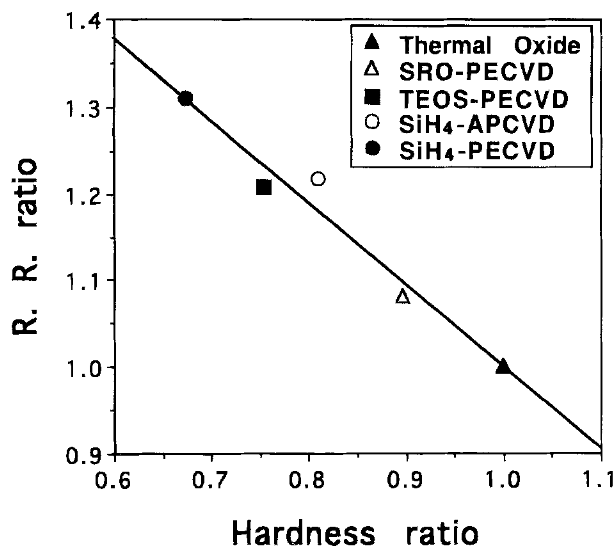

Fig. 5. Linear relationship of the normalized removal rate (R.R.) on the normalized hardness for various dielectric films.

glass and the water in the slurry chemically reacts with silicon dioxide. The reaction proceeds as follows

$$\equiv \text{Si-O-Si} \equiv + H_2O \leftrightarrow 2 \equiv \text{Si-OH}$$

However, the diffusion coefficient of water in silica, which is believed to be the rate-controlling factor of this reaction, is quite low. Hence, the chemical process may not play as much of a role as the surface mechanical factors in determining *CMP* polish rate for undoped oxide films. Modulus as well as hardness could be the determining factor of removal rate in this case. Gilman[27] has shown that the microhardness of structural materials usually increases linearly with an increase in modulus, and the *H/E* ratio is about 1/10 for most covalently bonded materials. These two scenarios together with our experimental findings seem to suggest that the hardness dependence of removal rate is actually justified through the hardness-to-modulus ratio *H/E*. Development of a new model that provides linkage between CMP removal rate and mechanical factor (*e.g.*, *H/E* ratio) is currently underway.[28]

It must be emphasized that this linear relationship is effective only in the well-controlled polishing region. The linear relationship would disappear because glazing of pad surface and inadequate pad conditioning lead to a different degree of decrease in removal rate.

As Eq. 6 and 8 predict, an increase in the number of Si-O bonds (and bond density assuming constant volume) strengthens the oxide film, leading to higher hardness value and hence lower removal rate. Desai *et al.*[29] reported that increasing the O_2 content in the reaction gas mixture led to a significant increase in the removal rate of their SiO_x films deposited by the ECR plasma CVD method. It was assumed that as the O_2 partial pressure in the chamber was increased, the reaction, $2\ O_2 + SiH_4 \rightarrow SiO_2 + 2H_2O$, was favored. The presence of excess O_2 would result in the formation of H_2O. Consequently, it was possible that the H_2O formed during the deposition process tended to be incorporated in the film as H_2O, Si-OH, or Si-H resulting in the decrease of the Si-O bonding density and the increase in the removal rate of their SiO_x films.

Conclusions

The nanoindentation technique is a powerful tool for examining the deformation exhibited by various thin-film materials in response to fine-scale surface contacts. The surface mechanical properties of the undoped dielectric films presented here were determined by nanoindentation. Crack resistance of the various dielectric films were examined from the loading curve. Experimental results show that crack initiation for SiH_4-APCVD films with a tensile stress, as compared with other dielectric films with compressive stresses, occurs during the low-load indentation. The hardness of dielectric films was determined from the unloading section. It is proposed that the CVD oxide films with a more open structure would have lower hardness. Moreover, FTIR microstructure analysis showed that the estimated Si-O bond densities of the undoped oxide films prepared by different methods exhibited a linear variation with the film hardness. The different material removal behavior could be attributed to the varied surface mechanical properties of the undoped films. The CMP removal rate for the various SiO_2 films was found to exhibit a linear dependence on their hardness. A simple perspective which relates removal rate to the mechanical factor *H/E* is proposed to account for this observation. Based on this perspective, it is suggested that a linear relationship is reasonable between the surface hardness and the removal rate of the undoped dielectric films in the well-controlled CMP process. This linear relationship may disappear due to pad glazing and inadequate pad conditioning which lead to a different degree of decrease in removal rate.

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Adsorption Species of Transition Metal Ions on Silicon Wafer in SC-1 Solution

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ABSTRACT

Adsorption of transition metal ions such as Fe(III), Ni(II), and Zn(II) on silicon wafers in ammoniac hydrogen peroxide solution (SC-1 solution) has been studied. It was found by comparing the experimental results with the equilibrium calculations that the main adsorption species is the dissolved neutral hydroxide complex. This was supported by the calculated free energy change of adsorption of hydroxide complexes.

Introduction

It is well known that surface contamination of silicon wafers, from metal ions and particles, deteriorates electrical properties of large scale integrated circuit (LSI) products. In order to reduce such contamination introduced from the environment and equipment, many kinds of cleaning solutions have been developed and used. SC-1 solution (29% NH_4OH:31% H_2O_2:H_2O = 1:1:5 volume ratio)[1] is one of the widely used cleaning solutions in semiconductor manufacturing. It offers very high particle removability relative to other cleaning solutions like SC-2 (35% HCl:31% H_2O_2:H_2O = 1:1:5 volume ratio) and DHF (50% HF:H_2O = 1:99 volume ratio).[1] At the same time, however, surface metal contamination is caused by some metal impurities in the solution.[2] Metal impurities, especially transition metals, cause electrical deterioration such as gate oxide breakdown.[3] Some improvements such as the addition of chelating agents[4] have been made to reduce the metal ion adsorption on a silicon wafer surface. There have also been several efforts to explain the metal adsorption mechanisms. Ryuta *et al.* investigated the kinetics of metal ion adsorption and estimated adsorption and desorption coefficients for some transition metals.[5] But they did not mention the adsorption species. Hiratsuka *et al.* investigated metal ion adsorption as a function of pH and proposed that the adsorption species of Al is the hydroxide complexes.[6] But they did not discuss the adsorption species of transition metals. To clarify the adsorption species of transition metal ions in SC-1 solution is of importance for the understanding of the cleaning mechanism and the development of new cleaning solutions.

When a silicon wafer is immersed in an SC-1 solution, the wafer is etched continuously. Though the etching seems to affect the adsorption behavior of metal ions as well as adsorption equilibria, we do not take it into account in this study. The reason is as follows: although the etching rates of bare and thermally oxidized silicon wafers are quite different, the adsorption behavior of transition metal ions onto the wafers is almost the same.[7] In the present study, we have investigated the adsorption behavior by means of equilibrium analyses. The analyses have been used to assign the adsorption species. Free energy calculation of adsorption has also been performed to know the adsorption species and to support the results of equilibrium analysis. The metal ions examined in this work are Fe(III), Ni(II), and Zn(II) as typical contaminants in semiconductor manufacturing.

Experimental

Sample preparation.—The wafers used in the present work were polished silicon single crystals with a (100) face. Both p- and n-type wafers with a conductivity range of 8 to 12 Ω cm were used. The wafer diameter was 125 mm and the thickness was 500 to 600 μm.

The schematic of the sample preparation process is shown in Fig. 1. The wafers were dipped in an HF-H_2O_2-H_2O cleaning solution[8] for 10 min to remove initial metal contamination. Then they were rinsed in deionized water and dried with a spindrier. They were subsequently immersed in the testing SC-1 solution (29% NH_4OH:31% H_2O_2:H_2O = 1:1:5 volume ratio) for 10 min at 80°C, rinsed in deionized water, and dried with a spindrier. A certain amount of standard solution which contains transition metal ions of Fe(III), Ni (II), or Zn(II) was added to make the contaminant level of the SC-1 solution 10^{-9}-10^{-4} mol l^{-1}. Tetramethylammonium hydroxide was used to raise the pH of the SC-1 solution if necessary.

The following chemicals used in this work were EL grade which contain transition metal impurities below 0.5 ppb: 50% HF, 29% NH_4OH, 31% H_2O_2, 20% tetramethylammonium hydroxide. Metal standard solutions (1000 ppm) for atomic absorption spectrophotometry (AAS) were used for the intentional contamination. The deionized water used in this work contains transition metal impurities below 10 ppt.

All the processes were carried out in a class 100 clean room, and wet chemicals were treated inside a clean draft in the room.

AAS and TXRF measurements.—Surface metal concentration on a standard sample for total reflection x-ray fluorescence spectrometry (TXRF) was assigned by determining the amount of metals on another wafer treated in the same batch, using a graphite furnace (GF) AAS (Perkin-Elmer Z-5100). In the GF-AAS measurement, surface

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