ESD Robustness of 40-V CMOS Devices With/Without Drift Implant

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ABSTRACT

The dependences of device structures and layout parameters on ESD robustness in a 40-V CMOS process have been investigated in silicon chips. From the experimental results, the high-voltage (HV) MOSFETs without drift implant in the drain region have better TLP-measured It2 and ESD robustness than those with drift implant in the drain region. Furthermore, the It2 and ESD level of HV MOSFETs can be increased as the layout spacing from the drain diffusion to polygate is increased.

I. INTRODUCTION

High-voltage (HV) process has been widely used in LCD driver circuits, telecommunication, power switch, motor control systems, etc [1]. In smart-power technology, high-voltage MOSFET, silicon controlled rectifier (SCR) device, or bipolar junction transistor were used as on-chip electrostatic discharge (ESD) protection devices [2]–[8]. Some ESD protection designs used the lateral or vertical bipolar transistors as ESD protection devices in smart power technology [6], [7]. However, fabrication cost and process complexity are increased by adding bipolar modules into the high-voltage CMOS process. The high-voltage MOSFET was often used as the ESD protection device because it can work as both of output driver and ESD protection device simultaneously in the high-voltage CMOS ICs. Due to an ultra-high operating voltage, the ESD robustness of high-voltage MOSFET is quite weaker than that of low-voltage MOSFET [2]–[8]. Moreover, HV MOSFET will have the extremely strong snapback phenomenon during ESD stress, which often results in non-uniform turn-on variation among the multi-fingers of MOSFET [9]. Hence, ESD reliability has been an important issue for HV IC products fabricated in HV CMOS technology.

In this paper, ESD robustness in a 40-V CMOS process is investigated with or without drift implant. In addition, the layout spacing from the drain diffusion to polygate is split to find its dependence on ESD robustness. All test chips have been fabricated in a 0.35-μm 40-V CMOS technology. The experimental results can provide a design guideline of on-chip ESD protection for HV CMOS ICs.

II. DEVICE STRUCTURES IN 40-V CMOS PROCESS

To integrate the high-voltage devices while maintaining the characteristics of the standard 0.35-μm low-voltage CMOS process without changing all of the design rules and device parameters, the device structures of high-voltage MOSFET can be achieved by adding several additional mask layers in the standard 0.35-μm CMOS technology. The additional mask layers are HV N-well, HV P-well, N-drift or P-drift, N-grade or P-grade, and N-field or P-field. The HV N-well and HV P-well in the HV region are complementary layers which are fabricated on the same P-substrate. The lightly doped N-drift (P-drift), N-grade (P-grade), and N-field (P-filed) implants are required for high voltage MOSFETs to sustain the high voltage (40-V) during normal operating conditions in 0.35-μm 40-V CMOS process.

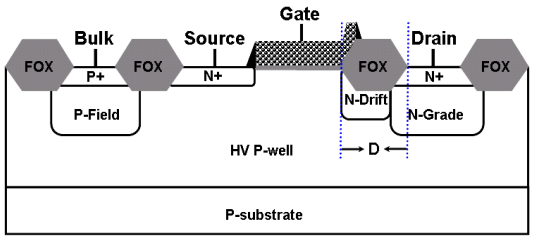
In the given 0.35-μm 40-V CMOS process, the device structures in the test chip can be classified as: (1) HV NMOS with or without N-drift implant in the drain region, (2) HV PMOS with or without P-drift implant in the drain region.

A. HV NMOS With or Without N-Drift Implant

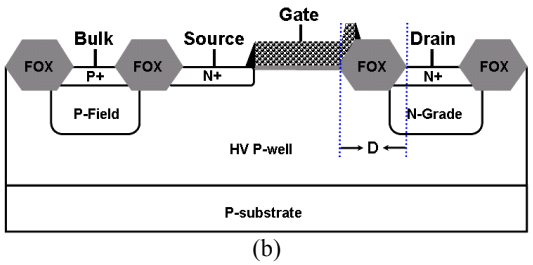
The device cross-sectional views of HV NMOS with or without N-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 1(a) and 1(b), respectively.

The HV NMOS is fabricated in the HV P-well, as shown in Fig. 1(a), where the P-field implant is used as isolation ring to isolate the device from one another. The N-grade implant is used to increase the breakdown voltage of the drain region in the HV NMOS. Moreover, the HV NMOS has lightly doped N-drift implant below the field oxide in the drain region, and utilizes the field oxide between the gate and the drain contact to minimize the peak electric field around the corner of the drain region, which can avoid the hot carrier effect in the N-channel. Furthermore, the N-drift in the drain region can increase the drain-to-source current while the device is under normal circuit operating conditions.

The device structure of HV NMOS without N-drift implant was also fabricated, as shown in Fig. 1(b), where the N-drift in the drain region was removed.



(a)



(b)

Fig. 1. The cross-sectional views of HV NMOS (a) with, and (b) without, N-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chips.

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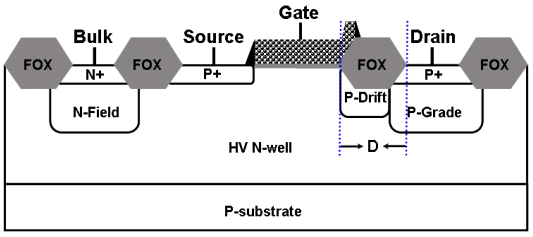
B. HV PMOS With or Without P-Drift Implant

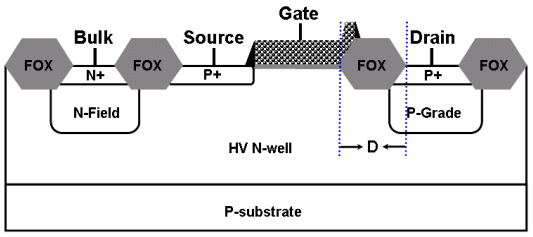
The device cross-sectional views of HV PMOS with or without P-drift implant in the given 0.35-μm 40-V CMOS process are shown in Figs. 2(a) and 2(b), respectively.

The HV PMOS is fabricated in the HV N-well, as shown in Fig. 2(a), where the purpose of N-field implant is the same as the P-field implant in HV NMOS to isolate device from one another. The P-grade implant in the drain region is also used to increase its breakdown voltage for high voltage application. The lightly doped P-drift implant below the field oxide is also used to avoid the hot carrier effect in the P-channel. Furthermore, the drain-to-source current can also be increased under normal circuit operating conditions due to P-drift implant.

The device structure of HV PMOS without P-drift implant was also fabricated, as shown in Fig. 2(b), where the P-drift in the drain region was removed.



(a)



(b)

Fig. 2. The cross-sectional views of HV PMOS (a) with, and (b) without, P-drift implant in the drain region. The spacing (D) from the drain diffusion to polygate is a layout parameter to be investigated in the test chips.

III. EXPERIMENTAL RESULTS AND DISCUSSION

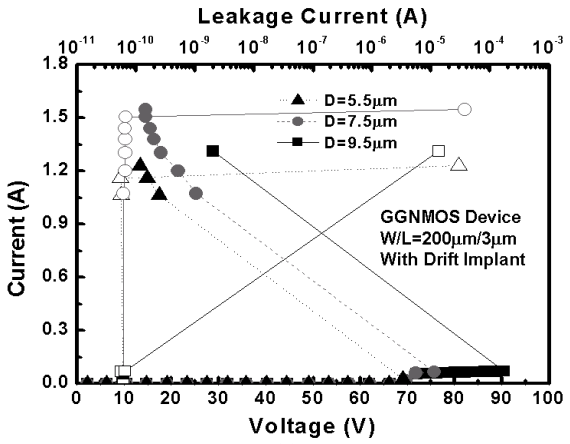
A. TLP-Measured I-V Characteristics

To simulate the human-body-model (HBM) [10] ESD event of the devices, the transmission line pulsing generator (TLPG) [11] is designed to generate stable and consistent pulses of very high current in a very short period of time. To investigate the device behavior during high ESD current stress, the TLP technique with a pulse width of 100ns and rise time of 10ns has been widely used to measure the secondary breakdown current (It2) and turn-on mechanism of ESD devices. In the test chip, the device dimension (W/L) of HV NMOS was 200μm/3μm and the device dimension (W/L) of HV PMOS was 200μm/4μm, where the minimum device lengths (L) of HV NMOS and HV PMOS are 3μm and 4μm in the given 0.35-μm 40-V CMOS process, respectively.

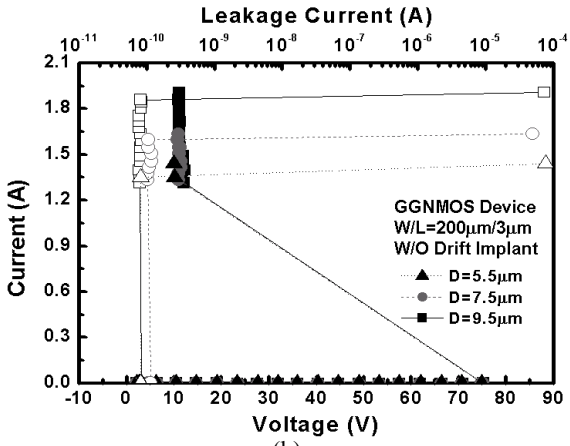
Generally, the ESD robustness is highly dependent on the ESD current discharging path among HV MOSFETs. In HV MOSFETs, the location of ESD damage is usually occurred at the junction breakdown of the drain region. Therefore, in this test chip, the drift implant in the drain region and the layout spacing (D) from the drain diffusion to polygate were split to see the dependence on ESD performance.

The TLP-measured I-V curves of HV gate-grounded NMOS (GGNMOS) with or without N-drift implant in the drain region are shown in Fig. 3, where the layout spacing from the drain diffusion to polygate (D, as shown in Fig. 1) is split to find the dependence on TLP-It2. The trigger voltage of HV GGNMOS with or without N-drift is about 70V~75V, which is higher than the operation voltage of 40V. When the parasitic n-p-n BJT of HV GGNMOS is turned on, it will snap back to a low voltage region. However, comparing with other HV GGNMOS, no double-snapback characteristic [12] was found in the TLP I-V curves of HV GGNMOS in the given 0.35-μm 40-V CMOS process.

In Fig. 3(a), with N-drift implant in the drain region, the parasitic n-p-n BJT of HV GGNMOS will be turned on with a high turn-on resistance as the voltage reaches to about 70V. Then, the TLP I-V curves will snap back to a low voltage snapback region as the voltage reaches to some critical value. Moreover, the TLP-It2 of HV GGNMOS are 1.1A, 1.5A and 0.1A for the spacing D of 5.5μm, 7.5μm, and 9.5μm, respectively. The voltage switching from high turn-on resistance region to snapback region will be increased when the spacing D is increased. With the spacing D of 9.5μm, as shown in Fig. 3(a), the measured TLP-It2 of HV GGNMOS with N-drift implant is only 0.1A, which is due to the higher switching voltage from high turn-on resistance region to low voltage snapback region.



(a)



(b)

Fig. 3. The TLP I-V curves of HV GGNMOS (a) with, and (b) without, N-drift implant in the drain region under different spacings D.

In Fig. 3(b), without N-drift implant in the drain region, the parasitic n-p-n BJT of HV GGNMOS will be turned on as the voltage reaches to about 75V. Then, the HV GGNMOS will soon snap back to a low voltage level of about 10V. Without N-drift implant, there is no high turn-on resistance in the TLP I-V curve. The voltage switching to snapback region is 75V which is independent to the spacing D. Moreover, the TLP-It2 of HV GGNMOS are 1.3A, 1.6A, and 1.9A for the spacing D of 5.5μm, 7.5μm and 9.5μm, where the TLP-It2 is obviously increased as the parameter D is increased.

Comparing Fig. 3(a) and Fig. 3(b), under the same spacing of D, the HV GGNMOS without N-drift implant in the drain region has a higher TLP-It2 than that with N-drift implant in the drain region due to different current distributions among the devices. The current of HV NMOS without N-drift implant will flow more deeply into the HV P-well to avoid the current crowding at the surface of the channel, which can sustain a higher ESD stress. Moreover, without N-drift implant in the drain region, there is no high turn-on resistance in the TLP I-V curves. This is why HV GGNMOS without N-drift implant in the drain region can switch to its snapback quickly and keep at the lower holding voltage, which in turn results in a higher TLP-It2.

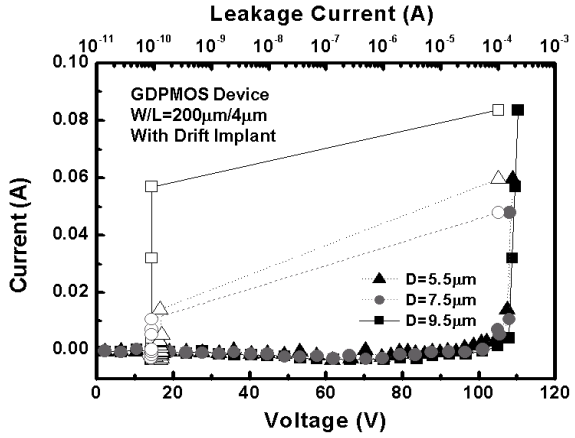


Fig. 4. The TLP I-V curves of HV GDPMOS (a) with, and (b) without, P-drift implant in the drain region under different spacings D.

The TLP-measured I-V curves of HV gate-VDD PMOS (GDPMOS) with or without P-drift implant in the drain region are shown in Fig. 4, where the spacing D is also split to find the dependence on TLP-It2. The trigger voltage of HV GDPMOS with or without P-drift is about 80V, which is higher than the operation voltage of 40V in the given 0.35-μm 40-V CMOS process. After the HV GDPMOS is breakdown, the current will be increased as the voltage is increased. There is no snapback characteristic in TLP I-V curves of HV GDPMOS.

In Fig. 4(a), with P-drift in the drain region, the HV GDPMOS will be turned on as the voltage reaches to about 80V. When the voltage is over 80V, the current of HV GDPMOS will be only slightly increased as the voltage is increased. When the voltage reaches to over 110V, the current will suddenly increase to burn out the HV GDPMOS. Moreover, the TLP-It2 of HV GDPMOS are 0.01A, 0.01A, and 0.06A for the spacing D of 5.5μm, 7.5μm and 9.5μm, where the TLP-It2 is slightly increased as the parameter D is increased.

In Fig. 4(b), without P-drift in the drain region, the HV GDPMOS will be turned on as the voltage reaches to about 80V. If the voltage of HV GDPMOS is continuously increased over 80V, the current will be increased quickly. Moreover, the TLP-It2 of HV GDPMOS are 0.13A, 0.1A, and 0.14A for the spacing D of 5.5μm, 7.5μm and 9.5μm, where the TLP-It2 will is slightly increased as the parameter D is increased.

Comparing Fig. 4(a) and Fig. 4(b), under the same spacing of D, the HV GDPMOS without P-drift in the drain region has a higher TLP-It2 than that with P-drift implant in the drain region. Moreover, while the GDPMOS is turned on, the turn-on resistance of GDPMOS without P-drift implant in the drain region is much lower than that with P-drift implant in the drain region, which will result in the lower holding voltage and higher TLP-It2.

Table I. TLP-It2 of HV GGNMOS and GDPMOS with or without drift implant under different spacings D.

Spacing D in Layout	5.5μm	7.5μm	9.5μm
TLP-It2 of HV GGNMOS (With N-Drift Implant)	1.1A	1.5A	0.1A
TLP-It2 of HV GGNMOS (Without N-Drift Implant)	1.3A	1.6A	1.9A
TLP-It2 of HV GDPMOS (With P-Drift Implant)	0.01A	0.01A	0.06A
TLP-It2 of HV GDPMOS (Without P-Drift Implant)	0.13A	0.1A	0.14A

Table I summarizes the dependence of TLP-It2 of HV GGNMOS and GDPMOS with or without drift implant under different spacings D. Due to the inefficient parasitic p-n-p bipolar action in the HV GDPMOS, no snapback characteristic is found in the TLP-measured I-V curves. So, the holding voltage of HV GDPMOS is much higher than that of HV GGNMOS, which results in a lower TLP-It2 of HV GDPMOS. For both HV GGNMOS and GDPMOS (HV MOSFETs) with the same spacing of D, the device without drift implant in the drain region has a higher TLP-It2 than that with drift implant in the drain region due to the different current distributions among the devices. Moreover, HV MOSFETs with drift implant in the drain region has the higher turn-on resistance than that without drift implant in the drain region. For HV MOSFETs with or without drift implant, the TLP-It2 can be increased as the spacing of D is increased.

B. HBM ESD Robustness

HBM ESD events are produced by the discharge of a charged 100pF capacitor through a 1.5kOhm resistor. The HBM ESD levels of HV GGNMOS and GDPMOS under different spacings D are shown in Figs. 5 and 6, respectively. In the ESD verification, the HBM levels are measured by *KeyTek ZapMaster* and the failure criterion is defined as the I-V characteristic curve shifting over 30% from its original curve after three continuous ESD zaps at every ESD test voltage level. The HBM ESD levels of HV GGNMOS with N-

drift implant in the drain region are about 400V which is not suitable for on-chip ESD protection device in HV CMOS ICs due to the low ESD robustness. By removing the N-drift implant in the drain region, the HBM ESD levels of HV GGNMOS with the same device dimension can be improved up to over 2kV, which can pass the requirement of 2-kV HBM [10]. Moreover, while the spacing D is increased from 5.5μm to 9.5μm, the HBM ESD levels of HV GGNMOS without N-drift implant can be improved from 2kV to 2.8kV.

The HBM ESD levels of HV GDPMOS are only improved from 200V to 300V by removing the P-drift implant in drain region. Moreover, the HBM ESD levels of HV GDPMOS is not increased as those measured by the TLP measurement when the spacing of D is increased due to the minimum step of 100V used in the instrument. Such a low ESD robustness of HV GDPMOS is not suitable for on-chip ESD protection device in HV CMOS ICs. To achieve a good on-chip ESD protection, the power-rail ESD clamp circuit [13] can be added across the power lines of the HV CMOS ICs to avoid the ESD current flowing through the GDPMOS in its breakdown region.

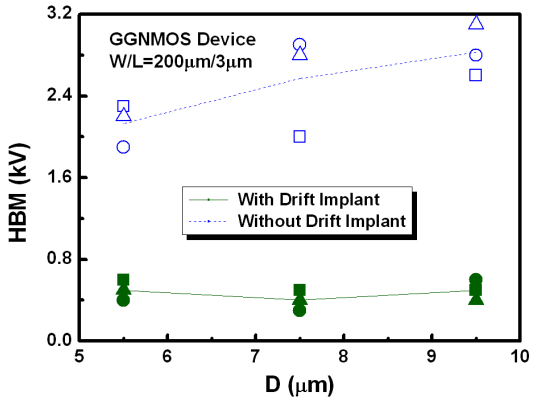


Fig. 5. The HBM ESD levels of HV GGNMOS with or without N-drift implant in the drain region under different spacings D.

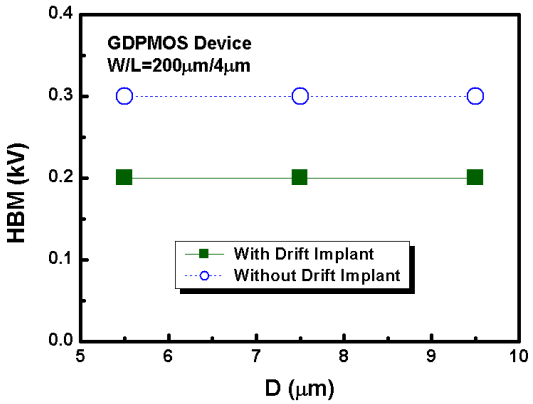


Fig. 6. The HBM ESD levels of HV GDPMOS with or without P-drift implant in the drain region under different spacings D.

IV. CONCLUSIONS

The drift implant in the drain region and layout spacing from the drain diffusion to polygate (D) have been spilt to verify the ESD robustness with silicon chips in the given 40-V CMOS process. It was demonstrated that HV MOSFETs without drift implant in drain region have better TLP-measured It2 and ESD robustness than those with drift implant in the drain region. Moreover, without N-drift implant, the It2 and ESD level of HV GGNMOS can be obviously improved as the spacing D is increased. The ESD robustness of HV GGNMOS can be improved up to pass the requirement of 2-kV HBM by removing the N-drift implant in the drain region. The experimental results can provide a design guideline of on-chip ESD protection to HV CMOS ICs.

ACKNOWLEDGEMENTS

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