CIRCUIT PERFORMANCE DEGRADATION OF SAMPLE-AND-HOLD AMPLIFIER DUE TO GATE-OXIDE OVERSTRESS IN A 130-NM CMOS PROCESS

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ABSTRACT

The effect of gate-oxide reliability on MOS switch in the bootstrapped circuit is investigated with the sample-and-hold amplifier in a 130-nm CMOS process. After overstress on the MOS switch of sample-and-hold amplifier, the circuit performances in the frequency domain are measured to verify the impact of gate-oxide reliability on circuit performance.

INTRODUCTION

The sample-and-hold amplifier (SHA) is an important building block in analog integrated circuits, such as analog-to-digital data converter (ADC). The high-speed and high-resolution analog-to-digital data converter needs a high-performance sample-and-hold amplifier. The low-supply voltage will degrade the performance of the sample-and-hold amplifier due to the nonlinear effect of the MOSFET switch such as body effect, turn-on resistance variation, charge injection, and clock feedthrough. The bootstrapped technique provided a constant voltage between the gate and source terminals of the MOS switch is usually used to improve the performances of sample-and-hold amplifier under the low-supply voltage operation. However, the bootstrapped technique induces the gate-oxide overstress on MOS switch [1-4] to degrade the lifetime of the switch device. Therefore, the gate-oxide reliability on MOS switch in the sample-and-hold amplifier with the bootstrapped technique is a very important reliability issue in analog circuits. The thick-oxide MOSFET device [3] and the suitable device size of the bootstrapped switch circuit [1] can be used to avoid the gate-oxide overstress on the switch device. However, the impact of gate-oxide reliability on MOS switch in the sample-and-hold amplifier is still not investigated.

In this work, the impact of gate-oxide reliability on MOS switch in the sample-and-hold amplifier circuit is investigated in a 130-nm CMOS process. The frequency-domain performances of the sample-and-hold amplifier are measured after the gate-oxide overstress on MOS switch device.

SAMPLE-AND-HOLD AMPLIFIER WITH BOOTSTRAPPED TECHNIQUE

The conceptual schematic of the bootstrapped technique for sample-and-hold amplifier is shown in Fig. 1(a). The basic schematic includes the signal MOS switch M_S, five ideal switches S_1-S_5, and a capacitance C_b. The CLK_1 and CLK_2 clock signals are the out-of-phase signals. When CLK_1 is low and CLK_2 is high, the S_3 and S_4 switches charge the capacitance C_b to the supply voltage V_{DD}, and the S_5 switch is used to turn off the switch M_S. When CLK_1 is high and CLK_2 is low, the S_1 and S_2 switches change the capacitance C_b in series with the input signal V_{IN} and connect to the gate of switch M_S, such that the gate-to-source voltage across the switch M_S is equal to the supply voltage V_{DD}. The gate voltage on the switch device M_S will be charged to $V_{IN}+V_{DD}$, which is larger than the supply voltage. The detailed circuit implementation is shown in Fig. 1(b) [1]. The M_1, M_2, M_3, M_4 and M_5 correspond to the five ideal switches S_1-S_5 shown in Fig. 1(a). The M_6 transistor is added to reduce the maximum drain-to-source voltage (V_{DS}) of M_5 transistor to avoid the gate-oxide overstress. However, the sampling capacitance C_S in the sample-and-hold amplifier with the bootstrapped technique is usually designed with several pF to improve the circuit performance. The different RC delay times between the sampling network (M_S and C_S) and the bootstrapped network (M_1-M_8 and C_b) will induce the transient gate-oxide overstress across the gate-to-drain terminals of the switch M_S to cause the long-term reliability issue in the sample-and-hold amplifier with the bootstrapped technique.

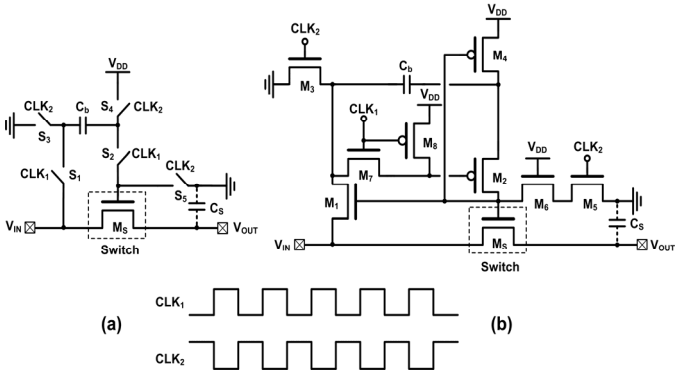

FIGURE 1. (A) CONCEPTUAL SCHEMATIC, AND (B) DETAIL CIRCUIT IMPLEMENTATION, OF BOOTSTRAPPED TECHNIQUE FOR SAMPLE-AND-HOLD AMPLIFIER (SHA).

The sample-and-hold amplifier with the bootstrapped technique has a long-term reliability problem, which causes the circuit performance degradation. The overstress voltage on the gate oxide of the switch device depends on the voltages of input and clock signals. The obvious degradation of circuit performance in the sample-and-hold amplifier with bootstrapped technique needs a long-term operation, which may need many years, to measure the change under the gate-oxide degradation of switch device. In order to accelerate the degradation of circuit performance, the sample-and-hold amplifier with the gate-oxide reliability test circuit is proposed in Fig. 2. The sample-and-hold amplifier with the open-loop configuration is used to verify the gate-oxide reliability of the bootstrapped MOS switch. In Fig. 2, the operational amplifier with the folded-cascode structure is used to realize the buffer. The sampling capacitance C_S is realized by a PMOS transistor.

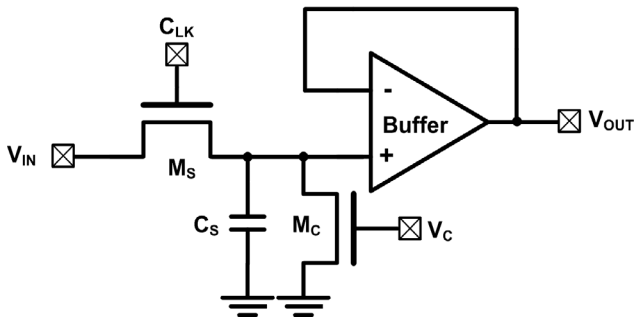

FIGURE 2. COMPLETE CIRCUIT WITH THE GATE-OXIDE RELIABILITY TEST CIRCUIT FOR SAMPLE-AND-HOLD AMPLIFIER.

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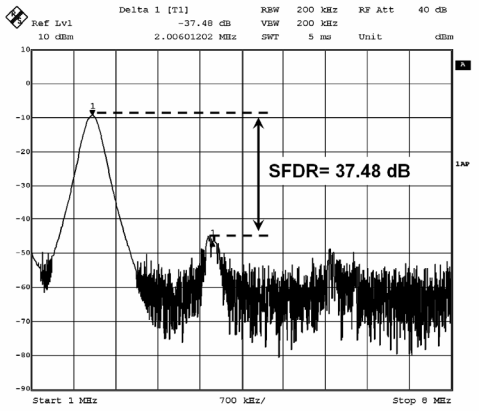
The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in the sample-and-hold amplifier with the gate-oxide reliability test circuit are 1.2 V and 2.63 nm, respectively, in a 130-nm CMOS process. The control device M_C is used to control the drain voltage of the switch M_S. The device ratio of the switch M_S is determined by the sampling frequency of the sample-and-hold amplifier. Therefore, the device ratio of the control device M_C should be designed larger than that of the switch M_S. If the device ratio of the control device M_C is smaller than that of the switch M_S, the drain voltage of control device M_C will not be kept at ground. In normal operation, the control voltage V_C is biased to ground, so the control device M_C is turned off. The sample-and-hold amplifier can be successfully operated under the sample and hold modes, respectively. In the gate-oxide overstress test, the control voltage V_C is biased to supply voltage, and the input signal V_{IN} is kept to the supply voltage. The voltage at C_{LK} node can be applied with any voltage level higher than the supply voltage to overstress the gate oxide of switch device. The voltage across the gate-to-drain terminals of the switch M_S is controlled by the C_{LK} voltage. This test circuit can be used to simulate the overstress across the gate-to-drain terminals of switch M_S in the sample-and-hold amplifier with bootstrapped technique.

OVERSTRESS TEST RESULTS

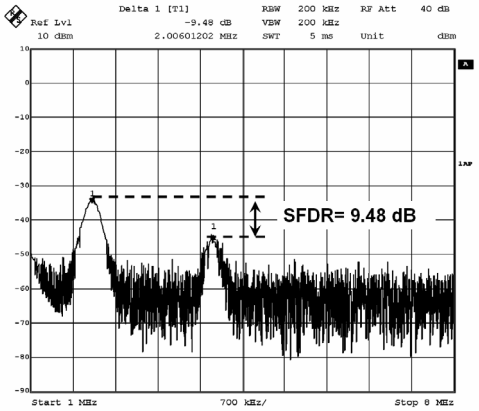
When the sample-and-hold amplifier with the gate-oxide test circuit operates in the overstress mode, the input signal V_{IN} is biased to supply voltage, and the control voltage V_C is set to supply voltage. In order to observe the circuit performance degradation of the sample-and-hold amplifier due to the gate-oxide degradation of switch device, the voltage at C_{LK} node is biased to 1.8 V for accelerating the gate-oxide degradation of switch device. Only the gate-to-drain terminals of the switch M_S is overstressed to simulate the sample-and-hold amplifier with the bootstrapped technique. The frequency-domain waveforms are re-evaluated under this overstress condition. Figs. 3(a) and 3(b) show the frequency spectrum at V_{OUT} node under different stress times with the 25 MHz square signal (sampling frequency) at C_{LK} node and 2 MHz sinusoidal signal at V_{IN} node. The gate-oxide overstress on the switch M_S degrades the performance of the sample-and-hold amplifier. The spurious free dynamic range (SFDR) of the sample-and-hold amplifier is degraded by the gate-oxide overstress on the switch device from 37.48 dB to 9.48 dB after the 8-hours stress time. The effective number bits of the sample-and-hold amplifier will be reduced by gate-oxide overstress on the switch device. Because the gate-oxide degradation induces the leakage current across the drain-to-gate terminals [5], the leakage current of MOS switch causes the voltage at V_{OUT} on the hold mode to be degraded. If the gate oxide (gate-to-drain) of the MOS switch is fully broken down, the output waveform at V_{OUT} node of sample-and-hold amplifier will become square waveform due to the large leakage current. Finally, the sample-and-hold amplifier will not be functional. Therefore, the circuit performance of the sample-and-hold amplifier with the bootstrapped technique is degraded by gate-oxide degradation of switch device after long-term operation.

CONCLUSION

The impact of gate-oxide reliability on switch device in the bootstrapped circuit has been investigated and analyzed with the sample-and-hold amplifier. The frequency-domain waveforms of the sample-and-hold amplifier after different tress times have been measured. The gate-oxide overstress across the gate-to-drain terminals of the switch device induces the leakage current to degrade the voltage at V_{OUT} in the hold mode. After the gate-oxide overstress, the performance of the sample-and-hold amplifier is seriously degraded by gate-oxide degradation of MOS switch. The gate-oxide reliability of MOS switch in the sample-and-hold amplifier with the bootstrapped technique has been a very important application concern for analog circuits in the nano-scale CMOS processes. The bootstrapped technique designed with thick gate-oxide MOSFET device can overcome this problem. How to design the sample-and-hold circuit with only thin gate-oxide devices is still a challenge to analog circuit designers.



(a)



(b)

FIGURE 3. THE MEASURED FREQUENCY-DOMAIN WAVEFORMS OF THE SAMPLE-AND-HOLD AMPLIFIER WITH THE GATE-OXIDE RELIABILITY TEST CIRCUIT UNDER DIFFERENT OVERSTRESS TIMES. (A) OVERSTRESS TIME = 0 HOUR, AND (B) OVERSTRESS TIME = 8 HOURS.

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