EFFECT OF CHEMICAL MECHANICAL POLISH PROCESS ON LOW-TEMPERATURE POLY-SIGE THIN-FILM TRANSISTORS

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ABSTRACT

The improvement of polycrystalline silicon germanium thin-film transistors (poly-SiGe TFTs) using NH_3 passivation and chemical mechanical polishing (CMP) process was examined. Experimental results indicated that NH_3 passivation could effectively improve the turn on characteristics. Moreover, the TFTs fabricated on polished poly-SiGe film exhibit higher carrier mobility, better subthreshold swing, lower threshold voltage, and higher on/off current ratio due to the smooth poly-SiGe interface. [*keywords:* SiGe thin-film transistors, chemical mechanical polishing, passivation, smooth interface]

INTRODUCTION

Polysilicon TFTs have been widely used in various applications. Since the melting point of SiGe is lower than that of Si, the lower process temperature can be used for TFTs fabrication [1-2]. However, the rough surface of channel causes the poor performance and the low reliability of the device. It is shown that a planarized polysilicon surface will yield TFTs with improved performance and reliability. The CMP process has been used extensively for smoothing surface of polysilicon films [3]. Thus it is possible to be applied to smooth the poly-SiGe films. In this paper, we develop optimization strategies for fabrication of high-performance SiGe TFTs.

EXPERIMENTAL

The main process sequence for fabricating the poly-SiGe TFTs is illustrated in **Fig. 1**. The starting materials were 6-inch dummy wafers capped with a 500-nm-thick thermal oxide. Un-doped 100-nm- thick amorphous silicon germanium ($Si_{1-x}Ge_x$, x=0.18) films were deposited by low-pressure chemical vapor deposition (LPCVD). Then the a-SiGe films were transformed into polysilicon phase by a solid-phase re-crystallization (SPC) treatment at 550℃ for 12hr. The films were then polished by CMP process. The parameters of CMP process condition were shown in **Table 1**. After definition of the active channel regions, a 50-nm-thick CVD oxide layer was deposited to form the gate oxide. Subsequently, the SiGe films were deposited and patterned to form the gate electrode. For n-channel transistors, P^+ implant with a dosage of 5×10^{15} cm^{-2} at 25 KeV was performed. The implanted dopants were activated in N_2 ambient. Next, a 300-nm-thick passivation oxide was deposited, followed by contact hole and aluminum pad formation. The samples were then subjected to the NH_3 plasma treatment in various time periods. Electrical characteristics were performed using a HP4156 system.

RESULTS AND DISCUSSION

The surface roughness of the poly-SiGe films were examined by atomic force microscope (AFM). **Fig. 2** shows the surface image of this film before and after CMP. It can be seen that CMP is very effective in smoothing the surface. The roughness of SiGe films are 4.75nm, 1.2nm and 0.35nm for unpolished and polished in 10 and 20 seconds, respectively.

Fig. 3 illustrates the I-V characteristics of unpolished TFTs with various NH_3 plasma treatment times. The treatment results in superior electrical characteristics because of the grain boundaries passivation. The transfer curves of samples with and without CMP process are shown in **Fig. 4**. The observable improvements were not only due to the mobility enhancement, but also due to the significantly reduced leakage current with the reduction of surface roughness. The characteristics of with and without CMP process are shown in **Table 2**. The TFTs fabricated on polished poly-SiGe film exhibits higher carrier mobility, better subthreshold swing, lower threshold voltage, higher on/off current ratio and reduction of trap state density. **Fig.5** shows the density of states in the band gap by field-effect conductance method [4] in different NH_3 treated time. For the long time NH_3 treated TFTs, nitrogen atoms were introduced into the interface reducing the trap state and resulting in a great improvement of device characteristics. The hot-carrier stress test was performed at V_D=15V, V_G=10V, and source electrode grounded for 200sec to investigate the device reliability. **Fig. 6** shows the variations of the threshold voltage over hot carrier stress time. The improvement of the surface roughness at the oxide/poly SiGe interface is found to be critical to reduce the hot carrier generation rate and eliminate damage.

CONCLUSIONS

We have fabricated poly-SiGe TFTs using CMP process. The results clearly show that by employing the plasma and CMP steps, significant improvement in the poly-SiGe TFTs with low thermal budget can be achieved.

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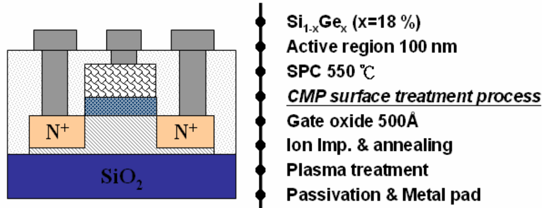
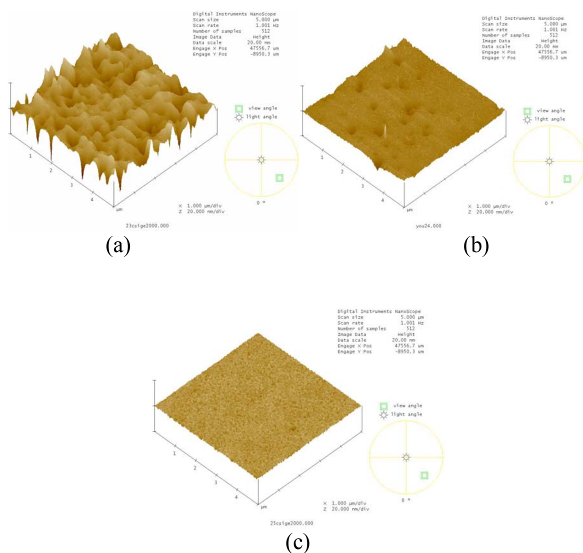


Fig. 1 Process flow for SiGe TFTs.

Table 1 Parameters of CMP process condition

Parameter	Down Force	Platen/ Carrier Speed	Platen Pad	Time	Removal Rate	Slurry (CABOT)	p.H
Value	3 psi	50/50 cyc.	Politex	10,20 sec.	25A /sec.	S.S.-25:H2O 1:9	11.5



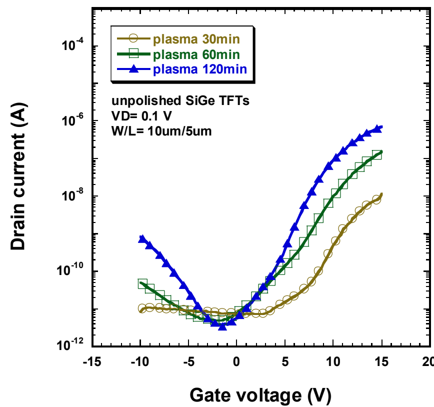


Fig. 2 Three-dimensional AFM images of SiGe film surface (a)before CMP process and after CMP polishing process for (b)10 seconds and(c)20 seconds, respectively.

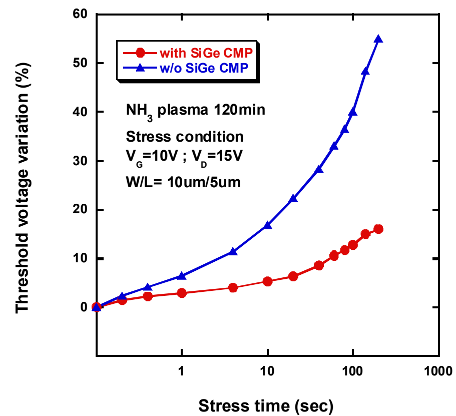


Fig. 3 Transfer curves of unpolished TFTs with various NH_3 plasma treatment times in 30, 60, 120 minutes.

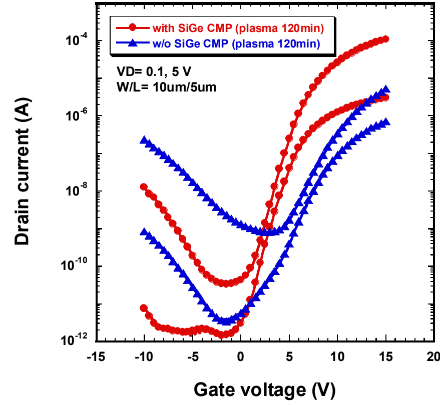


Fig. 4 Transfer curves of SiGe TFTs with and without CMP polishing process.

Table 2 Characteristics of TFTs with and without CMP process

	Vth (V)	S. S. (V/dec.)	μeff (cm^2/V.s)	Ion@ VG=15V (A)	Ioff	ON/OFF Ratio	Nt (cm^{-2})
SiGe TFTs w/o CMP	10.3	2.1	6.3	7.16×10^{-7}	1.21×10^{-11}	5.92×10^{4}	6.42×10^{13}
SiGe TFTs with CMP	5.75	1.25	12.5	3.06×10^{-6}	1.42×10^{-12}	2.15×10^{6}	1.42×10^{13}

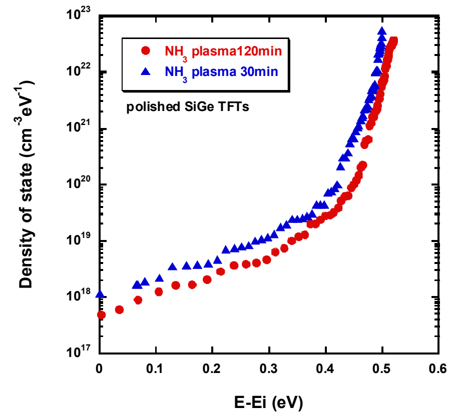


Fig. 5 Density of states in band gap of the device using the polished SiGe film as channel with different NH_3 plasma treatment times.

Fig. 6 Threshold voltage degradation as a function of stress time under hot-carrier stress.