PROCESS INDUCED INSTABILITY AND RELIABILITY ISSUES IN LOW TEMPERATURE POLY-SI THIN FILM TRANSISTORS

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ABSTRACT

We investigated the impact of plasma process on the devices' performance and reliability degradation of low temperature poly-Si thin film transistors (LTPS TFTs). LTPS TFTs with different antenna areas were used to study the effects of the plasma etching process on the devices. The larger TFT antenna area, the more performance instability occurs. The reliability of LTPS TFTs with large antenna areas was found to be degraded from gate bias stress and hot carrier stress. [*keywords:* LTPS TFTs, antenna area, gate bias stress, hot carrier stress]

INTRODUCTION

Poly-Si TFTs are the key devices in flat panel display, such as active-matrix liquid crystal displays (AMLCD) [1]. The high mobility of poly-Si TFTs enables the integration of pixels and driving circuit on a panel. To achieve good process repetitiousness, plasma dry etching process has been widely adopted. Many reports have pointed out plasma process may induce device degradation in VLSI manufacturing [2], but this phenomenon is rarely investigated in poly-Si TFTs. Some studies have indicated plasma process may also degrade the performance of poly-Si TFTs; however, the dependence of the reliability of poly-Si TFTs on plasma process has not been well explored.

In this paper, we investigated the effects of plasma process on the characteristics of low temperature poly-Si TFTs (LTPS TFTs). Moreover, in order to investigate the plasma damage effects on the reliability of LTPS TFTs, both gate bias stress and hot carrier stress were applied in our research.

EXPERIMENTAL

N-channel LTPS TFTs with 1.5um LDD structure were fabricated in this study. A 43-nm-thick amorphous-Si layer was deposited on a buffer layer and crystallized by excimer laser annealing. Channel doping was then applied for V_{th} adjustment. After source/drain formation, gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer. Mo was deposited and patterned as the gate electrode. After gate formation, self-aligned LDD was formed. Finally, inter-layer dielectric and inter-connection metal were deposited and patterned. The antenna area ratio (AR) is defined as antenna area over gate area on active region. **Figure 1** shows the schematic cross-section diagram of the structure. Two sets of antenna patterns were designed as shown in **Table 1** and **Table 2.**

RESULTS AND DISCUSSION

There are many device parameters to check plasma process effects, such as threshold voltage shift (ΔV_{th}) and drive current degradation (ΔI_{ON}) [4]. **Figure 2** reveals the threshold voltage distribution of LTPS TFTs, which shows clear dependence on AR. When the device is exposed to plasma, stress occurs as charges are placed on the gate electrode and creates a voltage across the gate oxide. Such stress causes the generation of trap states in the gate oxide [5]. Thus, the LTPS TFT with larger AR shows more instability in V_{th} due to enhanced plasma damage.

Figure 3 illustrates the time dependence of ΔV_{th} under positive gate bias stress. The transfer characteristics of LTPS TFTs before and after gate bias stress for 1000s are also shown in **Fig. 4**. Plasma process creates numerous trap states in the gate oxide, and the number of trap states depends on the degree of damage [5]. When positive gate bias stress was applied to the damaged LTPS TFT, electrons were injected into the gate oxide and captured by the trap states, resulting in the shift of V_{th}. The schematic diagram of the damaged LTPS TFT after gate bias stress is shown in **Fig. 5**.

Figure 6 shows the I_{ON} degradation rate of LTPS TFTs under hot carrier stress. The device with larger AR is susceptible to plasma damage and generates more trap states in the gate dielectric. During the hot carrier stress, carriers have more chance to be injected into the gate dielectric and generate more interface states. Therefore, the LTPS TFT with AR=1000 shows serious drive current degradation.

The distribution of V_{th} for different channel width in LTPS TFTs with a fixed AR of 1000 is shown in **Fig. 7**. The device with 30um channel width shows more non-uniform V_{th} distribution than those with smaller channel width. This is due to the difference of antenna area exposed in plasma. **Figure 8** shows the ΔV_{th} for devices with AR=1000 under gate bias stress. The LTPS TFT with larger channel width shows larger ΔV_{th}, because the bigger antenna area enhanced the plasma damage. The ΔV_{th} of LTPS TFTs with a fixed AR under hot carrier stress is shown in **Fig. 9**. The TFT with smallest channel width has smallest ΔV_{th}. **Figure 10** reveals the transfer characteristics and transconductances of the TFT under hot carrier stress corresponding to the points A and B in **Fig. 9**. In the beginning of the stress, holes were trapped in the gate oxide. Later, electron trapping dominates.

CONCLUSIONS

The effects of plasma process on the reliability of LTPS TFTs have been investigated. As the antenna area increases, the uniformity of device characteristics becomes degraded. Because the device with large antenna area has more trap states in the gate oxide, the device after gate bias stress and hot carrier stress shows severe degradation on the threshold voltage and drive current, respectively. Therefore, for the fabrication of high reliable devices and yield improvement, the antenna structures must be carefully designed.

ACKNOWLEDGEMENT

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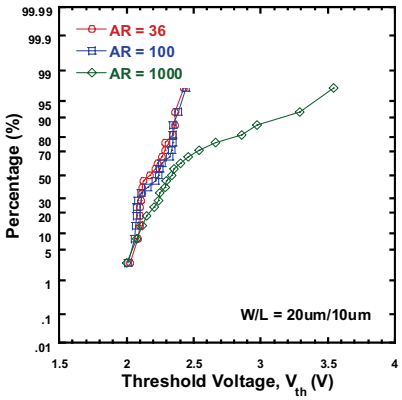

Fig. 2 Cumulative probabilities of V_{th} for LTPS TFTs with various AR.

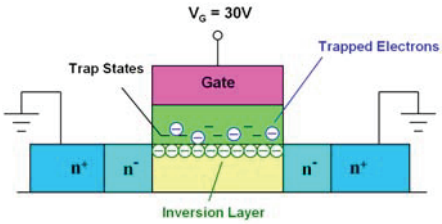

Fig. 5 Schematic diagram of the damaged n-channel LTPS TFT under gate bias stress.

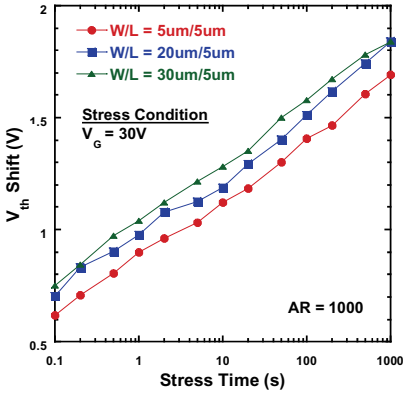

Fig. 8 Time dependence of ΔV_{th} for LTPS TFTs with different channel widths under gate bias stress.

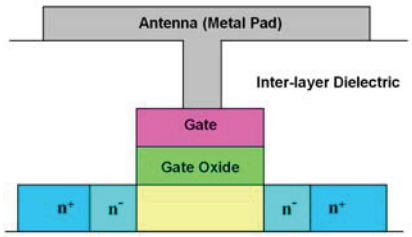

Fig. 1 Schematic cross-section diagram of the test structure used in this work.

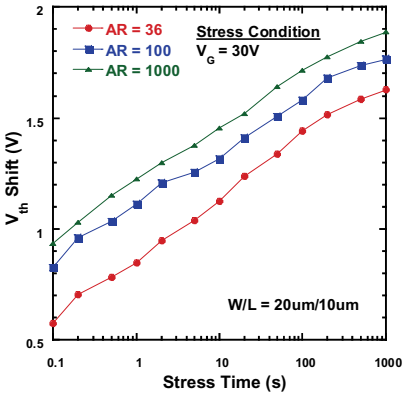

Fig. 3 Time dependence of ΔV_{th} for LTPS TFTs with various AR under gate bias stress.

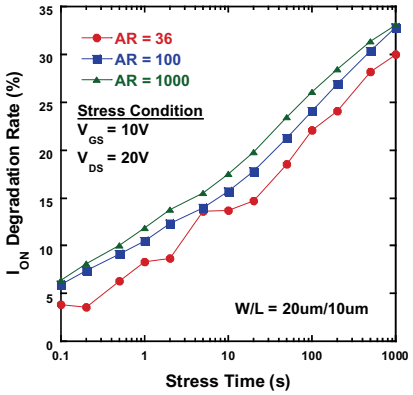

Fig. 6 Time dependence of I_{ON} degradation for LTPS TFTs with various AR under hot carrier stress.

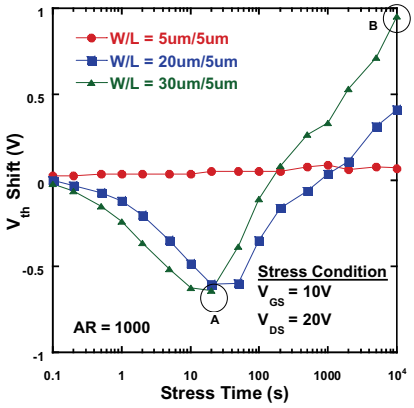

Fig. 9 Time dependence of ΔV_{th} for LTPS TFTs with different channel widths under hot carrier stress.

Table 1 Antenna patterns with "fixed gate area" on active region.

W/L (um/um)	AR	Antenna Area (um^2)
20/10	36	7200
20/10	100	20000
20/10	1000	200000

Table 2 Antenna patterns with "fixed AR" of 1000.

W/L (um/um)	AR	Antenna Area (um^2)
5/5	1000	25000
20/5	1000	100000
30/5	1000	150000

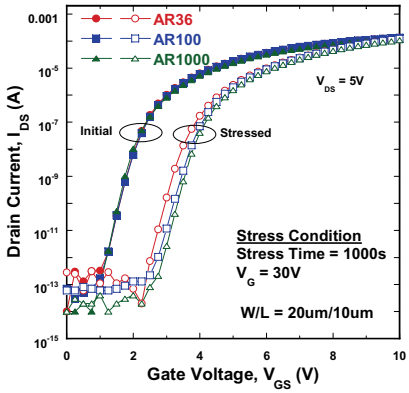

Fig. 4 I_{DS}-V_{GS} of LTPS TFTs with various AR under gate bias stress for 1000sec.

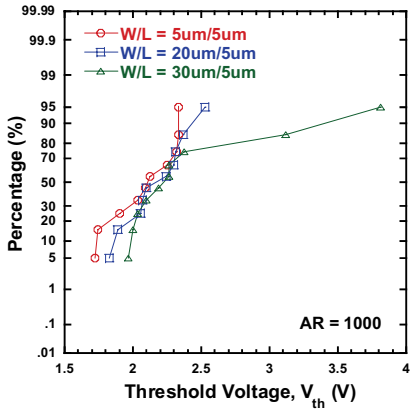

Fig. 7 Cumulative probabilities of V_{th} for LTPS TFTs with different channel widths.

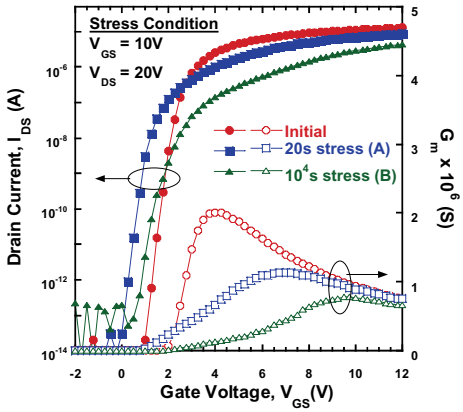

Fig. 10 I_{DS}-V_{GS} and G_m of LTPS TFTs corresponding to points A and B in Fig. 9.