Reliability Issues for High Performance Nanoscale CMOS Technologies with Channel Mobility Enhancing Schemes

Steve S. Chung
Emerging Device and Technology Lab., Department of Electronic Engineering,
National Chiao Tung University, Hsinchu, Taiwan
TEL: 886-3-573 1830 FAX: 886-3-573 4608 email: schung@cc.nctu.edu.tw

Abstract*- In this talk, an overview of the mobility enhancing techniques for high performance/low power CMOS technologies will be introduced first. Two categories for mobility enhancing schemes, channel induced strain using Si/SiGe, and hybrid-substrate engineering, with (100) and (110) orientations, will be discussed next. In terms of the device reliability, different mechanisms are responsible for these two different technologies. While we have paid much more attention on the performance of these technologies, the device reliability has not been taken care of in the past studies. As a consequence, this talk will address several examples of these mobility enhancing schemes and their impact on the device reliability for advanced CMOS technologies for 65nm and beyond.*

1. The Strain-Engineering for Mobility Enhancement

The interest in the strain engineering has been speed-up in recent years for a need in further scaling of CMOS device for high speed and low power applications. A typical 3D strain engineering is illustrated in Fig. 1 [1], in which biaxial stress can be achieved by channel [2] or substrate engineering[3]. Uniaxial strain can be achieved by trench isolation, silicide, nitride cap layer, and recessed S/D etc [4]. Depending on process types and device structures, these devices exhibit mobility enhancement with a factor of up to 100% or even higher over that of conventional process/device structures.

2. The Channel Engineering

The MOSFET with a strained-Si/SiGe channel has been the prime initiative for mobility enhancement schemes. Fig. 2 shows the schematic diagram of a typical strained-Si device made on a conventional bulk-Si or SOI substrate. As a result of the lattice mismatch shown in Fig. 3, a Si layer on relaxed SiGe layer is under a tensile strain, which modifies the band structure and enhances carrier transport since this induces a lower effective mass of the carriers. Figs. 4 and 5 show the n-MOSFET and p-MOSFET drain currents and mobilities respectively [5]. It shows that Si/SiGe n-MOSFET mobility has been increased 70% over that of bulk device. However, there is one disadvantage of the SiGe strained devices in that p-MOSFET does not get much gain. Here comes another idea on developing p-MOSFET on (110) substrate [3]. A typical result shown in Fig. 6 manifests that p-MOSFET mobility has been enhanced while we receive a loss of mobility in n-MOSFET [6]. As a result, an idea of the so-called hybrid substrate CMOS technology becomes a more promising technology.

3. The Hybrid-Substrate Engineering

In order to maintain a simultaneous current gain in a CMOS technology, we can take advantage of the n-MOSFET on (100) substrate while p-MOSFET is made on (110) substrate. This constitutes the hybrid substrate technology[3] as shown in Fig. 7. Here, p-MOSFET mobility can be more than doubled on (110) Si-substrate with current flow on the (110) direction comparing to that along the (100) direction (Fig. 7). Also, electron mobility is the largest along the (100) direction.

4. The Challenges on the Reliability of Mobility Enhanced Devices

A. Enhanced Degradations in Strained Si/SiGe Devices

As mentioned above, Figs. 4 and 5 show the drain currents and mobility for both nMOS and pMOS devices, respectively.

For strained-Si devices, there is much larger drain current enhancement in nMOS. This drain current enhancement is related to the enhanced mobility in the strained channel. To investigate its degradation mechanisms, the vertical and lateral field effects have been evaluated. Fig. 8 shows the measured ICP for studying the vertical field effect in both

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bulk and strained devices under FN stress. Since ICP is proportional to the generated Nit, we do not see a major difference. However, when we look at the comparison for devices under VG= VD HC stress(Fig. 9), we have seen a huge difference of ICP for bulk and strained devices, in which lateral field becomes dominant. This implies that the more enhancement in channel mobility is, the larger is the device degradation. In other words, the enhanced degradation is weaker in the vertical direction but stronger in the lateral direction for strained-Si devices.

Although the Si/SiGe strained devices have shown the merit of high performance, their reliabilities can not be easily controlled as good as those of bulk-Si devices. Wang et al. [7] revealed the difficulties of controlling Ge out-diffusion into the channel such that it will limit the integration and manufacturing problems. It also leads to an increase of the off-state leakage current. Good control of the Ge out-diffusion becomes important.

B. Reliability for Hybrid-Substrate Technology

If we examine the reliability of devices mode on (110) substrate, we can also find a similarities of the device reliability in that those mobility enhanced devices may exhibit a worse reliability. One example is shown in Figs. 10 and 11 where the HC reliability for both (100) and (110) orientations are demonstrated. For HC evaluations, these results show the comparison between FN stress and VG=VD HC stress. This comparison shows a comparable degradations in that the main degradation mechanism is mainly contributed from the vertical field. It implifies that the degradation is not related to the lateral field but comes from the vertical field as supported by the weak dangling bond between Si and O for the (110) surface.

C. NBTI Comparisons for Strained-Si and (110)/(100) Substrate Devices

To explore the NBTI effect, gated-diode measurement [8] has been conducted. For the strained-Si device NBTI-like measurements in Fig. 12, we see that HC effect (component 2) is enhanced comparing to bulk devices(component 1) and is consistent with the previous HC observations in that major degradations come from the lateral field. For the (110) and (100) comparisons in Fig. 13, the results show that the enhanced degradation by NBTI is larger comparing to HC component. In short, for high temperature stress of (110) devices, the vertical field effect is stronger than that of lateral field and its origin is believed to be the weak Si-H bond. It can be concluded that we have seen different field effects for different mobility enhancement scheme using various strained-Si or (110) orientations.

To summarize, although various mobility enhancing schemes have been shown with very good performance in terms of its ION, IOFF, we still face challenges for a successful applications in terms of the process control, manufacturability, and in particular their reliabilities. For either strained channel or substrate engineering with combination of mobility enhancing schemes, it tends to give a worse reliability for the advanced CMOS devices. Therefore, Much effort needs to be done for the understanding of their reliabilities before these devices can be used for high end logic applications.

Acknowledgments

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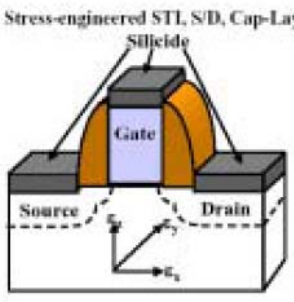

Fig. 1 Several different approaches to enhance the mobility of CMOS devices. [1]

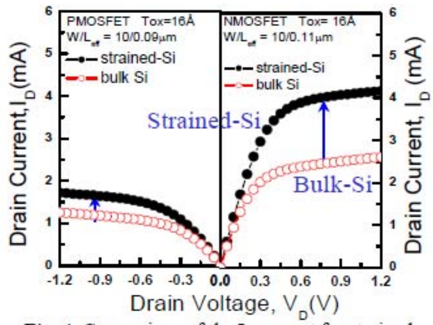

Fig. 4 Comparison of the I_D current for strained-Si and bulk-Si devices, (left) p-MOSFET (right) n-MOSFET.

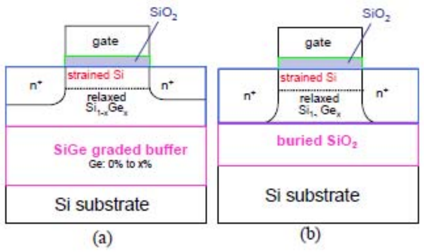

Fig. 2 (a) The strained Si/SiGe structure on bulk-Si substrate and (b) the strained Si/SiGe on SOI substrate.

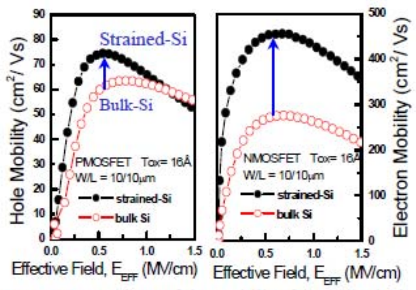

Fig. 5 Comparison of the mobility for strained-Si and bulk-Si devices, (left) p-MOSFET, (right) n-MOSFET.

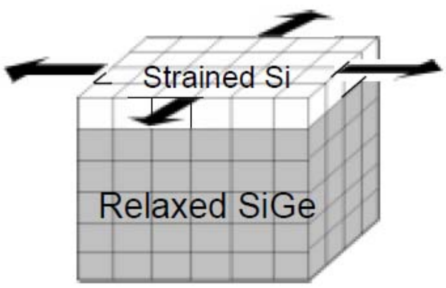

Fig. 3 A strained-Si layer on top of SiGe showing the biaxial strain.

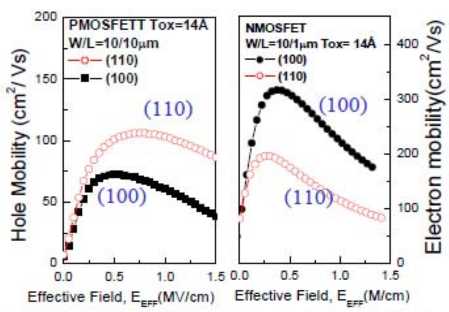

Fig. 6 Comparison of the mobility for (110)and (100) substrate devices, p-MOSFET (left) and n-MOSFET (right).

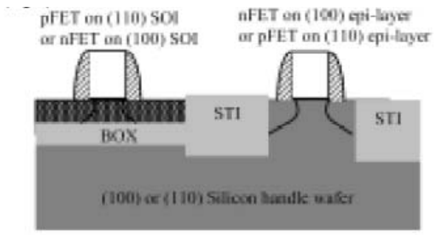

Fig. 7 The concept of hybrid substrate engineering with pMOSFET on (110) substrate while nMOSFET is on (100) substrate. [3]

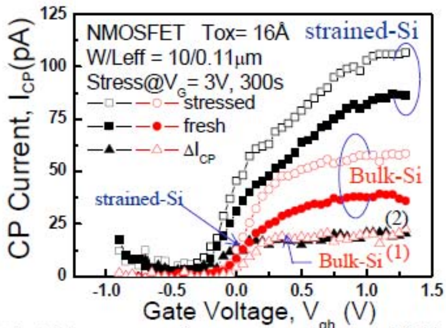

Fig. 8 The stress experiment to show the vertical field effect on the device reliability. [5]

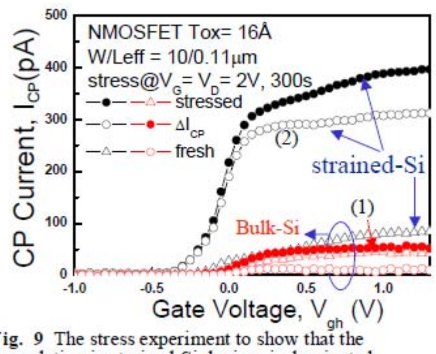

Fig. 9 The stress experiment to show that the degradation in strained-Si devices is dominated by the lateral field effect. [5]

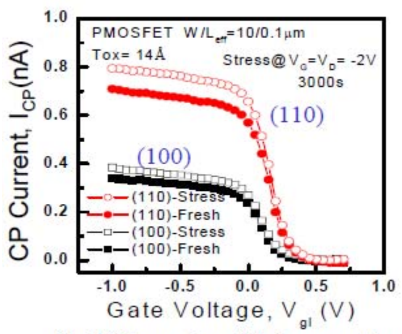

Fig. 10 Comparison of the I_{CP} current for worst HC stress at V_G=V_D of (110) and (100) substrate p-MOSFET's.

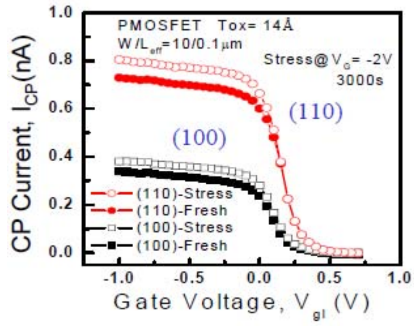

Fig. 11 Comparison of the I_{CP} current for FN stress at V_G= -2V of (110) and (100) substrate p-MOSFET's.

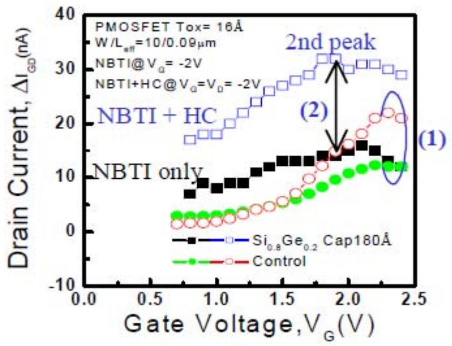

Fig. 12 Gated-diode measurement for strained and bulk devices after V_G=V_D NBTI and NBTI-like HC stress. Note the difference of NBTI-like HC and NBTI of strained Si is larger than bulk Si.

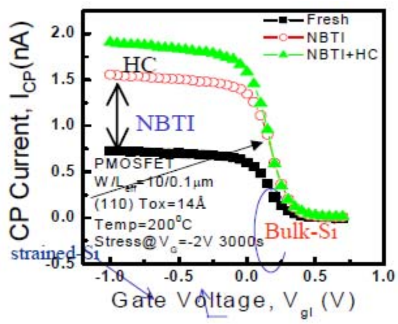

Fig. 13 Comparison of the I_{CP} current for NBTI and NBTI like HC stress of (110) substrate p-MOSFET. Note that NBTI stress induced degradation is larger comparing to HC effect. This is different from strained-Si (Fig. 12).