A 40-nm-Gate InAs/$In_{0.7}Ga_{0.3}As$ Composite-Channel HEMT with 2200 mS/mm and 500-GHz f_T

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***Abstract*— A 40-nm T-gate high-electron-mobility-transistor with InAs/$In_{0.7}Ga_{0.3}As$ composite-channel has been fabricated. The device exhibits a transconductance (g_m) of 2200 mS/mm, a cutoff frequency f_T of 506 GHz and a minimum noise figure of 1.21 dB at a frequency of 58 GHz. These performances make the device well-suited for millimeter-wave or sub-millimeter-wave applications.**

Keywords- InAs-channel, HEMTs, sub-millimeter-wave

I. INTRODUCTION

For high-frequency wireless communication applications such as remote atmospheric sensing, weapon detection, through-wall imaging and future automobile collision avoidance systems, it is essential to fabricate a low-noise amplifier (LNA) MMICs with high gain, large bandwidth, and low power consumption [1]. InP-based high electron mobility transistors (HEMTs) show great potential for such demand because of their high low-field electron mobility properties, high peak electron velocity and high sheet carrier density [2-4]. In general, the InAs has high electron mobility of 40,000 cm^2/Vs at room temperature, high electron peak velocity, low electron effective mass ($0.023/m_0$), reasonable energy bandgap (0.36 eV) and high quantum confinement in the channel region [5]. Therefore, the InAs material shows great potential as a transistor-channel candidate in future microwave and millimeter-wave low-power consumption applications [6,7]. Nevertheless, the device structure required to be optimized to avoid short channel effect in order to achieve high current gain cutoff frequency together with low noise figure (NF) [8, 9].

In this study, we report on the fabrication of the 40-nm-gate InAs/$In_{0.7}Ga_{0.3}As$ composite-channel HEMTs and their DC/RF electrical performance. An extremely high transconductance of 2200 mS/mm and current gain cutoff frequency of 506 GHz were achieved for the devices due to the short distance of gate-to-channel and the superior electron transport properties. Additionally, a noise figure of 1.21 dB was measured at 58 GHz biased at V_{DS} = 0.7 V.

II. DEVICE FABRICATION

The HEMTs structure of InAs-channel was grown by Molecular Beam Epitaxy (MBE) on InP. The epi-layer, from the bottom to top, consists of a 500-nm InAlAs buffer layer, a 2-nm InGaAs lower subchannel, a 5-nm InAs channel, a 3-nm InGaAs upper subchannel, a InAlAs spacer layer, a 8-nm InAlAs barrier, a 4-nm InP etching stop layer, and a 40-nm si-doped InGaAs cap (2×10^{19} cm^{-3}).

The mesa isolation was done by wet chemical etch. Source and drain ohmic metals were formed with Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 ^oC for 30 s. Then a 60-nm silicon nitride film was deposited to be a support of nanometer gate length foot. The 40-nm T-shaped gate was carried out in JEOL electron beam system with 100 pA beam current using a conventional ZEP/PMGI/ZEP tri-layer resist. Gate recess was performed by two-step-recessed technique and Pt-buried gate. Silicon nitride film was etched by ICP using the gas mixture of SF_6 and Ar. After Si_3N_4 etching, the heavy doped InGaAs cap layer was removed by wet chemical etching using PH-adjusted succinic acid-based solution. Ar plasma was used to etch the InP etch-stop layer and part of the InAlAs schottky layer. Then the Pt/Ti/Pt/Au gate metal was formed by evaporation and lift off process. In order to attain gate stability and a short gate-to-channel

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distance (d_{GC}) between channel and gate electrode, the wafer was annealed at 250 ^{o}C for 10 min in a forming gas ambient. In addition, the passivated SiNx was deposited in order to improve not only the mechanical strength of deca-nano gate but also electric and thermal stability that will enhance the breakdown voltage and reliability. SEM image of the 40-nm T-shaped gate HEMT is shown in figure 1. As can be seen from SEM image, the fabricated 40-nm T-gate shows structural stability, even though the narrow gate foot and the side-recess length was 50 nm.

III. RESULTS AND DISSCUSION

The current voltage characteristics of fabricated 40-nm InAs HEMTs are shown in Fig. 2a. The device exhibit good pinch-off characteristics and the threshold voltage of -0.18 V at V_{DS} = 0.5 V. In addition, an on-state breakdown voltage of 1.4 V, which defined at 1 mA/mm gate current was measured. Fig. 2b shows the transconductance g_m versus gate–source voltage V_{GS} curves of the 40-nm gate InAs HEMTs with different drain bias. The source-drain current density I_{DS} was 600 mA/mm. The peak g_m of a 40-nm device was 2200 ms/mm at drain voltage V_{DS} = 0.9V. In particular, the peak gm of device occurred at the gate bias between 0.05 and 0.15 V. The fabricated HEMTs operate in quasi-enhancement mode and could be comparable to E-mode devices. Such E-mode devices have the advantage of single bias operation which greatly simplifies DC biasing schemes in terms of circuit realization. Meanwhile, the main reasons for this high g_m are the short d_{GC} between the gate electrode and 2DEG channel, low source resistance, high electron transport property in the InAs channel, as well as the suppression of the short channel effect.

The RF characteristics were measured by using Cascade Microtech on-wafer probing system and a vector network analyzer (HP8510XF) from 5 to 80 GHz. A standard load-reflection-reflection-match calibration method was used to calibrate the measurement system. The parasitic capacitances due to the probing pads were carefully subtracted from the measured S-parameter of the fabricated device [10, 11]. Fig. 3 shows the frequency dependence on the current gain H_{21} and the power gain "MAG/MSG" of the 40-nm-gate InAs HEMTs. A high f_T of 506 GHz and a maximum oscillation frequency of 285 GHz were simultaneously obtained when biased under V_{DS} = 1.0 V and V_{GS} = 0.05 V. The f_T versus drain current density as a function of various drain bias were shown in Fig.4. It should be noted that f_T will exceeds 300 GHz even in very low applied voltage, V_{DS} =0.5 V. Therefore, it indicates the suitability of InAs HEMTs for high-speed and low-power applications. This superior result is again attributed to the high channel aspect ratio and small lateral gate-recess region. The small side-recess structures were adjusted to increase the lateral electric field under the gate, resulting in accelerating the electron velocity [12]. Additionally, the gate leakage current was 9×10^{-6} A at V_{GS} of -0.2 V, indicating that good Schottky characteristics were achieved by using the Pt-buried gate on InAlAs Schottky barrier layer. These results were caused by the high Schottky barrier height Pt metal and the forming amorphous layer under gate which in turn decreased the grain boundaries and reduced the leakage current path. [13]. The fabricated InP-based devices showed good stability, no kink effect, no short channel effect, and frequency dispersion in the transconductance.

Fig. 5 shows the measured minimum noise figure (NF) together with the associated gain as a function of gate bias with drain biased at 0.7V at 54GHz and 58GHz. As is seen from the figure, a minimum NF of 1.12dB was achieved at the gate bias of 0.05V. Such optimal gate bias for minimum NF also corresponds to peak g_m and f_T as evidenced from Fig. 2 and Fig. 4. The NF and associated gain (Ga) as a function of frequency ranging from 18 to 64 GHz at V_{DS} = 0.6 V were plotted in the Fig. 6. The measured NF_{min} at 60 GHz was 1.75 dB with a corresponding gain of 3.4 dB and the corresponding power consumption was 10.3 mW.

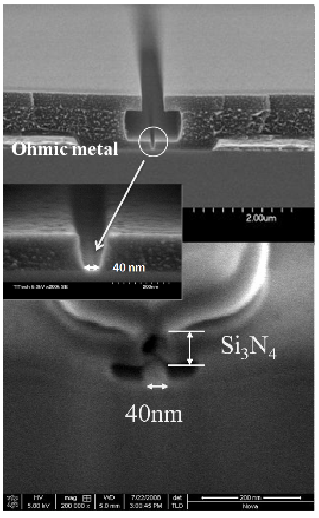
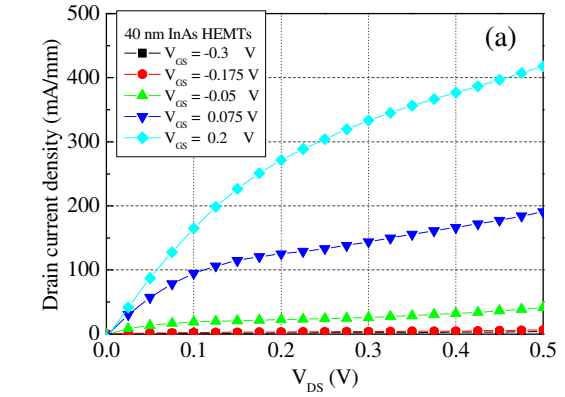


Fig. 1 SEM image shows the bottom of the 40-nm-gate T-Shaped Gate for InAs HEMT.



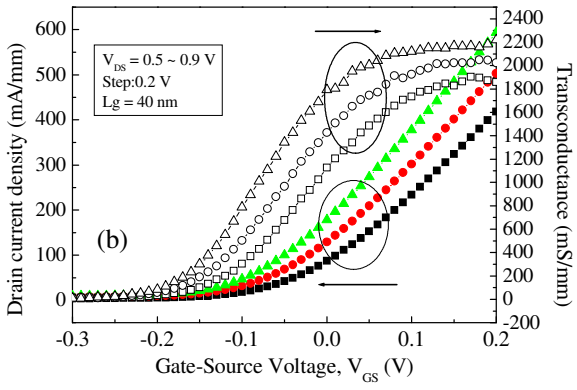


Fig. 2 (a) Current-Voltage (I_{DS}-V_{DS}) characteristics of the 40 nm HEMTs (b) DC drain current density and transconductance g_m as a function of V_{GS} with different drain voltage V_{DS}.

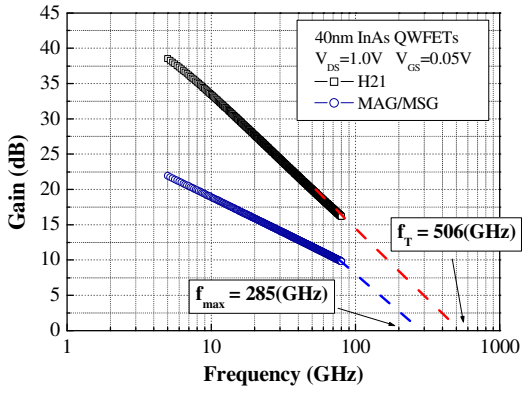


Fig. 3 Frequency dependence of H_{21} and MAG/MSG for the 40-nm-gate InAs HEMTs. The frequency range was from 5 to 80 GHz and the device was bias at V_{DS} = 1.0 V and V_{GS} = 0.05 V.

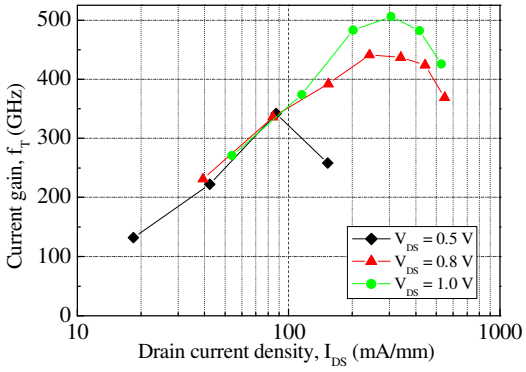


Fig. 4 current gain f_T vs. I_{DS} and V_{DS} of fabricated 40-nm InAs HEMTs.

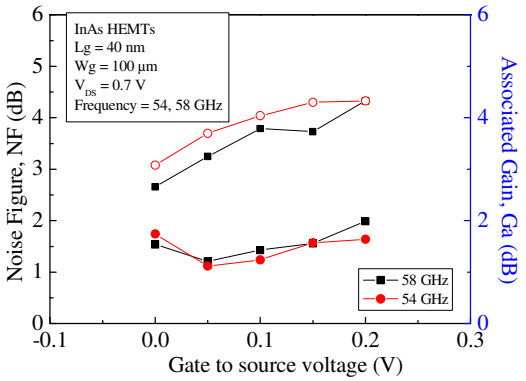


Fig. 5. Gate-source voltage dependence on minimum noise figure and associated gain.

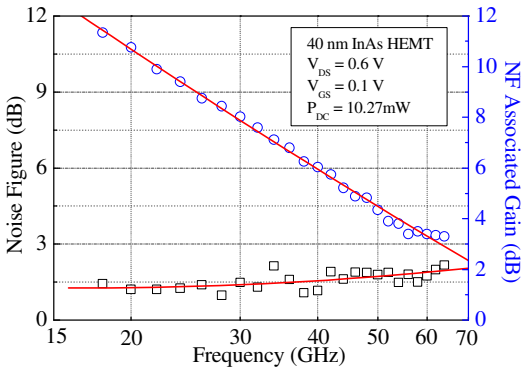


Fig. 6. Measured minimum noise figure and associated gain for drain bias of 0.6 V with the frequency range from 18 to 64 GHz.

The state-of-the-art results indicate that deep-nano scale gate InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs are suitable for high-gain and low-noise amplifiers and receivers for next generation sub-millimeter wave communications and high-resolution imaging applications.

IV. CONCLUSION

In this study, we have successfully fabricated 40-nm-gate length InAs/$In_{0.7}Ga_{0.3}As$ composite channel HEMTs with a maximum g_m of 2200 mS/mm, a high f_T of 506 GHz and a minimum noise figure of 1.21 dB at 58 GHz. The excellent performance can be attributed to the high mobility of the InAs material, the short Lg of 40 nm, short distance between gate electrode and channel, and the use of Pt-buried gate technology. This high-frequency characteristics and low noise property show great potential for millimeter-wave, submillimeter-wave communications applications and high-resolution image system.

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