Proceedings of ESSDERC, Grenoble, France, 2005

Physics and Modeling of Ge-on-Insulator MOSFETs

Albert Chin[(1)], H. L. Kao[(1)], Y. Y. Tseng[(1)], D. S. Yu[(1)], C. C. Chen[(1)], S. P. McAlister[(2)], C. C. Chi[(3)]

(1) Nano-Sci. Tech. Center, Dept. of Electronics Eng., NCTU, Univ. System of Taiwan, Hsinchu, Taiwan, ROC
(2) National Research Council of Canada, Ottawa, Canada.
(3) Dept. of Physics, National Tsing Hua Univ., Hsinchu, Taiwan, ROC
achin@cc.nctu.edu.tw

Abstract:

We have used process and device simulation tools (T-Supreme and Medici) to analyze the measured DC characteristics of Ge-on-Insulator (GOI) MOSFETs. The GOI devices have higher drive current than do their Si counterparts, due to the smaller effective mass (m^*) and smaller Ge energy bandgap – however this also causes a larger off-state I_{ds} leakage current. The simulations predict that the GOI MOSFETs have better RF gain and noise performance compared with Si devices. This is important for high speed operation as down-scaling continues.

1. Introduction

As the down-scaling of VLSI technology continues into the sub-100nm regime, the degradation of drive-current/gate-width of Si MOSFETs, limited circuit delay improvements, and increasing DC and AC power consumption are significant challenges for continuing the technology evolution [1]-[3]. These occur along with increasing manufacturing costs. The performance degradation in the MOSFETs may be overcome if the channel mobility is improved. Devices involving Ge-on-Insulator (GOI) are potentially useful because they show drive currents better than those of currently-used strained-Si. The bulk electron and hole mobilities in Ge are half to one-order of magnitude higher than those in Si. In addition the low process temperature of GOI makes it an ideal candidate for metal-gate and high-κ gate dielectric integration [4]-[7], both of which are essential for reducing the DC power dissipation arising from the gate leakage current [8]-[10]. The low process temperature is also important for three-dimensional (3D) IC integration [4]-[5] – currently the only known way to reduce the dynamic AC power consumption from the backend interconnects [4]. Since the 3D GOI improvements - higher drive current (2-3.5 X) and lower power consumption - only require a simple bonding and smart-cut process, it may help alleviate the rapidly-increasing manufacturing costs associated with down-scaling. However, the drawbacks of GOI technology are the small energy bandgap (E_G) of Ge, the related higher drain-source off-state leakage current, and the required ultra-thin body (UTB) GOI structure that is needed to lower the leakage [11]. There are also no reported device characteristics for small gate length (L_G) GOI MOSFETs. In this paper we have used process and device simulations (T-Supreme and Medici) to analyze measured DC characteristics of GOI MOSFETs. We confirm that the higher DC drive current and mobility arise from the smaller effective mass (m^*) of Ge compared with Si. After calibrating T-Supreme and Medici for 0.18μm Si MOSFETs, we also simulated the RF performance of 0.18μm gate-length GOI MOSFETs. Significant improvement of the RF current gain ($|H_{21}|^2$), unity-gain cut-off frequency (f_t), and minimum noise figure (NF_{min}) were obtained for GOI MOSFETs compared with their Si counterparts [12]-[16]. The RF performance improvements, vital for high speed circuits, also arise from the smaller m^* in Ge.

2. Simulation Procedure

We first calibrated the T-Supreme and Medici simulations using data for multi-fingered 0.18μm Si MOSFETs, made in an IC foundry. The primary function of Medici is to solve the three partial differential equations - Poisson, Boltzmann Transport and Continuity Equations - self-consistently for the electrostatic potential and for the electron and hole concentrations, respectively. Then the DC characteristics of long-channel metal-gate/high-κ/GOI MOSFETs were simulated. (The device characteristics and process steps can be found in previous publications [4]-[5].) After achieving a good match with the DC data, we used the simulators to examine the scaled 0.18μm metal-gate/high-κ/GOI MOSFETs. The NF_{min} was obtained by using an analytical expression derived from circuit theory [12]-[14]. We note that a microstrip transmission line layout had been used for the RF measurements [12]-[13] rather than the conventional CPW layout, to screen the RF noise generated from the lossy Si substrate network [17]. The basic Ge data for simulation is shown below, in Table 1.

Table 1. Basic Ge data for TMA device simulation.

E_G (eV)	Affinity (eV)	Density of states m_n^*	Density (g/cm^3)	N_c (cm^{-3})	N_V (cm^{-3})
0.66	4.13	0.55 m_0	5.33	1×10^{19}	6×10^{19}

3. Results & Discussion

3.1 Long Channel GOI MOSFETs

Figure 1 shows the measured and simulated I_d -V_g characteristics for 10 μm long-channel metal-gate/high-κ/GOI nMOSFETs. For comparison, the I_d -V_g data for metal-gate/high-κ/Si devices are included. Good agreement was obtained between the measured and simulated data, including the modeling of the off-state leakage current. The Medici simulation suggests that the large leakage current is due to the small E_G of Ge, especially from the drain junction depletion region. The suppression of the leakage current can be achieved by using Ultra-thin Body (UTB) GOI [11] similar to Si MOSFET in the UTB SOI case. In addition, proper device design can reduce the off-state leakage current by more than an order of magnitude from that obtained from the Medici simulation.

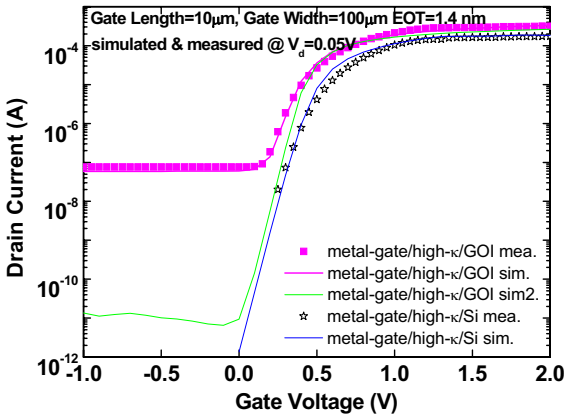

Figure 1: Comparison of the measured and simulated I_d -V_g data for metal-gate/high-κ/GOI nMOSFETs.

We show the measured and simulated I_d -V_d characteristics of metal-gate/high-κ on GOI MOSFETs in Fig. 2. For comparison the metal-gate/high-κ/Si MOSFET data is also included. The device had the same gate length and gate stack structure. The slight deviation of the drain current between the simulation and the measurements is due to the soft phonon scattering at low effective field. This is also shown in the deviation of the data, as a function of effective electric field, in Fig. 3. This is because soft phonon scattering is not included in the Medici simulation. However, good matching of the measured and simulated mobility data occurred at medium to high effective field region. The higher drain current of the GOI MOSFETs, compared with Si devices (Fig. 2), is due to the higher mobility of the GOI as depicted in Fig. 3. This improved mobility is important for the RF characteristics, as shown in the following sections.

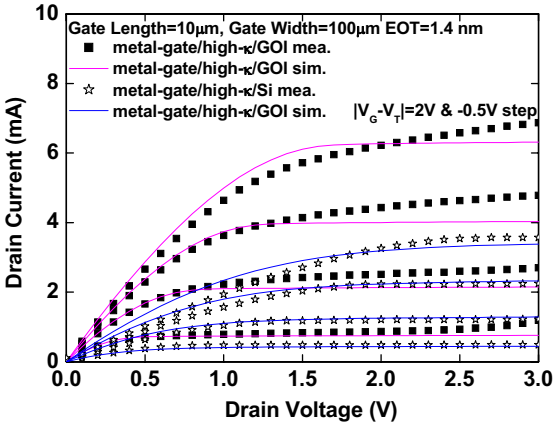

Figure 2: Measured and simulated I_d -V_d characteristics of metal-gate/high-κ/GOI nMOSFETs.

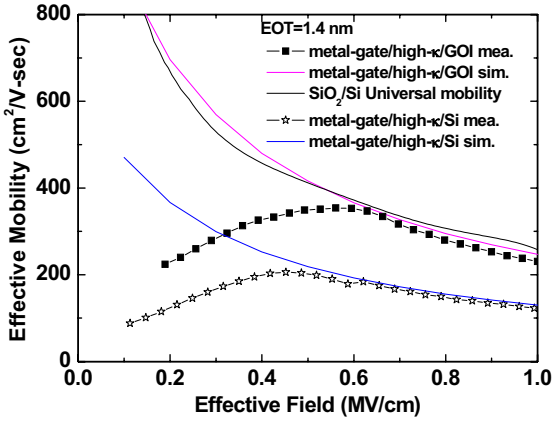

Figure 3: The measured and simulated effective mobility data for metal-gate/high-κ/GOI and metal-gate/high-κ/Si nMOSFETs.

3.2 0.18μm GOI vs. Si MOSFETs

Simulating the GOI devices with small channel lengths is important for predicting the device RF performance. We first calibrated the T-Supreme and Medici simulators with the standard multi-fingered 0.18μm Si MOSFETs obtained from a foundry. Figure 4 shows the measured and simulated I_d-V_d characteristics for 0.18μm poly-Si/SiO_2/Si MOSFETs. The good agreement between the measured and simulated data indicates that the process and device simulators are suitable for analyzing the DC characteristics of metal-gate/high-κ/GOI MOSFETs. Note that these 0.18μm devices have good current saturation since the device design included a pocket implant. Similar good I_d -V_d characteristics can also be obtained by such a device design approach in small energy bandgap GOI devices.

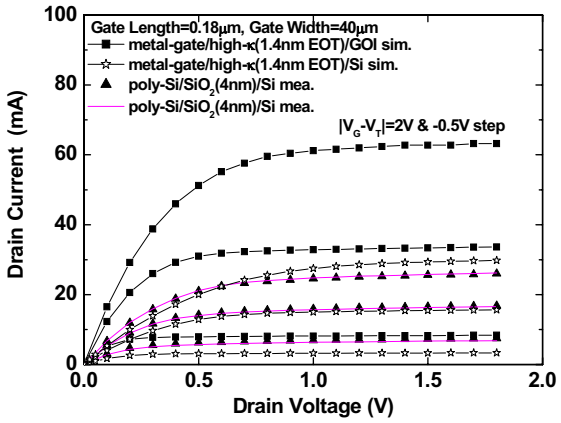

Figure 4: Comparison of the measured and simulated I_d-V_d data for 0.18μm Si MOSFETs. Good agreement helped calibrate the simulators for application to the 0.18μm metal-gate/high-κ/(GOI or Si) nMOSFETs.

We show, in Fig. 5, the $|H_{21}|^2$ current gain, obtained from S-parameters, as a function of frequency for 0.18μm MOSFETs. Good matching was obtained between the measured and simulated results for the poly-Si/SiO_2/Si MOSFET, indicating the excellent simulation results by T-Supreme and Medici. An f_t of 47 GHz was obtained from the extrapolation of a -20 dB/decade slope, which is typical for a conventional 0.18μm poly-Si/SiO_2/Si MOSFET.

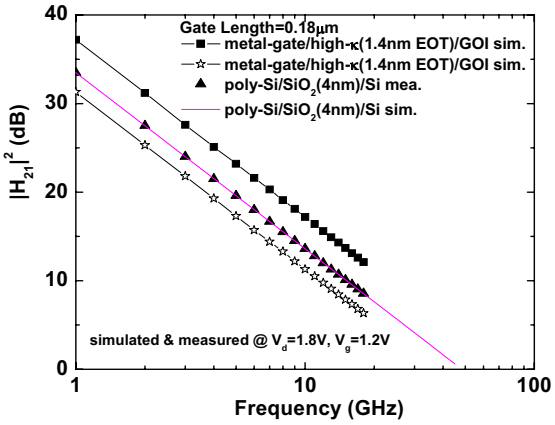

Figure 5: Measured and simulated $|H_{21}|^2$ gain as a function of frequency for 0.18μm Si MOSFETs. The $|H_{21}|^2$ of 0.18μm metal-gate/high-κ MOSFET was simulated following the successful matching of the simulated and measured data for the SiO_2/Si devices.

The measured NF_{min} for 0.18μm MOSFETs are shown in Fig. 6. The data were calculated from the following expression, derived from circuit theory [13]-[14]:

$$NF_{\min} = 1 + 2\gamma\left(1 + \frac{g_m R_g}{\gamma}\right)^{1/2} \frac{f}{f_t} \qquad \text{Eq. 1}$$

The f_t and g_m are given by the T-Supreme and Medici simulations. R_g is the parasitic resistance. Here γ is the drain current noise correlation factor - the ideal value of 2/3 was used. Good agreement was obtained between the simulation and measured NF_{min} for conventional 0.18μm poly-Si/SiO_2/Si MOSFETs. The good match between the measured and simulated DC I-V, S-parameters (not shown), $|H_{21}|^2$ and NF_{min} data indicates the success in simulating the 0.18μm poly-Si/SiO_2/Si MOSFET devices, using the approach of combining T-Supreme-Medici and the noise equation for analysis.

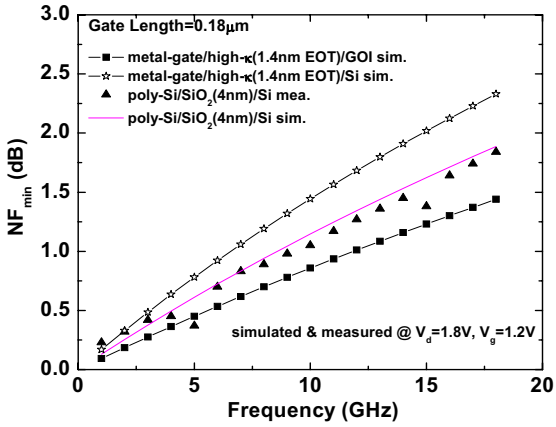

Figure 6: Measured and simulated NF_{min} as a function of frequency for 0.18μm MOSFETs. From the well-matched simulation and measured data for the poly-Si/SiO_2/Si device, the NF_{min} of 0.18μm metal-gate/high-κ/(GOI or Si) MOSFET can be calculated with confidence.

Following the good match between the simulated and measured data for the 0.18μm poly-Si/SiO_2/Si devices, we then simulated the DC to RF characteristics of the 0.18μm metal-gate/high-κ/GOI MOSFETs. The detailed process steps are similar to those for the Si device. However, the thermal budgets are much lower for GOI MOSFETs compared with the Si case. This helps reduce impurity diffusion which is required for sub-100nm devices. The low thermal budget is also suitable for metal-gate and high-κ gate dielectric integration, to prevent Fermi-level pinning and cause high threshold voltage (V_{th}).

For comparison, the simulated DC I_d -V_d , $|H_{21}|^2$ and NF_{min} of 0.18μm metal-gate/high-κ/(GOI or Si) MOSFETs are also shown in Figs. 4, 5 and 6, respectively. Good DC I_d -V_d characteristics were obtained, in addition to the higher saturation drive current, compared with metal-gate/high-κ/Si devices. The higher drive current reflects the fact that the electron mobility is higher in GOI than in Si, as shown in Fig. 3. This, in turn, is due to the smaller m^* of Ge. The drive current improvement is significantly higher than the 11%-13% obtained from strained Si [18]-[19] - this is the advantage of using GOI for mobility scaling beyond the

strained-Si case. The simulated 0.18μm metal-gate/high-κ/GOI MOSFETs show better RF performance - such as higher $|H_{21}|^2$ current gain and larger f_t - than their Si counterparts. The poorer RF $|H_{21}|^2$ gain and f_t of metal-gate/high-κ/Si compared with poly-Si/SiO_2/Si MOSFETs are due to the decreased mobility caused by soft-phonon scattering, see Fig. 3. This is one of the difficult challenges for metal-gate/high-κ technology.

The calculated NF_{min} of the metal-gate/high-κ/GOI MOSFET also shows a large improvement compared with its Si counterparts, over the whole frequency range from 1-18 GHz. This arises from the higher f_t shown in Fig. 5. At 10 GHz, required for Ultra-Wide Band (3.1-10.6 GHz) communications, the simulated NF_{min} is <1dB and close to that for III-V HEMTs. This has the same origin: the higher electron mobility and smaller m^* in both GOI and III-V semiconductors. Note that the simulated NF_{min} of the 0.18μm GOI MOSFET is comparable with the measured data for the 90nm node strained-Si MOSFETs, which have a 70-80nm gate length [20]. This also reflects the underlying higher mobility of GOI compared with strained Si.

4. Conclusions

We have simulated the characteristics of metal-gate/high-κ/GOI MOSFETs, from DC to radio frequencies. The T-Supreme and Medici simulators were calibrated using measured data for 0.18μm poly-Si/SiO_2/Si MOSFETs and used for long-channel metal-gate/high-κ/GOI devices. The improvements in the DC drive current, RF $|H_{21}|^2$ gain and NF_{min} for the GOI MOSFETs, compared with their Si counterparts, arise from the higher mobility. The simulated performance of metal-gate/high-κ/GOI MOSFET shows their potential to out-perform strained Si MOSFETs.

5. Acknowledgements

The authors at NCTU wish to thank Dr. G. W. Huang at the National Nano-Device Lab. (NDL) for his help with the RF measurements. This work was partially supported by NSC (92-2215-E-009-031) and the nano-project from the Nano-Science Tech. centre of Taiwan.

References:

[1] S. Thompson, *IEDM Tech. Dig.,* p. 591 Dec. 2003.
[2] H. Iwai, *IEDM Tech. Dig.,* pp. 11-16, Dec. 2004.
[3] M. Brillouët, pp. 17-24, Dec. 2004.
[4] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, *IEDM Tech. Dig.*, pp. 181-184, Dec. 2004.
[5] A. Chin and S. P. McAlister, IEEE Circuit & Devices Magazine, vol. 21, no. 1, pp. 27-35, Jan/Feb. 2005.
[6] C. H. Huang, D. S. Yu, A. Chin, W. J. Chen, C. X. Zhu, M.-F. Li, B. J. Cho, and D. L. Kwong, *IEDM Tech. Dig.*, pp. 319-322, Dec. 2003.
[7] C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, *Symp. on VLSI Tech. Dig.*, pp. 119-120, June 2003.
[8] X. Yu, C. X. Zhu, X. P. Wang, M. F. Li, Albert Chin, A. Du, W. D. Wang, D. L. Kwong, *Symp. on VLSI Tech. Dig.*, pp. 110-111, June 2004.
[9] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, *Symp. on VLSI Tech. Dig.*, pp. 16-17, June 2000.
[10] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, *Symp. on VLSI Tech. Dig.*, p.133-134, June 1999.
[11] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S.-I. Takagi, *Symp. on VLSI Tech. Dig.*, pp. 198-199, June 2004.
[12] H. L. Kao, Albert Chin, B. F. Hung, J. M. Lai, C.F. Lee, M.-F. Li, G. S. Samudra, C. Zhu, Z. L. Xia, X. Y. Liu and J. F. Kang, *Symp. On VLSI Tech. Dig.*, June 2005 (in press).
[13] H. L. Kao, Albert Chin, J. M. Lai, C. F. Lee, K. C. Chiang, and S. P. McAlister, *IEEE RF-IC Symp. Dig.*, June 2005 (in press).
[14] M. C. King, Z. M. Lai, C. H. Huang, C. F. Lee, M. W. Ma, C. M. Huang, Y. Chang and Albert Chin, *IEEE RF IC Symp. Dig.*, pp. 171-174, June 2004.
[15] M. C. King, M. T. Yang, C. W. Kuo, Y. Chang, and A. Chin, *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 6-11, June 2004.
[16] C. H. Huang, K. T. Chan, C. Y. Chen, A. Chin, G. W. Huang, C. Tseng, V. Liang, J. K. Chen, and S. C. Chien, *IEEE RFIC Symp. Dig.*, pp. 373-376, June 2003.
[17] A. Chin, K. T. Chan, H. C. Huang, C. Chen, V. Liang, J. K. Chen, S. C. Chien, S. W. Sun, D. S. Duh, W. J. Lin, C. Zhu, M.-F. Li, and S. P. McAlister, *IEDM Tech. Dig.*, pp. 375-378, Dec. 2003.
[18] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, M. Bohr; *IEDM Tech. Dig.*, pp. 978-980, December 2003.
[19] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Standford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson and M. Bohr, *Symp. on VLSI Tech. Dig.*, pp. 50-51 (2004).
[20] K. Kuhn, R. Basco, D. Becher, M. Hattendorf, P. Packan, I. Post, P. Vandervoorn and I. Young, *Symp. on VLSI Tech. Dig.*, pp. 224-225 (2004).