Single-Electron Emission of Traps in HfSiON as High-k Gate Dielectric for MOSFETs

C. T. Chan[1], C. J. Tang[1], C. H. Kuo[1], H. C. Ma[1], C. W. Tsai[2], H. C.-H. Wang[2], M. H. Chi[2], and Tahui Wang[1]

[1]Dept. of Electronics Engineering, National Chiao Tung University
[2]Taiwan Semiconductor Manufacturing Company, Science-Based Industrial Park, Hsin-Chu, Taiwan
e-mail: twang@cc.nctu.edu.tw

ABSTRACT

A novel method for characterizing MOSFETs with HfSiON high-k gate dielectric is demonstrated for the first time by direct measurement of single-electron de-trapping. Individual high-k trapped electron emission is recorded, which is manifested by the step-like evolution of channel current. The physical path of electron de-trapping can be identified from the emission time of such single-electron de-trapping. The dependence of charge emission time on gate voltage and temperature is measured. An analytical model based on thermally assisted tunneling can predict the emission time behavior, trap activation energy, trap density, and total available traps in high-k gate dielectric.

[*Keywords:* high-k gate dielectric, HfSiON, traps, single electron emission, thermally-assisted tunneling]

INTRODUCTION

As CMOS scaling continues with thinner gate oxides, the standby power increases to intolerable level as a result of direct tunneling current through the oxides. Thus, high dielectric constant (high-k) materials are emerging as a post-SiO_2 solution [1]. Recently, Hf-based silicate dielectric (HfSiON) has been successfully integrated in CMOS as gate dielectric (with EOT~1.5nm) for low power applications with good reliability, comparable mobility (to SiO_2), and greatly reduced gate leakage [2]. The characterization of high-k gate dielectric is usually performed by a charge pumping (CP) technique [3]. However, the resolution of CP is limited due to the mixture of interface traps and traps in high-k gate dielectric bulk.

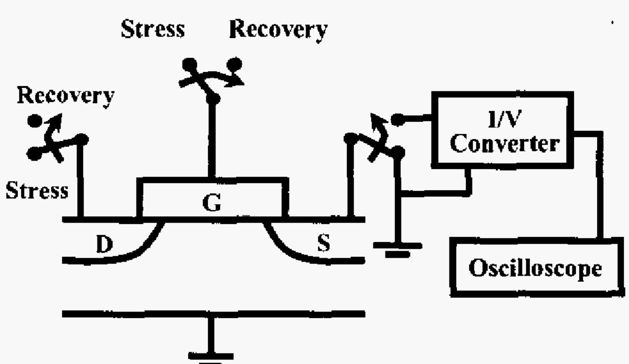

Figure 1. Experimental setup to measure high-k trapped charge emission times. In stress phase, V_g=0.7V, V_d=0V for 0.1s. In recovery phase, V_g=0.25~0.55V, and V_d=0.2V, and drain current temporal evolution is recorded by an digital oscilloscope. The high-speed switches minimize the delay between phase transitions down to μs.

In this study, we will demonstrate a novel technique for direct measurement of single-electron de-trapping in nMOSFETs with HfSiON gate dielectric [2]. Due to the discrete nature of trapped charge emission, the charge emission time can be clearly measured, and the physical path of de-trapping can be identified from the charge emission time. An analytical model based on tunneling can predict the behavior of electron emission, trap activation energy, trap density, and total available traps in high-k dielectric.

SINGLE-ELECTRON EMISSION TIME OF TRAPS IN HFSION

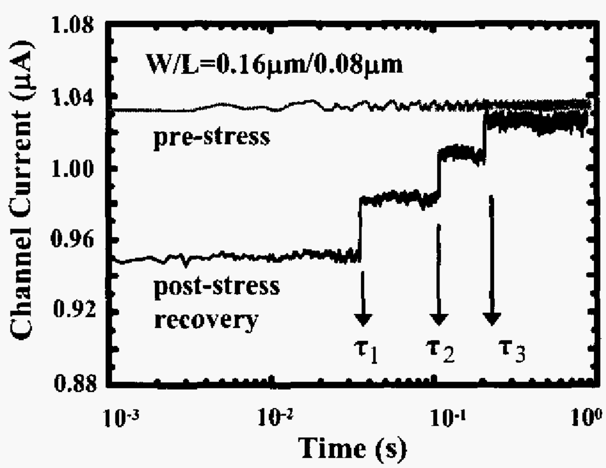

Figure 2. Pre- and post-stress current evolutions in a high-k nMOSFET with W/L=0.16μm/0.08μm.The measurement bias is V_g=0.3V and V_d=0.2V. Each current jump in the post-stress recovery corresponds to a single trapped charge escape from the high-k gate dielectric. Only three electrons are trapped during stress. The charge emission times in recovery phase are denoted by τ_1, τ_2, and τ_3 in the figure.

The trapped charge behavior in high-k gate dielectric is studied by "stress" and "recovery" as shown in Fig. 1, where the temporal evolution of drain current is recorded by a digital oscilloscope and the time delay during phase transition is minimized by high-speed switches down to μs. The transient measurement setup is tested on MOSFETs with SiO_2 as gate dielectric, stable I-t characteristics ensure that this method induces no spurious current transient. In "stress" phase, V_g is 0.7V for 100ms and electrons are injected and trapped into the high-k dielectric. In "recovery" phase, the drain current is measured with V_g (@ 0.25 - 0.55V) and V_d (@0.2V). The drain current of a small area post-stress nMOSFET (W/L= 0.16/0.08μm) (Fig.2) increases in steps and finally saturates to a level close to the pre-stress level (Fig. 2). In this study, each drain current step corresponds to a "single" electron de-trapping from the high-k dielectric. Interestingly, the time of occurrence for each electron de-trapping (i.e. τ_1, τ_2, and τ_3) (or referred to as emission time) increases with V_g applied in "recovery" (Fig. 3). Ten measurements of each V_g bias on the same device were made to take an average. Furthermore, as expected, the emission time of electron de-trapping is found to decrease at elevated temperature (Fig. 4). The extracted activation energy is about 0.18eV. The above data indicates the mechanism of electron trapping/de-trapping in high-k gate dielectric as discussed next.

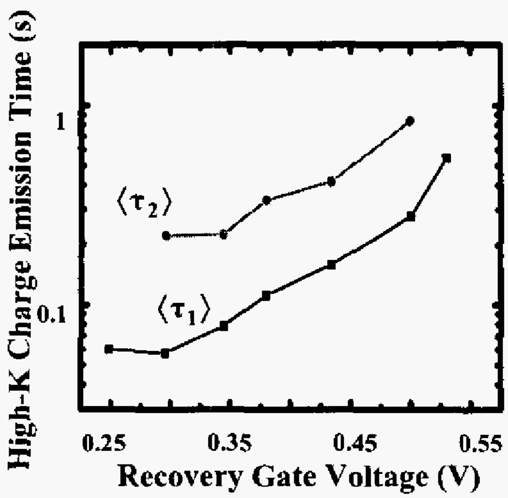

Figure 3. V_g dependence of averaged high-k trapped charge emission times $<\tau_1>$ and $<\tau_2>$ in recovery phase. Ten measurements on the same device are made to take average.

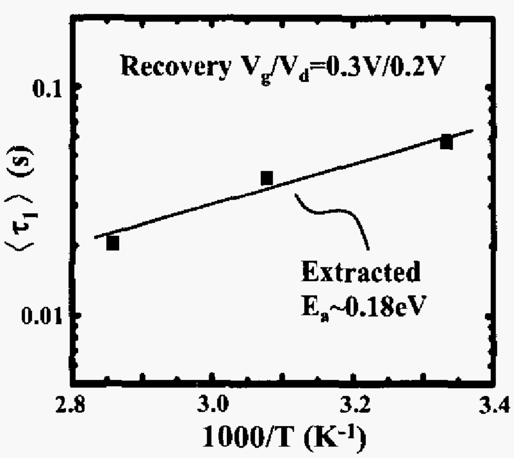

Figure 4. Temperature dependence of $<\tau_1>$. A straight line in the Arrhenius plot implies a thermal process is involved in trapped charge emission. The extracted activation energy is ~0.18eV.

RESULTS AND DISCUSSION

Trapped Electron Emission Mechanism

The observed longer electron emission time at larger V_g (Fig. 3) suggests the dominant path of charge emission toward Si substrate. There are three possible paths for electron de-trapping as illustrated in the energy band diagram in Fig. 5, i.e. Frenkel-Poole (F-P) emission (path a), SRH-like thermally-assisted-tunneling (TAT) (path b) [4-6] toward the gate electrode, and TAT toward the Si substrate (path c). The de-trapping path (a) is ruled out, since the activation energy for F-P mechanism should be equal to the trap energy, E_t (>1eV), and the extracted E_a is only 0.18eV. The de-trapping path (b) is ruled out too since a larger V_g would accelerate the electron emission toward the gate electrode resulting in a shorter emission time. The observed emission time is just the opposite (Fig. 3). Temperature dependence (Fig. 4) with extracted activation energy of 0.18eV confirms the role of thermal process in charge emission.

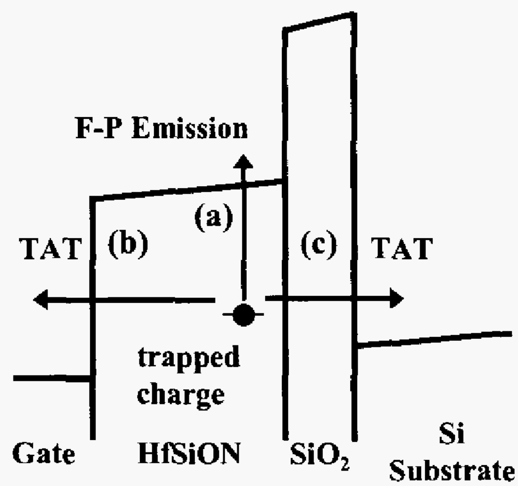

Figure 5. Energy band diagram in recovery phase. Various charge escape paths are illustrated: (a) Frenkel-Poole (F-P) emission, (b) thermally-assisted-tunneling (TAT) to the gate, and (c) TAT to the Si substrate. From V_g dependence and temperature dependence of charge emission time in Fig. 3 and Fig. 4, only (c) should be considered.

Analytical Model for Electron De-trapping

An analytical model of the TAT mechanism is developed with energy band diagram and trap distance illustrated in Fig. 6:

$$\tau_i^{-1} = \upsilon \exp(-\alpha_{ox}T_{ox})\exp(-\alpha_k x_i) \qquad \text{Eq.(1)}$$

where

$$\upsilon = [N_C(1-f_t)]\upsilon_{th}[\sigma_0 \exp(\frac{-E_a}{kT})] \qquad \text{Eq.(1a)}$$

$$\alpha_{ox} = \frac{2\sqrt{2m_{ox}^* q(E_t+\Phi_B)}}{\hbar}\ ;\ \alpha_k = \frac{2\sqrt{2m_k^* qE_t}}{\hbar} \qquad \text{Eq.(1b)}$$

Eq. (1) reveals the nature of tunneling for trapped electron emission time, τ_i. The pre-factor υ, a lumped parameter referred to as the "attempt-to-escape frequency" can be re-written as in Eq. (1a) [4] where N_C is the effective density-of-state in the Si conduction band, $N_C(1-f_c)$ is the amount of available states in Si substrate for out-tunneling electrons from high-k traps, σ_0 and E_a represent the trap cross-section and the activation energy. Other variables have their usual definitions. The Fermi-Dirac distribution (f_c) in the Si conduction band is a function of V_g in "recovery." A smaller recovery V_g leads to a lower surface carrier density (a smaller f_c) and thus a shorter electron emission time. As the recovery V_g drops below the threshold voltage (V_t), decrease in the emission time tends to saturates since f_c approaches zero. The electron nearest to the interface of Si substrate will be the first electron for de-trapping to occur. With respect to the temperature effect, a small recovery V_g (<0.25V), where f_c~0, was chosen for measurement of the trap activation energy, E_a, shown in Fig. 4. The extracted activation energy from the Arrhenius plot is 0.18eV.

High-k Trap Density and Total Available Traps

The high-k trap density can be evaluated through the analytical model, Eq. (1). By comparing

$$\tau_1 = \upsilon^{-1}\exp(\alpha_{ox}T_{ox})\exp(\alpha_k x_1)$$
$$\tau_2 = \upsilon^{-1}\exp(\alpha_{ox}T_{ox})\exp(\alpha_k x_2)$$

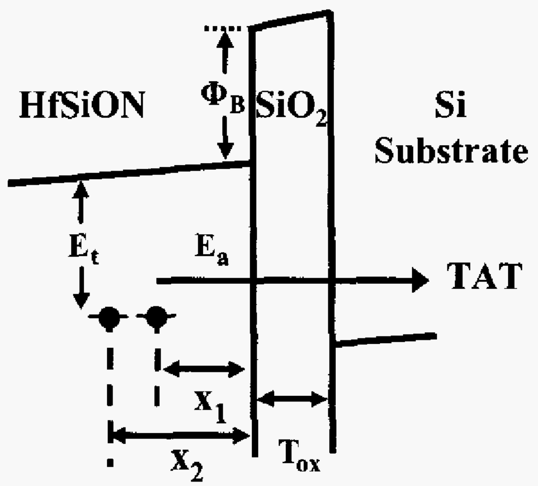

Figure 6. Schematic representation of gate dielectric band diagram in recovery phase and trap positions. E_a is the activation energy for TAT, and the proposed model is described in detail in the text.

we obtain

$$\frac{\tau_2}{\tau_1} = \exp[\alpha_k(x_2 - x_1)] \qquad \text{Eq.(2)}$$

and the high-k trap density (N_t) is readily calculated as

$$N_t = \frac{1}{(x_2 - x_1)WL} = \frac{1}{WL\frac{1}{\alpha_k}\ln\left(\frac{\tau_2}{\tau_1}\right)} \qquad \text{Eq.(3)}$$

Eq. (2) predicts that the ratio of emission times (e.g. τ_2 to τ_1) is only related to the physical distance of trap sites away from the interface. Figure 7 indeed shows the ratio of τ_2/τ_1 (10 readings of each gate bias on the same device) is constant and independent of recovery V_g. The average high-k trap density calculated from Eq. (3) (assuming m^*_k ~0.18m_0 [7]) is ~$3.5*10^{17}cm^{-3}$, or equivalently, an areal density of ~$8.8*10^{10}cm^{-2}$. This small trap density can hardly be resolved by CP due to a comparable interface trap density [3]. It should be pointed out that the extracted trap density, according to Eq. (3), is not affected by variables such as T_{ox}, m^*_{ox} and E_a. The total available number of traps in high-k gate dielectric of each device is related to high-k thickness, trap density, and transistor size. The observed 3 electrons trapped in the nMOS after the "stress" in this study are less than the total available traps (~10) as calculated from the estimated trap density and transistor size.

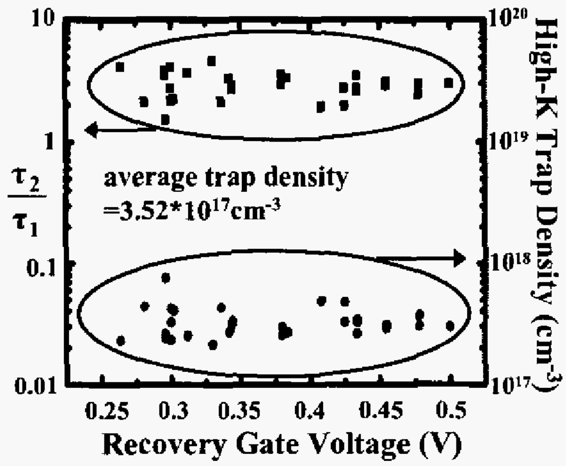

Figure 7. The ratio of τ_2 to τ_1 versus gate voltage in recovery phase. Note that τ_2/τ_1 remains almost unchanged with respect to Vg. The extracted high-k trap density from Eq.(2) is also given. Totally, 10 devices are measured in the figure.

Gate Length Effects

The experiment was conducted on devices with different gate lengths, 0.08μm, 0.14μm, and 0.22μm. It is found that while step-like current recovery traces due to single-electron de-trapping are still observed for all lengths, the amplitude of the drain current step (ΔI_d) decreases with longer gate lengths, as shown in Fig. 8. This trend is consistent with the Random Telegraph Signal theory [8] and implies that the impact of the trapped electron in the high-k dielectric spreads over the entire channel. Thus, a single-electron emission can be observed only when the device size is small enough and the high-k is clean enough!

CONCLUSIONS

Single electron emission in HfSiON gate dielectric is observed. The emission times can be used to identify the de-trapping mechanism. The extracted high-k trap density and trap activation energy from this method is around ~$3.5*10^{17}cm^{-3}$ and 0.18eV, respectively. The proposed technique is a powerful tool to characterize trap in high-k gate dielectric for advanced CMOS.

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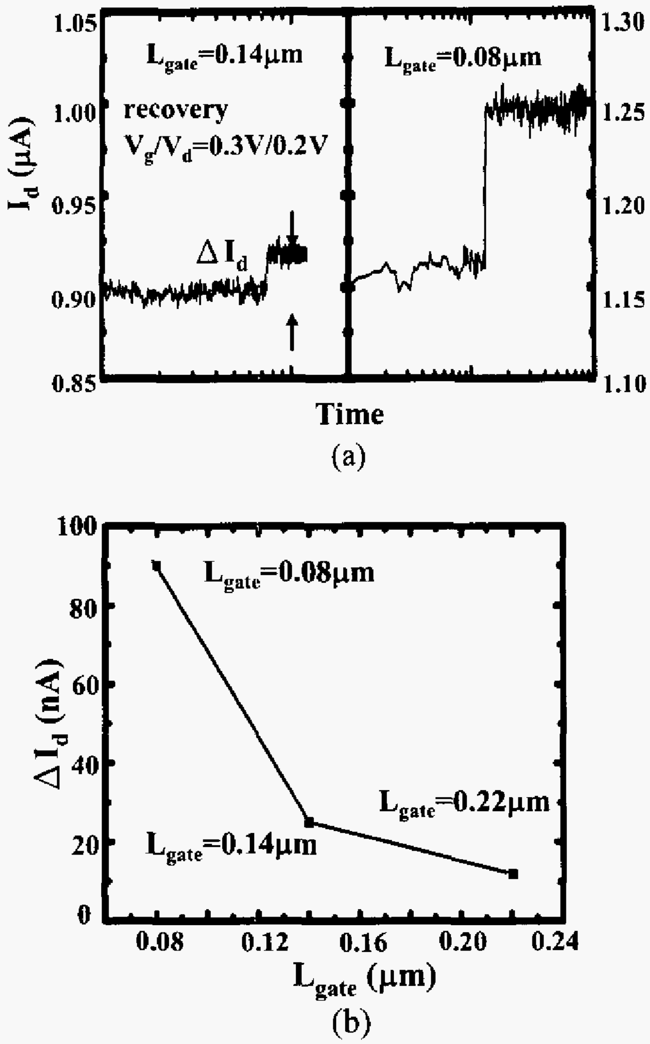

Figure 8. (a) Comparison of the current jump amplitude for L_{gate}=0.08μm and for L_{gate}=0.14μm. (b) The amplitude of charge escape induced current jump versus L_{gate}.

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