LOW FREQUENCY NOISE DEGRADATION IN ULTRA-THIN OXIDE (15Å) ANALOG n-MOSFETS RESULTING FROM VALENCE-BAND TUNNELING

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ABSTRACT

Abnormal increase of low frequency flicker noise in analog n-MOSFETs with gate oxide in valence band tunneling domain is investigated. In 15Å oxide devices, valence-band electron tunneling from Si substrate to poly-gate occurs at a positive gate voltage and results in the splitting of electron and hole quasi Fermi-levels in the channel. The excess low frequency noise is attributed to electron and hole recombination at interface traps between the two quasi Fermi-levels. The trap capture and emission times in valence band tunneling domain are extracted from random telegraph signal. The dependence of measured trap times on gate voltage is consistent with our proposed model. [*Keywords:* flicker noise, n-MOSFET, valence-band tunneling, trap emission and capture times, random telegraph signal.]

INTRODUCTION

CMOS technology is finding more and more important applications in the area of mixed mode and RF ICs. However, MOSFETs are notorious for flicker noise in the low frequency range. Drain current flicker noise has become one of the key considerations in device geometrical scaling since it will affect the signal-to-noise ratio in operational amplifiers and in analog/digital and digital/analog converters. In addition, low frequency flicker noise can be up-converted to undesired phase noise in RF circuits [1].

Low frequency flicker noise in MOSFETs with relatively thick gate oxides has been extensively studied. A unified noise model [2] based on oxide charge tunnel trapping and de-trapping has been adopted. The carrier number and mobility fluctuation induced from trapped oxide charges is thought to be the source of flicker noise. In addition, some studies showed that the low frequency noise may result from charge emission and capture at interface traps in weak inversion condition or in the very high frequency regime of noise power spectral density. As gate oxide thickness is scaled into direct tunneling domain, oxide trap density should be much reduced. In addition, channel electrons would likely tunnel through an ultra-thin gate oxide directly without being captured by oxide traps. However, the low frequency noise in ultra-thin oxide CMOS devices still exhibits a significant level [3]. The traditional oxide charge tunnel trapping and de-trapping concept seems no longer suitable to explain the noise behavior in ultra-thin oxide MOSFETs.

In addition to the noise behavior in frequency domain, we also investigate the noise behavior in time domain. The time domain presentation of low frequency noise is known as random telegraph signal (RTS) and has been extensively studied in past decades [4,5]. Due to a single charge trapping and de-trapping in a small area device, RTS exhibits two levels. The upper level corresponds to an empty trap, i.e., no electron occupation, and the duration of time is denoted by τ_H. The lower level corresponds to an electron occupied state and is denoted by τ_L. In many cases, τ_H corresponds to the time it takes to capture a carrier, while carrier release (emission) from traps governs τ_L.

In this study, the low frequency noise in a 15Å gate oxide n-MOSFET is investigated in time and frequency domain. The electron trapping and de-trapping times (τ_H and τ_L) are characterized from RTS in a small area n-MOSFET. The normalized noise power spectral density (S_{id}/I_d^2) is measured as a monitor of drain current noise, which is considered as a fair index because of the normalization to the drain current. In addition, the normalized noise power spectral density in n-MOSFETs with different gate oxide thickness is characterized for comparison. The drain bias in RTS and noise measurement in this study is 0.1V to ensure a uniform charge distribution in the channel. Finally, a new noise source due to valence band electron tunneling will be proposed to explain observed noise behavior.

RESULTS AND DISCUSSION

In order to find out the real cause of low frequency noise in n-MOSFETs in valence band tunneling domain, the trap time constant behavior in both frequency and time domain is analyzed. First of all, the frequency domain noise characteristic in an ultra-thin oxide n-MOSFET due to a single trap is investigated. Fig. 1 shows the measured and calculated noise power spectral density in a small area (W/L=0.16μm/0.12μm) n-MOSFET at Vg=1.1V.

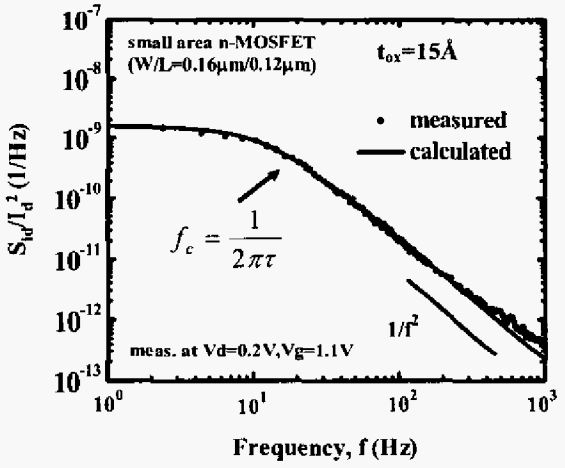

Fig. 1 Measured and calculated Lorentzian-like noise power spectral density of a small area n-MOSFET. The noise is measured in strong inversion.

The noise has a Lorentzian-like distribution, characterized by a constant power spectral density at low frequencies and a roll-off with f^{-2} at high frequencies [5]. The cut-off or corner frequency (f_c) corresponds to the 3-dB point of the spectrum and is related to the

reciprocal characteristic time (τ) of the underlying trap ($f_c=1/2\pi\tau$). The calculated result is based on the τ ($1/\tau=1/\tau_H+1/\tau_L$) extracted from associated RTS (will be shown later) and is in good agreement with the measured power spectral density.

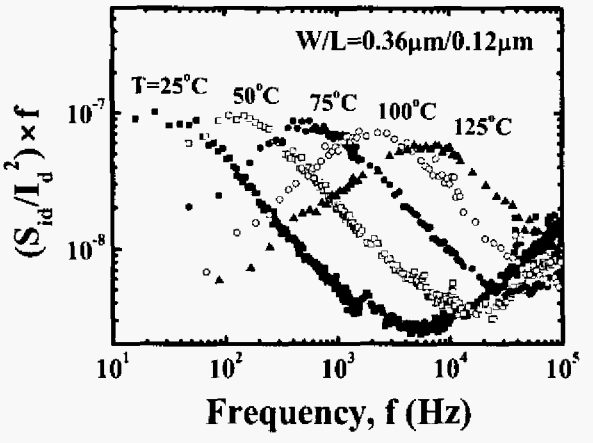

Fig. 2 Temperature dependence of the Lorentzian noise in a small area n-MOSFET (W/L= 0.36μm/0.12μm) with an oxide thickness of 15Å.

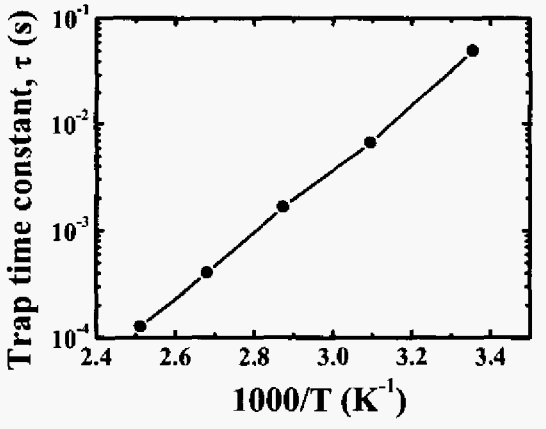

Fig. 3 Arrhenius plot of τ versus 1000/T.

Next, the temperature dependence of single trap time constant in ultra-thin oxide n-MOSFET is then investigated. Fig. 2 shows the temperature dependence of $(S_{id}/I_d^2)\times$frequency versus frequency. The temperature varies from 25°C to 125°C. Obviously, as temperature increases, the trap time constant decreases, resulting in a higher corner frequency. According to the Shockly-Read-Hall theory, the carrier capture time (τ) can be described by Eq. (1),

$$\tau = \frac{1}{N\sigma_0 \upsilon_{th}} \cdot \exp\left(\frac{\Delta E_b}{kT}\right) \qquad (1)$$

where ΔE_b is the energy barrier for the capture of a carrier and N is the carrier density in the vicinity of the trap. σ_0 is the capture cross-section. The linear behavior of the Arrhenius plot [6] shown in Fig. 3 reveals that the source of the noise is related to carrier capture/emission by interface traps. Although we cannot completely exclude the possibility that the traps for carrier capture/emission are in the silicon depletion region, it should be noted that the Si substrate trap density in bulk MOSFETs is around 10^8 cm^{-2} [7] by assuming a depletion width of 10nm. This number is quite small, as compared to interface trap density ~10^{10} cm^{-2}. Thus, the probability that the traps are in the depletion region is very small, only one hundredth.

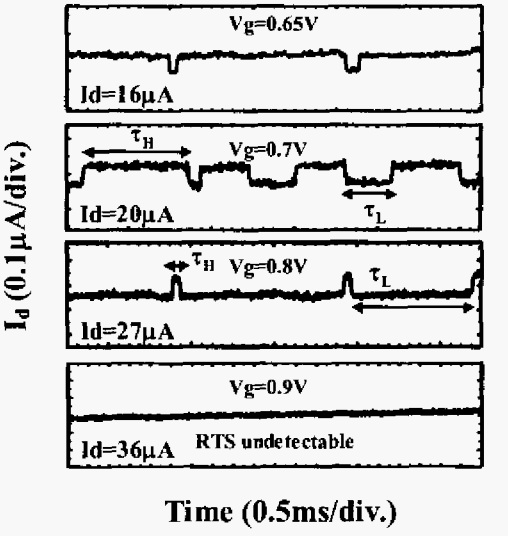

Fig. 4 The characteristics of two-level RTS at various gate voltages (in weak inversion) in a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å). RTS is undetectable at Vg=0.9V.

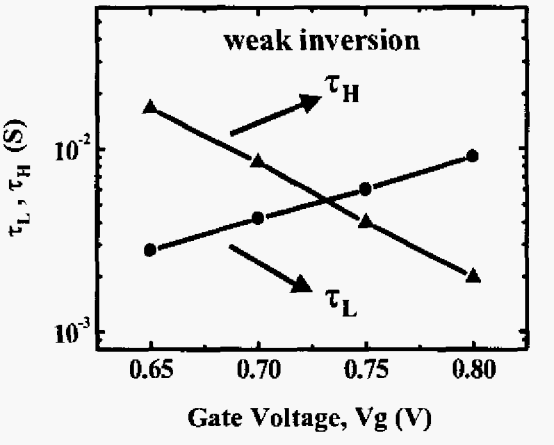

Fig. 5 Average τ_L and τ_H (extracted from RTS) versus gate voltage in weak inversion regime.

In addition, the single trap time constant behavior in time domain is also characterized through RTS measurement. Furthermore, significant substrate current is noticed in the 15Å oxide device, as the gate bias is larger than one volt because valence band electron

tunneling from the Si substrate to the poly-gate occurs and generated holes in the channel flow to the substrate.

The gate bias (Vg) dependence of corresponding RTS is then investigated. Fig. 4 shows typical RTS patterns in a small area n-MOSFET in weak inversion (Vg<0.9V). As can be seen, τ_L increases and τ_H decreases as Vg increases from 0.65V to 0.9V. Noticeably, RTS vanishes at Vg=0.9V in our measurement period. Fig. 5 shows the Vg dependence of average τ_L and τ_H (extracted from RTS).

The τ_L and τ_H in weak inversion correspond to the electron emission and capture times at the interface trap E_{tl}, as illustrated in Fig. 6. As Vg increases, τ_H decreases and τ_L increases because of a larger channel electron population and thus a smaller electron capture time. Our result here is consistent with the findings for thicker gate oxides in previous publications [4].

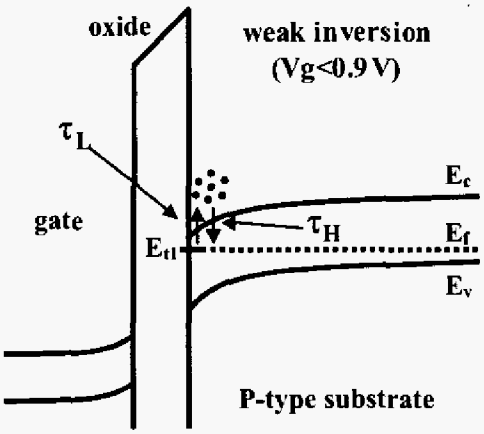

Fig. 6 RTS in weak inversion condition. The RTS results from electron capture (τ_H) and electron emission (τ_L) at interface trap E_{tl}.

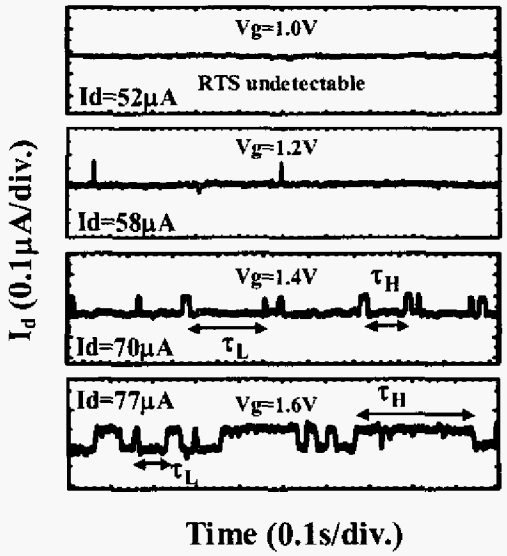

Fig. 7 The characteristics of two-level RTS at various gate voltages (in strong inversion regime) in a small area n-MOSFET (W/L=0.16μm/0.12μm, t_{ox}=15Å).

In contrast, Fig. 7 shows the RTS patterns in strong inversion from Vg=1.0V to 1.6V. The RTS is still undetectable at Vg=1V and re-appears for Vg>1V. Fig. 8 shows the Vg dependence of average τ_L and τ_H extracted from the RTS. Interestingly, we find that the RTS patterns in strong inversion (Vg>1V) exhibit an opposite trend. The Vg dependence of τ_L and τ_H in strong inversion is opposite to that in weak inversion.

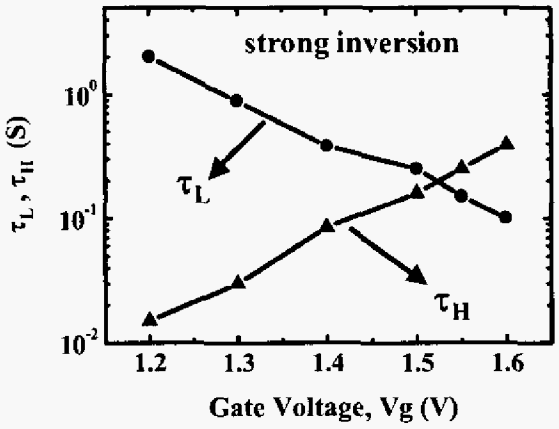

Fig. 8 Average τ_L and τ_H (extracted from RTS) versus gate voltage in strong inversion regime.

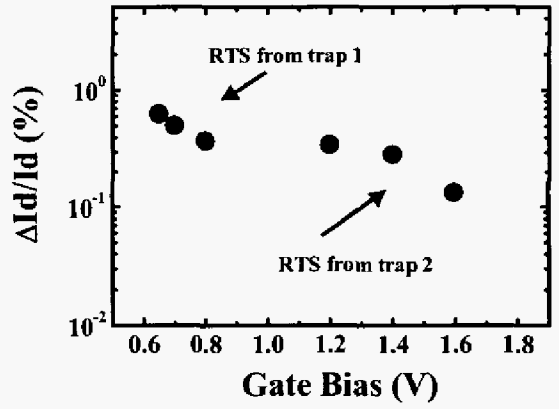

Fig. 9 $\Delta I_d/I_d$ versus the entire range of our measurement gate bias. The $\Delta I_d/I_d$ is extracted from the RTS patterns.

Although the mobility fluctuation theory [8] also can explain the abnormal gate bias dependence of τ_H and τ_L in our findings, further analysis shows that number fluctuation should dominate in the entire range of our measurement gate bias. Our reason is that the measured $\Delta I_d/I_d$ decreases with gate voltage (Fig. 9) and doesn't change sign, as expected from [8]. Thus, the explanation of mobility fluctuation should be excluded for our result.

In order to find out the cause of the opposite charge trapping and de-trapping behavior from weak inversion to strong inversion, the trap electron occupation factor (f_t) is analyzed. The f_t can be evaluated as $\tau_L/\tau_L+\tau_H$.

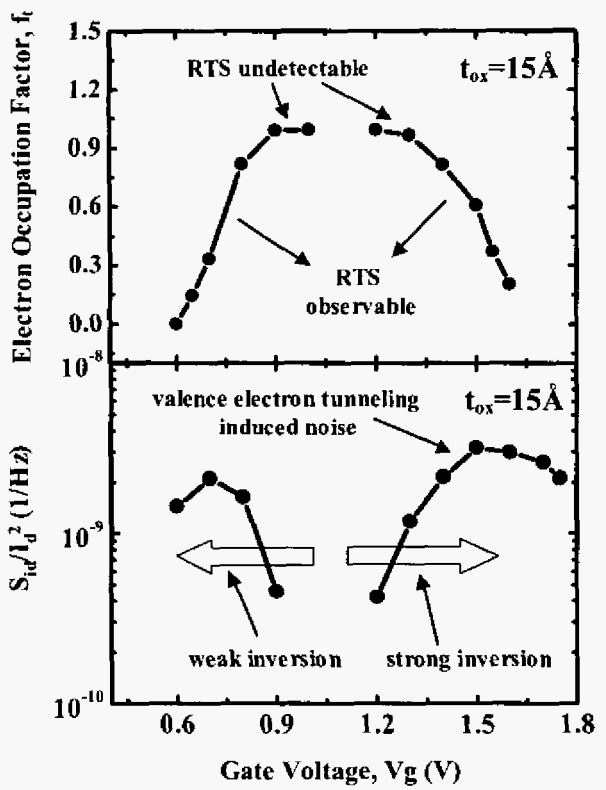

Fig. 10 The electron occupation factor (f_t) and normalized noise power spectrum density versus gate voltage in a small area n-MOSFET (W/L= 0.16μm/0.12μm, t_{ox}=15Å). The second noise peak in strong inversion is due to valence-band electron tunneling.

Fig. 10 shows f_t versus Vg from weak inversion to strong inversion. In weak inversion regime (i.e., Vg<0.9V), f_t increases with Vg because of an increased channel electron population. As f_t increases to 1, RTS is undetectable since the trap is always occupied by an electron. In strong inversion regime (i.e., Vg>1V), f_t declines from unity with increasing Vg. This means, at a larger Vg, although the energy level of the interface trap is deeper with respect to the electron Fermi level, the chance of the trap being occupied by an electron becomes smaller. This result is contrary to the equilibrium case that f_t should increase as the trap energy becomes more negative with respect to the Fermi level. In other words, the Si channel should be in non-equilibrium condition.

In addition to f_t, Fig. 10 also shows the S_{id}/I_d^2 (measured at f=100Hz in a small area n-MOSFET) from weak inversion to strong inversion. The S_{id}/I_d^2 has a peak around f_t ~0.5 for Vg from 0.6V to 1V. As f_t approaches unity, the RTS vanishes and the S_{id}/I_d^2 reduces because electrons always occupy the trap. However, the f_t begins to decrease as valence band electron tunneling occurs (Vg>1V). Thus, the RTS re-appears and the S_{id}/I_d^2 reaches another peak.

The possible explanation for the abnormal noise behavior in strong inversion is illustrated in Fig. 10. In strong inversion regime, a large Vg causes strong valence electron tunneling and leaves more holes behind in the channel. τ_H and τ_L then correspond to electron capture time and hole capture time respectively, as illustrated in Fig. 11. Because of the increased channel hole concentration at a larger Vg, τ_L is smaller. The non-equilibrium carrier distribution also results in the splitting of electron and hole quasi Fermi-levels. An interface trap (E_{t2}) between the two quasi Fermi levels serves as the recombination center of electrons and holes. Thus, the local electron concentration in the vicinity of the trap is reduced and τ_H increases. The increase of τ_H and the decrease of τ_L lead to a reduced f_t. The second peak of S_{id}/I_d^2 in strong inversion condition (Vg>1V) in Fig. 10 therefore can be well explained.

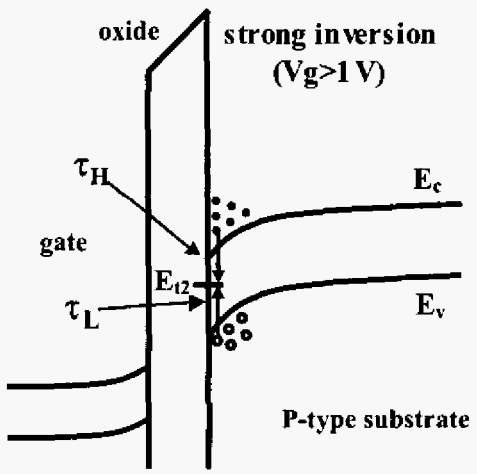

Fig. 11 RTS in weak inversion condition. The RTS results from electron capture (τ_H) and hole capture (τ_L) at E_{t2}.

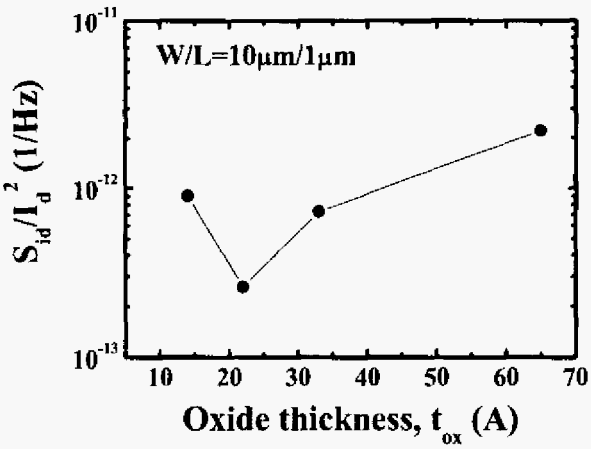

Fig. 12 Normalized noise power spectral density (measured at Vd=0.2V, Vg-overdrive=0.7V, f=100Hz) versus gate oxide thickness in n-MOSFETs (W/L=10μm/1μm).

Finally, the low frequency noise in a large area transistor with different gate oxide thickness is compared. Fig. 12 shows the gate oxide thickness dependence of the normalized noise power spectral density at f=100Hz. Due to the statistical nature of flicker noise, devices with too small area may exhibit a large fluctuation range in noise [9]. Therefore, the measured devices have a large area (W/L=10μm/1μm) and each noise measurement data point represents

an average of 5 devices. The noise is measured in the linear operation region (Vd=0.2V, Vg-overdrive=0.7V) to make sure the carrier distribution along the channel is uniform. As shown in Fig. 12, the S_{id}/I_d^2 decreases as the gate oxide thickness reduces from 65Å to 22Å. However, as gate oxide thickness continuously scales down, an abnormal increase in noise level appears, and the results is consistent with our proposed model.

CONCLUSION

Low frequency noise degradation in 15Å gate oxide n-MOSFETs is observed in strong inversion condition. A new generation/ recombination noise mechanism through interface traps is proposed in such thin gate oxide devices. The analysis of RTS patterns reveals that the increased channel hole concentration and a Fermi-level splitting due to valence-band electron tunneling is responsible for the noise behavior in ultra-thin oxide n-MOSFETs.

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