Suppression of Boron Penetration in BF_2-Implanted P-type Gate MOSFET by Trapping of Fluorines in Amorphous Gate

Chih-Yung Lin, *Student Member, IEEE*, Chun-Yen Chang, *Fellow, IEEE*, and Charles Ching-Hsiang Hsu, *Member, IEEE*

Abstract—**This work reports the use of amorphous/polysilicon gate electrode in BF_2-implanted poly-gated P-MOSFET's to suppress the boron penetration. SIMS analysis clearly illustrates that fluorine prefers to accumulate in the layer of amorphous silicon. The retardation of boron diffusion is therefore achieved by the trapping of fluorine in the amorphous layer of stacked amorphous/polysilicon (SAP) p-type gate due to a lower diffusion rate of fluorine in the amorphous silicon layer. Polysilicon depletion effect did not become more severe by introducing the amorphous silicon. In addition, gate oxide reliability is not degraded by using this gate structure. Results show that the structure is a promising gate electrode for future dual-poly gate CMOS technology development.**

I. Introduction

P+ poly-gate technology becomes indispensable for P-MOSFET as the CMOS devices continue to be scaled down to deep-submicrometer regime. The p^+ poly-gate surface channel device can reduce the short-channel effect compared to the buried channel n^+ poly-gate P-MOSFET [1]. However, the penetration of boron impurities from the p^+-doped electrode through the thin gate oxide into the channel region is a critical issue [2]–[4]. Furthermore, boron penetration is aggravated when annealed in the presence of hydrogen [2], [5], [6] or fluorine [3], [4]. We can eliminate the effect of hydrogen on the boron penetration by avoiding the presence of hydrogen after p^+ poly doping in the annealing furnaces. However, fluorine is incorporated in several processes which are needed for P-MOSFET, such as tungsten silicide deposition, BF_2 implantation for p^+ source/drain and gate during the P-MOSFET fabrication. Boron penetration then becomes a major issue in the fabrication of deep submicrometer PMOS device with p^+ poly-gate. The boron penetration can cause the shifts of flatband voltage (V_{FB}), the distortion of capacitance-voltage (C–V) curves, the increase of subthreshold swing (S) and leakage current, and the deterioration of the gate oxide quality. Therefore, boron penetration should be eliminated to keep the desired performance of the surface-channel device.

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C.-Y. Lin and C.-Y. Chang are with the National Nano Device Laboratory and Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan.

C. C.-H. Hsu is with the Microelectronics Laboratory, Semiconductor Technology & Application Research (STAR) Group, Department of Electrical Engineering, National Tsing-Hua University, Hsinchu, Taiwan.

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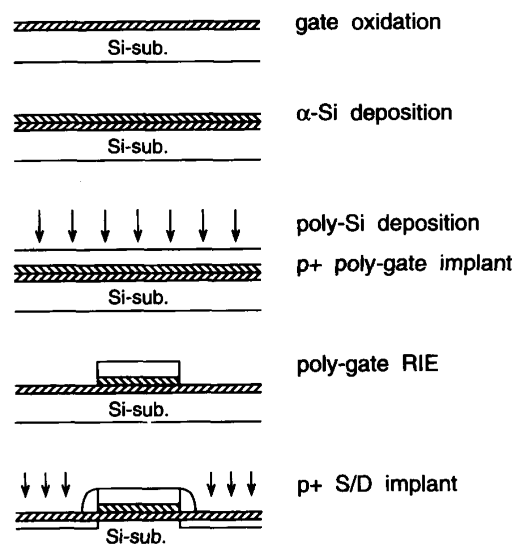

Fig. 1. Fabrication process sequence for SAP p^+ poly-gate P-MOSFET process.

Various approaches have been proposed to suppress the boron penetration [7]–[18]. Most of the previous studies in the literature [7]–[14] reported that thermally nitrided gate oxide or reoxidized nitrided oxide in NH_3 or N_2O ambient can act as a good diffusion barrier for boron penetration. However, a higher thermal budget is required for N_2O nitrided oxide due to the low nitridation rate. Furthermore, the nitridation process in NH_3 gas introduces a large number of electron traps [19] and a relatively high fixed positive charge density [20], [21]. These traps and oxide charges result in threshold voltage shift, mobility degradation, and reduced stability under electrical stress. Although to reoxidize the nitrided oxide at high temperature can improve dielectric properties by reducing the density of electron traps, such a high temperature step may not be desirable for future deep-submicrometer CMOS process. Instead of such a nitrided oxide, another approach is to modify the structure of the poly-gate, such as larger grain size formed by as-deposited amorphous silicon [16], [18], and stacked amorphous silicon film [17] to suppress the boron penetration. Less boron penetration is due to suppression of fluorine and boron diffusion in as-deposited amorphous silicon gate and a longer diffusion path in the stacked amorphous silicon layers. However, polysilicon depletion effect [22] and

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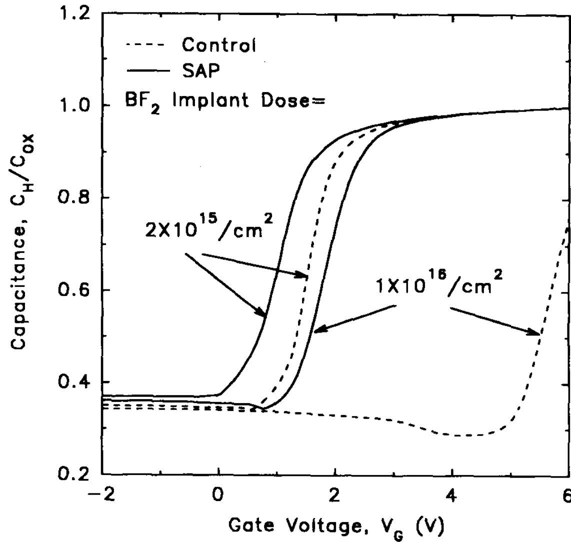


Fig. 2. High frequency C-V curves for p^+ poly-gate PMOS capacitors.

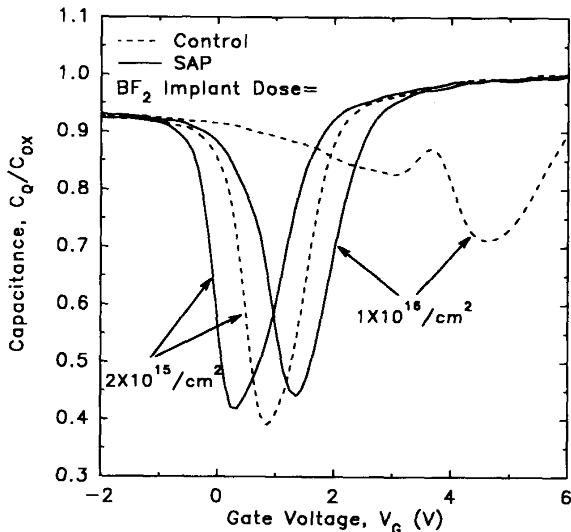


Fig. 3. Quasi-static C-V curves for p^+ poly-gate PMOS capacitors.

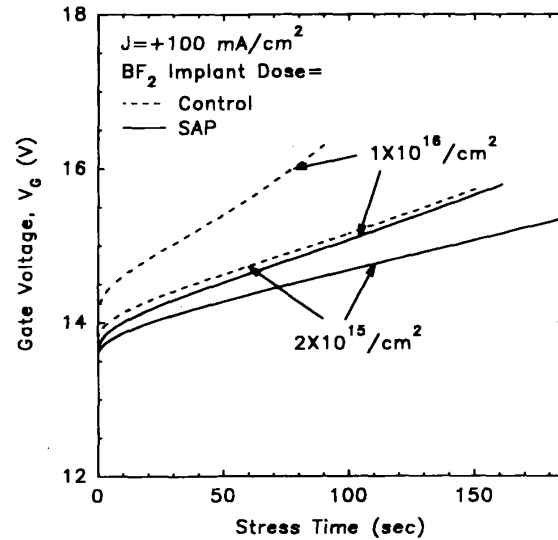


Fig. 4. Fowler–Nordhiem stress results for p^+ poly-gate PMOS capacitors. The gate voltage is plotted as a function of stress time with a constant currepnt density of +100 mA/cm^2.

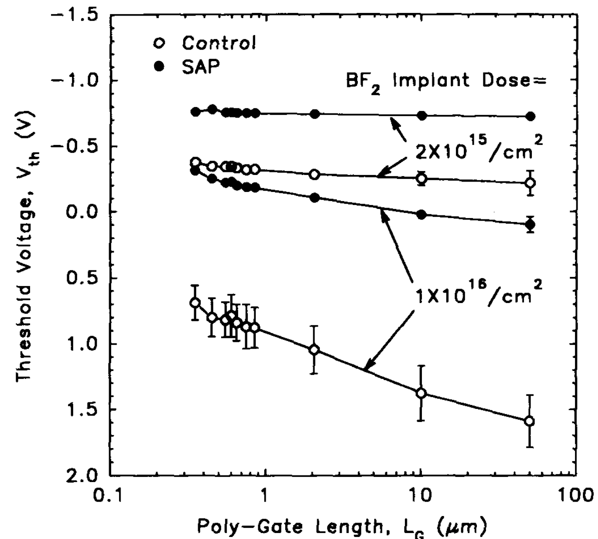


Fig. 5. Measured PMOS threshold voltage as a function of the poly-gate length. The threshold voltage was determined by the extrapolation on the V_G axis of the linear $I_D - V_G$ slope at the maximum transconduction (at $V_D = -0.1$ V) in the $I_D - V_G$ plot.

higher gate resistance may be resulted from such multi-stacked structure, and the performance of dual-gate CMOS devices is degraded accordingly.

In this paper, we propose a new gate structure which is composed of an as-deposited polysilicon layer as a top-layer and a thin as-deposited amorphous silicon layer as a bottom-layer to suppress the boron penetration and avoid the polysilicon depletion effect.

II. Device Fabrication

P^+ poly-gated PMOS capacitors (area = 2×10^{-4} cm^2) and P-MOSFET's were fabricated using boron doped (100)-oriented substrates with resistivity of 15–25 Ω-cm by employing conventional CMOS twin-well technology. The n-well was formed by phosphorus ion implantation and high temperature drive-in to adjust the surface concentration to 5×10^{16} cm^{-3}. Double channel implants were formed by As and Phosphorus to adjust the threshold voltage to about −0.8 V. After LOCOS and active area definitions, a thin gate oxide (11 nm) was thermally grown in dry oxygen and hydrogen chloride at 900°C. In this work, the p^+ poly-gate of the present structure which is referred to as "the SAP structure" is formed by first depositing a 500 Å amorphous silicon and then depositing a polysilicon layer to a total thickness of 3000 Å. Poly-gate composed of only a 3000 Å polysilicon layer was also fabricated as a control sample. The amorphous silicon and

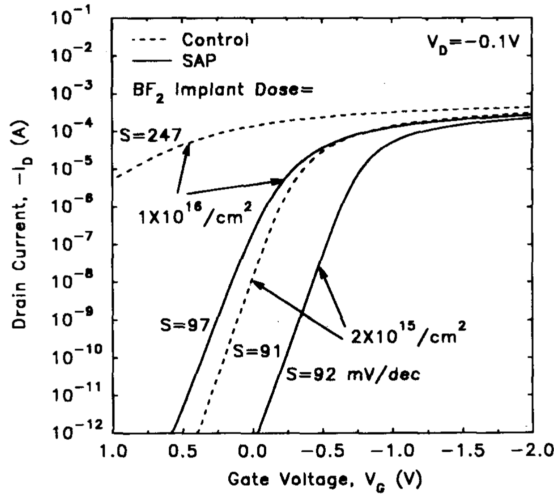


Fig. 6. Measured subthreshold characteristics of 0.35 μm drawn PMOS transistors.

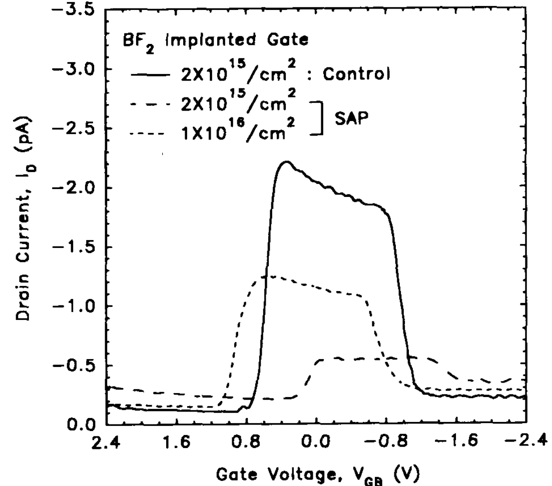


Fig. 8. Measured leakage current of the gated-diode as a function of gate voltage for control and SAP samples.

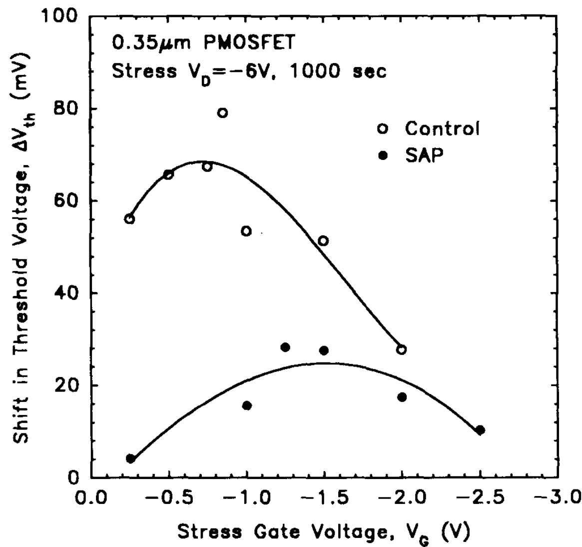


Fig. 7. P-MOSFET's device degradation in threshold voltage shift after channel hot-carrier stress versus stress gate voltage. P-MOSFET's were stressed at $V_D = -6$ V and at different V_G for 1000 sec.

polysilicon were deposited in a LPCVD furnace at 550°C and 620°C, respectively. P^+ poly was doped by various doses of BF_2 implantation at 50 KeV and annealed by the rapid thermal anneal (RTA) at 1000°C for 30 sec prior to poly-gate etch. After the gates had been patterned and etched, p^- LDD (lightly-doped drain) implantation with BF_2 was employed and APCVD oxide spacers were formed. P^+-doped source/drain were implanted with BF_2 at 55 KeV with doses of 2×10^{15} cm^{-2} through a thin sacrificial thermal oxide grown at 900°C. After BPSG deposition and densification at 900°C, contacts were defined. Then, the plug implantation was employed, and the samples were annealed at 900°C followed by metal-1 metalization and sintering at 400°C for 30 min. The fabrication process flow of the SAP poly-gate structure is illustrated in Fig. 1.

III. Results and Discussion

A. P^+-poly Gated MOS Capacitors

High frequency C–V and quasi-static C–V analyses are performed on PMOS capacitors for examining the boron penetration phenomena. All C–V curves were measured from inversion to accumulation in order to reduce spurious effects due to inversion-layer response time [23]. Fig. 2 shows the high-frequency (100 KHz) C–V curves for PMOS capacitors with BF_2-implanted dose of 2×10^{15} cm^{-2} and 1×10^{16} cm^{-2} for the two types of gate structures, respectively. It is shown that there is much less positive threshold voltage shift for the SAP samples than control samples as the implanted dose increasing from 2×10^{15} cm^{-2} to 1×10^{16} cm^{-2}. This indicates that less boron penetration occurs for the SAP structure. Due to a shallow boron doped layer resulted from boron penetration beneath the gate oxide, as modeled by Pfiester *et al.* [3], a slightly smaller minimum capacitance is observed for the boron-penetrated samples. This shallow p-layer creates an additional p-n junction depletion capacitance in series with oxide capacitance and channel depletion layer capacitance. Thus the C–V characteristics are modified. Similar C–V analysis has been done by Sigmon and Swanson [24] for ion-implanted p-channel MOS devices. Fig. 3 shows the effects of implanted dose on quasi-static C–V curves of the p^+ poly-gate MOS capacitors. The $C_{inv}/C_{\max}$ ratios are close to unity (≈93%) for both types of gate structures, indicating negligible polysilicon depletion effect resulted from the underlaid amorphous silicon layer. Furthermore, a distortion of quasi-static C–V curve in the strong inversion region is observed for the control sample with BF_2 implanted dose of 1×10^{16} cm^{-2}. This distortion has also been observed by Pfiester *et al.* [3] and Lo *et al.* [25], respectively. As reported by Lo

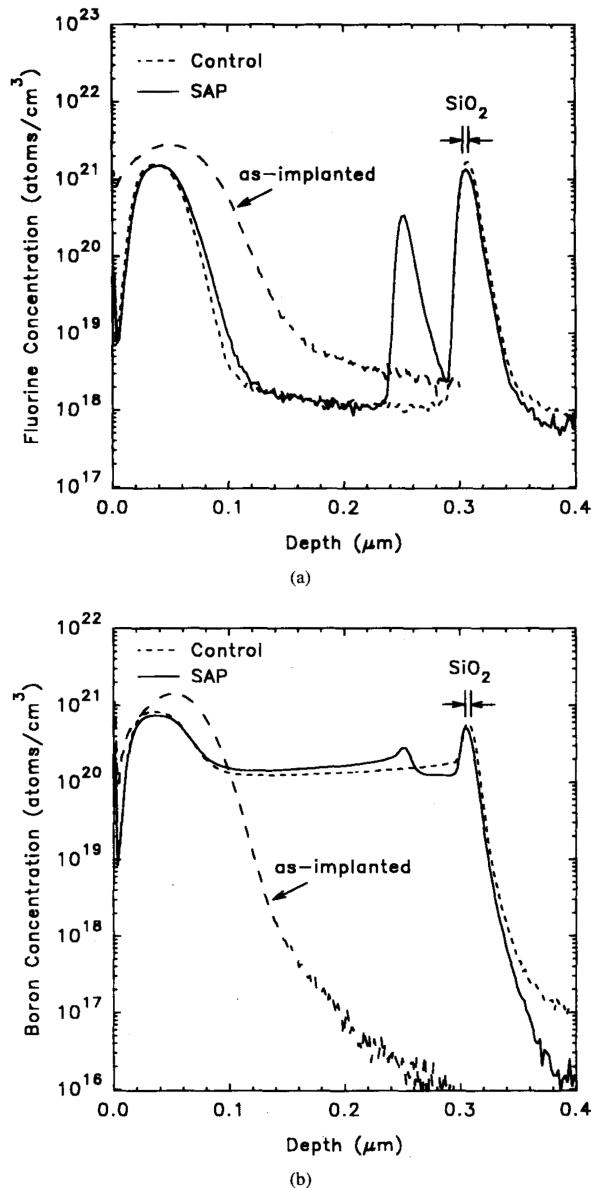


Fig. 9. The SIMS depth profiles of (a) fluorine and (b) boron of the BF_2-implanted control and SAP gates. The films were implanted with dose of 1×10^{16} cm^{-2} and annealed in N_2 for 30 min. at 900°C.

et al., the distortion may be due to the boron penetration induced donor-type defect centers within the surface region of Si substrate. In comparison with control and SAP gate structures, samples with SAP gate structure show a much less threshold voltage shift and C–V distortion. Fowler-Nordhiem stressing with a constant gate current density of +100 mA/cm^2 is performed on PMOS capacitors to characterize the gate oxide reliability, as shown in Fig. 4. Results show that electron trapping efficiency in the gate oxide increases with boron penetration and the capacitors with the SAP structure exhibit lower electron trapping efficiency and higher value of charge to breakdown (Q_{bd}).

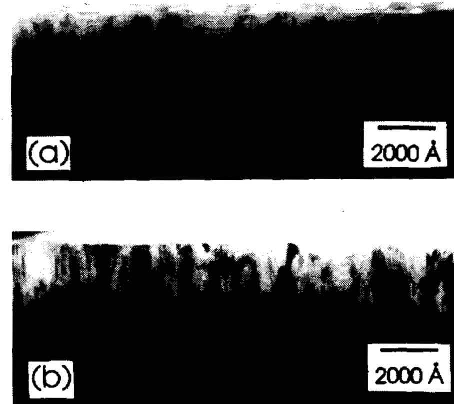
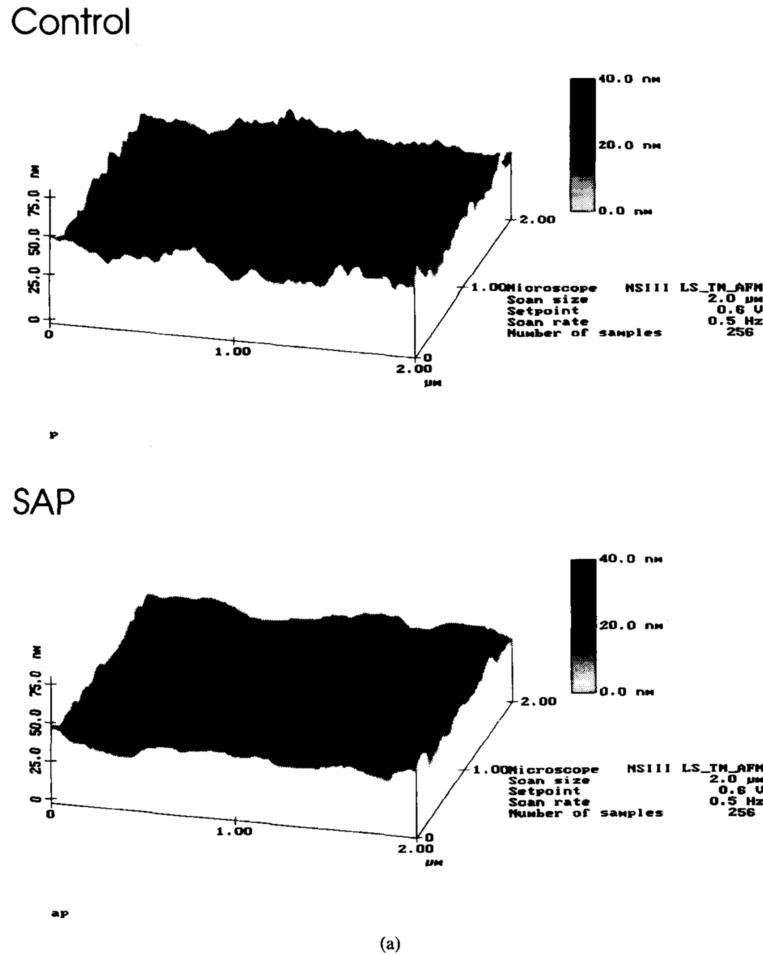


Fig. 10. TEM cross section for BF_2-implanted gate: (a) control; (b) SAP. The films were BF_2-implanted with 5×10^{15} cm^{-2}, after annealed at 900°C for 30 min.

B. P^+-poly Gated MOS Transistors

The measured threshold voltage as a function of poly-gate length is shown in Fig. 5. The threshold voltage is determined by the extrapolation of the interception point on the V_G axis of the linear I_D versus V_G slope at the maximum transconductance (at $V_D = -0.1$ V) in the I_D versus V_G plot. Less positive threshold voltage shift, resulted from boron penetration effect, is observed for the SAP structure. The reverse short-channel effect (RSCE), i.e., the threshold voltage becomes more negative with decreasing channel length, is also found. It can be explained by the laterally nonuniform channel profile in the channel due to effects of fluorine enhanced boron diffusion in the gate oxide and subsequent thermal budget after the poly-gate etch [26]. This phenomena was also observed by Sung *et al.* [4], H and/or OH radical during deposition of the TEOS gate spacer were reported to attribute to the enhanced reverse short-channel effect. In comparison with control and SAP structures, samples with SAP poly-gate show a much weaker gate length dependence, since the boron penetration is greatly suppressed by the SAP poly-gate. Furthermore, a less threshold voltage variation is obtained for the SAP structure. With significant boron penetration, the transistor becomes a depletion type and the subthreshold swing of the transistor increases [3], [4]. The measured subthreshold characteristics for short channel P-MOSFET's ($L_G = 0.35$ μm) of both types of gate structures are shown in Fig. 6. The subthreshold swing is increased largely for control samples as the BF $_2$-implanted dosage increases from 2×10^{15} cm^{-2} to 1×10^{16} cm^{-2}. Channel hot-carrier effects of short channel P-MOSFET's were also studied. As shown in Fig. 7, the SAP structure exhibits less degradation in terms of less threshold voltage shift for various gate voltage conditions.

Gated-diode measurement [27] was also performed to characterize the physical damage at the Si/SiO_2 interface induced by the boron impurities which were diffused from the heavily doped poly-gate. For $V_G < V_{FB}$, the interface is accumulated and the leakage current originates from the depletion region of the metallurgical p-n junction only. When the gate



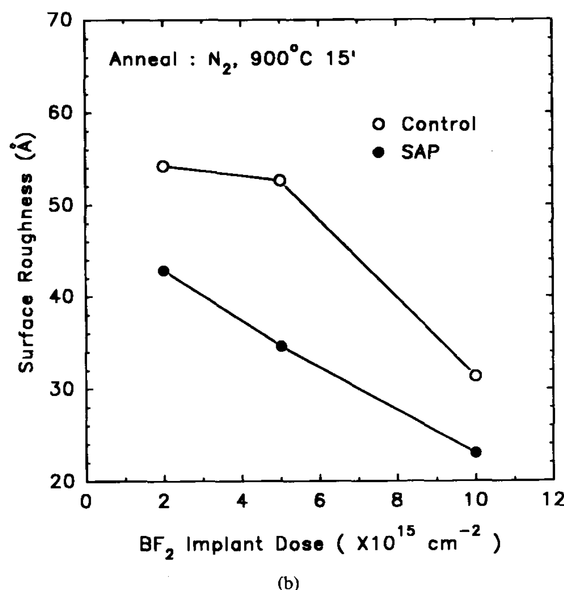
(a)

Fig. 11. (a) AFM images of poly-gate films in 2 μm square regions; (b) surface microroughness of the films for both gate structures as a function of BF_2-implanted dosage. The films were annealed at 900°C for 15 min.

voltage reaches flat-band condition, a field-induced depletion region is created under the surface which contributes to strong increase in diode reverse current. Besides the reverse current due to generation-recombination centers in the bulk silicon, there is a contribution due to the generation at surface states at the Si/SiO_2 interface as the gate voltage increases. When threshold voltage is reached, the inversion layer shields the surface states from the depletion region and the leakage current due to generation from interface traps decreases sharply by an amount directly proportional to the number of interface states. The measured results shown in Fig. 8 indicate that the penetration of boron into the gate oxide and channel actually results in an increase in interface state density.

C. SIMS Analysis

Fig. 9(a) shows the measured SIMS depth profiles of the fluorine concentration in the poly-gate/SiO_2/Si structure for both gate structures. The samples were implanted by BF_2 to a dose of 1×10^{16} cm^{-2}, followed by furnace annealing in N_2 ambient at 900°C for 30 min. As can be seen, the profile of the control sample at the as-implanted position is narrower than that of the SAP structure. This implies that fluorine diffusion in the SAP gate exhibits a lower effective diffusion rate than that in the control sample. Furthermore, there is a pile-up of fluorine at the interface between top-layer and bottom-layer for the stacked gate structure. The pile-up of fluorine results from the existence of a thin interfacial oxide layer between the polysilicon layer and amorphous silicon layer in the SAP structure. The interfacial oxide layer was formed during the deposition break due to the residual oxygen in the LPCVD system. Detail description of the segregation and diffusion mechanism for fluorine and boron atoms will be discussed in the later report [28]. The effects of lower fluorine diffusion rate in the underlaid amorphous silicon [16], [29] and segregation of fluorine impurities at the poly/amorphous interface result in a much larger amount of fluorine in the gate electrode. The more fluorine is retained in the poly-gate electrode, the less fluorine diffuses into the gate oxide. Therefore, for the SAP structure, less fluorine and boron are present in the gate oxide, which results in less fluorine



(b)

Fig. 11. (Continued)

enhanced boron penetration as shown in Fig. 9(b). Thus, boron penetration effect can be effectively suppressed by the SAP gate structure.

D. TEM Analysis and Surface Roughness

Fig. 10(a) and (b) are the TEM micrographs of both kinds of structures after 900°C annealing for 30 min. The texture of the SAP structure reveals that there exists an interface between polysilicon layer and amorphous silicon layer. Furthermore, the grain boundaries of the polysilicon and amorphous silicon are not aligned. The amorphous silicon layer exhibits more random orientation, while the polysilicon layer exhibits the well known columnar structure.

A smoother gate/oxide interface is observed in the structure of polysilicon with underlaid amorphous silicon. The smooth gate/oxide interface can simplify many processing steps such as lithography and etching. As gate electrodes, the surface morphology is an important factor in device reliability because that the presence of asperity on the film surface can lead to premature device failures from localized high electric fields. Thus, it is highly desirable to have gate electrodes with smooth surfaces [30]. Furthermore, as poly-gate etching is anisotropic, poly-gates with rough morphologies require extended overetch to remove highlight residues. This extended etching may have a propensity for the pitting of the substrate which would degrade device reliability, especially for the scaled gate oxide in future CMOS technology. Surface microroughness of gate films is evaluated by atomic force microscope (AFM: NanoScope III, Digital Instruments). AFM images in polysilicon films in 2 μm square regions for both gate structures are shown in Fig. 11(a). The surface roughness becomes smaller with increasing the implant dose of BF_2 as shown in Fig. 11(b). For the SAP gate, smoother surface is obtained resulted from smooth surface of the underlaid amorphous layer.

IV. Conclusion

Retardation of boron diffusion from the p^+ poly-gate into the substrate of the PMOS devices is significantly achieved by employing the SAP structure which is composed of polysilicon layer with underlaid amorphous silicon without degrading device reliability. Superior device performance and tighter threshold voltage controllability are obtained in the p-channel MOSFET's with the new poly-gate structure. Furthermore, the interface quality underneath the gate oxide can be preserved. Retention of fluorine impurity in the poly-gate due to lower diffusion rate in amorphous silicon, interfacial segregation effect, and differently aligned grain boundaries are shown to be the possible causes for retarding boron penetration. The process of the SAP poly-gate is simple and compatible with conventional CMOS process and can be readily adapted in deep submicrometer CMOS technology.

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Chih-Yung Lin (S'90) was born in Taichung, Taiwan, Republic of China, on September 4, 1967. He received the B.S. degree from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, in 1990. He is currently working toward the Ph.D. degree in the Institute of Electronics, National Chiao-Tung University. His research interests are in the areas of thin dielectric reliability, short-channel effects, process, and characterization of CMOS devices.

Chun-Yen Chang (S'69–M'70–SM'81–F'88) was born in Kaoshing, Taiwan, Republic of China, on October 12, 1937. He received the B.S. degree in electrical engineering from National Chen Kung University, Tainan, Taiwan, in 1960, and the M.S. and Ph.D. degrees from National Chiao Tung University in 1962 and 1970, respectively.

From 1962 to 1970, he was a research assistant and then an Instructor at Chiao Tung University working on organizing a semiconductor research laboratory. During 1966 to 1976, he was first an associate professor and later a professor in solid-state elecronics and semiconductor physics and technologies; he was also chairman of the Department of Electrophysics, Chiao Tung University, and has been a professor and director of the Institute of Electrical Engineering, National Chen Kung University, from 1977 to 1987, where he has established a strong research and development base in electrical and computer engineering. In 1981, he became a member of the technical staff at Bell Laboratories, Murray Hill, NJ, working in the VLSI Device Group. He was a visiting professor at the University of Florida, Gainesville, in 1987 and the University of Stuttgart, Stuttgart, Germany, in 1989, where he taught MBE technologies and devices. He has consulted ERSO/ITRI, Nippon Seiki Co., UMC, etc., on VLSI physics and technologies including III–V compound devices and materials using MBE and MOCVD, and amorphous-silicon devices. He has taught the majority of senior semiconductor engineers in Taiwan since 1962, and published more than 200 technical papers in international journals. He has contributed carrier transport theory and specifice contact resistivity in metal-semiconductor systems (1970, 1971). He invented a method for MOS surface stabilization (1966), the method of low-pressure MOCVD using TEG source (1981), amorphous Si phototransistors (1986), and the bipolar-unipolar transition negative resistance transistor (BUNDR) (1987), etc. He is now a professor, the first Dean of the College of Electrical Engineering and Computer Sciences of National Chiao Tung University where 172 faculties are involved, and the Director of National Nano Device Laboratory, Taiwan, Republic of China.

Dr. Chang is a member of Phi Tau Phi, the American Electro-Magnetics Academy, the Chinese Institute of Electrical Engineers, the American Physical Society, and the Electrochemical Society. He has been elected an IEEE fellow for "his contribution to semiconductor devices development and to education." He was the recipient of an academic achievement award in engineering from the Ministry of Education and the distinguished research award of the National Science Council, Republic of China, as well as the recipient of the 1989–1990 international traveling award granted by the China Foundation to the distinguished scholars in the Republic of China.

Charles Ching-Hsiang Hsu (M'88), for photograph and biography, see p. 294 of the February 1995 issue of this TRANSACTIONS.