A Self-Calibrate All-Digital 3Gbps SATA Driver Design

Hsin-Wen Wang
Dept. of Electrical Control Engineering
National Chiao Tung University
Hsin-Chu, Taiwan, ROC
hwwang.ece91g@nctu.edu.tw

Hung-Wen Lu
Dept. of Electrical Engineering
National Central University
Jhong-Li, Taiwan, ROC
s9521011@cc.ncu.edu.tw

Chau-Chin Su
Dept. of Electrical Control Engineering
National Chiao Tung University
Hsin-Chu, Taiwan, ROC
ccsu@cn.nctu.edu.tw

***Abstract* - This paper presents an all digital *Low Voltage Differential Signal* (LVDS) driver for *Serial-ATA* (SATA-II) with *simultaneous switching noise* (SSN) reduction capability. An auto calibration mechanism is included to deal with the process and environmental variation. The chip is implemented using TSMC 0.18-µm 1P6M CMOS technology. The core area is 350x350 μ m^2. The transmitter operates at 3 Gbps under a 1.8V power supply and consumes 11mW of power.**

I. INTRODUCTION

CMOS technologies have grown exponentially in recent years. The scale down of CMOS devices allows higher operating frequency, shorter rise/fall times, and narrower pulse width. With the increase in data rate and decrease in supply voltages, the SSN noise introduced by the transient current injecting into the power and ground grows rapidly [1].

In this paper, we propose an all digital LVDS driver in Section II. To reduce the SSN effect a turn-on spreading and duty cycle modulation mechanisms are proposed. A self-calibrated all-digital 3Gbps Serial ATA [3] driver is implemented. The self calibration circuit is designed in Section III to guarantee the output signal offset and swing meet the standard requirement under process variation. Finally, measurement results are described in Section IV and conclusions are given in Section V.

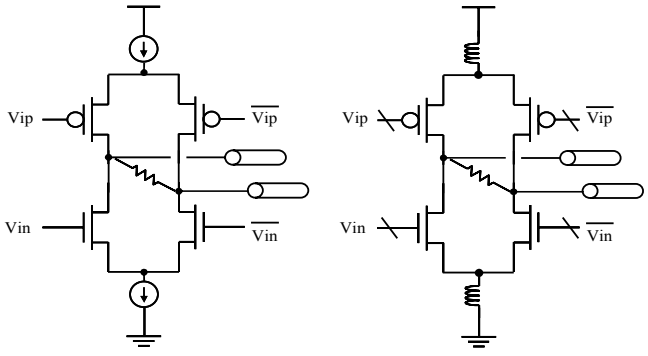

Figure 1. The tranditional and proposed driver

II. SSN REDUCTION TECHNIQUE

Traditionally, the SSN problem is solved by packaging techniques, such as reducing the bonding wire inductance or increasing the number of the power pads. However, the main source of the SSN is the large current fluctuation and it is difficult to measure [4]. So, circuit techniques to decrease the transient current are recommended. In Figure 1, the driver on the left includes two current sources to obtain constant current during the operation [2]. Our design, on the right, has no current source. The purpose is to have the advantages in large output swing and small switch transistor sizes. Therefore, the sizes of the pre drivers can be reduced as well. However, if the current sources connected to power and ground are removed, the SSN will be large due to large current transition when input data changes and the SSN effect will be large due to poor power supply rejection ratio (PSRR). So, we propose a novel turn on spreading technique to reduce SSN effect. By the way, the driver becomes an all digital as compare to the analog version of the LVDS standard.

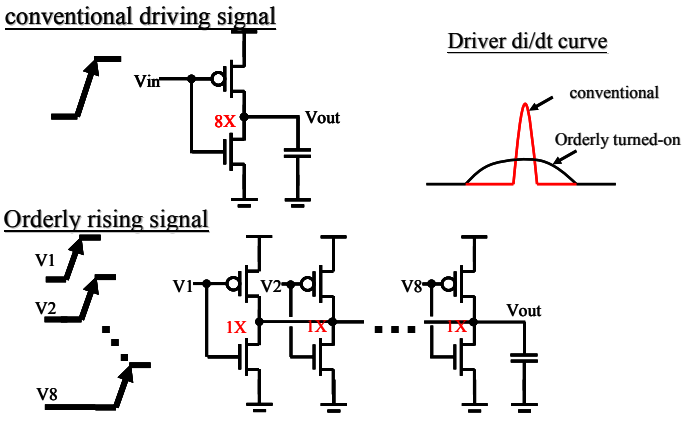

Figure 2. The idea of the orderly turn-on buffer

A. *Orderly Turn-on Buffer*

The idea of the orderly turn-on buffer is shown in Figure 2. The conventional driver has a current spike when switching. Our design is composed of several parallel drivers and

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each of them is orderly turned on with a small time step. As a result, the driving current increases gradually to minimize the L*dI/dT effect. The key issue is the design of pre drivers to obtain a time step as small as 15ps.

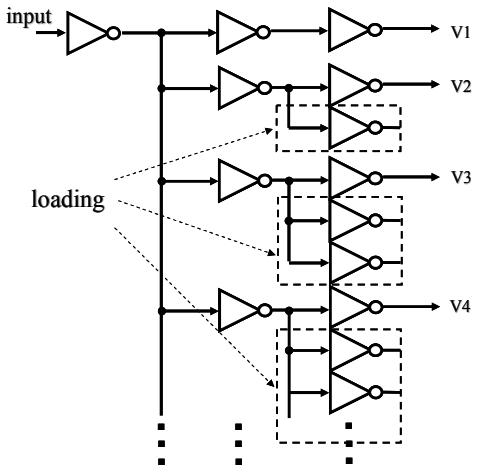

Figure 3. Orderly turn-on buffer

Figure 3 shows a new approach to generate the signals which separated by only 10~15ps. After the input passes the first two inverters, it goes in several paths with different loading. Because of the loading effects, the delay time of each output is separated.

B. *Duty Cycle Adjust Buffer*

Figure 4 shows the duty cycle adjust buffer. It minimizes the current which charge or discharge from power supply or ground. It also decreases the SSN because the lower variation of driving current.

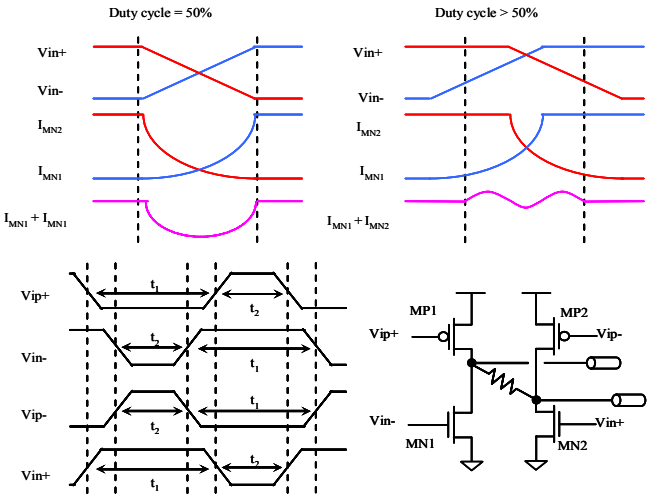

Figure 4. Duty cycle adjust buffer.

III. SELF-CALIBRATION OF THE DRIVER

A. *Overall Architecture*

The overall architecture is shown in Figure 5. Drivers are separated into two groups, one fixed and one programmable. 6 fixed drivers are controlled by 6 orderly turn-on buffers (Figure 3). The 8 programmable drivers are used to setup the desired offset and signal swing such that the high and low differential outputs are 375mV and 125mV respectively. A set of comparators are used to compare the high and low voltages to the differential output. The results are fed to the *finite state machine* (FSM) to control the number of turned on transistors for PMOS and NMOS so that the differential swing will be in the desired range.

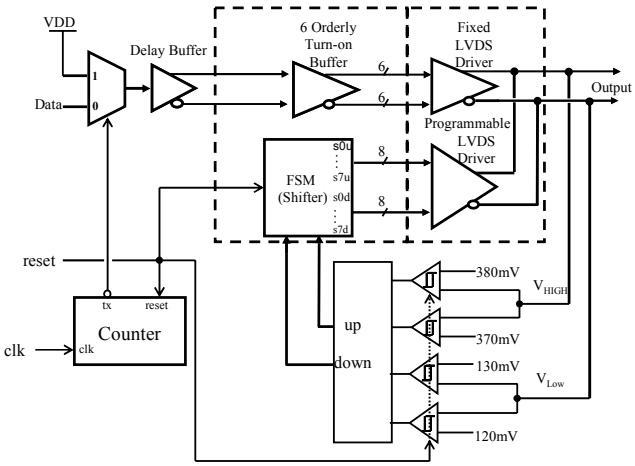

Figure 5. The overall auto self-calibration driver architecture

The purpose of the counter is to control the calibration cycle. During the calibration, VDD is selected as the input. The differential outputs are compared to $375 \pm 5mv$ $125 \pm 5mv$. If the voltages are not within the range, the number of turned on PMOS and NMOS transistors will be adjusted. If the differential high voltage is too low (high), the number of PMOS transistors is increased (decreased), and vise versa for differential low voltage and the NMOS transistors. Overall, it takes 24 control cycles for the calibration.

B. *Reflection and Process Vialation Consideration*

The termination is critical for high speed I/O. In general, the transmission channel is designed to have a characteristic impedance of 50Ω. Hence, the termination of 50Ω is desirable to minimize the reflection and maintain the signal integrity. However, the use of 50Ω implies the increase in power consumption. If both ends are terminated with 50Ω, the power consumption doubles. For example, SATA 1 use the circuit structure shown in left of Figure 6. Near end differential 100Ω in parallel with the far end differential 100Ω, the equivalent resistance is 50Ω. Therefore, the current must be doubled in order to obtain the same output swing.

The structure shown in the right of Figure 6 is the one being implemented. With far end 100Ω (50Ω+50Ω), if the transistors are programmed in such a way that the high voltage is 375mV and the low is 125mV, 3/4 and 1/4 of the 500mV terminal supply voltage. That means the equivalent resistance of PMOS and NMOS transistors are both 50Ω. By doing so, we solved the many problems with a single approach, programmable drivers. First, the offset is controlled at 250mV and the swing is controlled at 250mV. Second, the reflection is minimized due to the equivalent 50Ω termination at the near end. Third, the power consumption is halfed because there is no real near end termination. So, by merging 50Ω termination into the driver, we actually gain significant advantages.

The process variation is handled gracefully through programmable drivers. Figure 7 shows corner-case simulation results. The horizontal axis is the number of turned on transistors and the vertical one is the output voltage. Three curves represent the SS, TT, and FF corners. The left figure shows the output high voltage and left one shows the output low. As one can see, regardless of the process corner, there exists at least one combination that can produce the desired output levels.

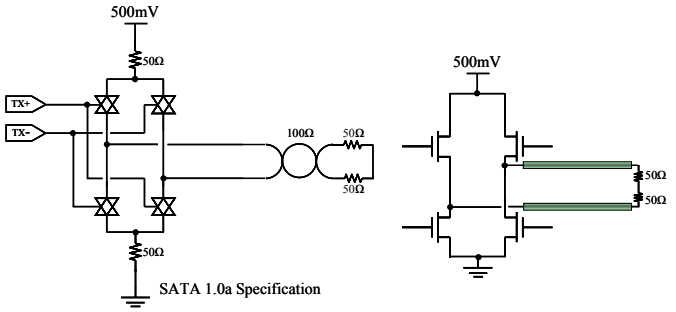

Figure 6. The transmitter circuit example in SATA 1.0a specification

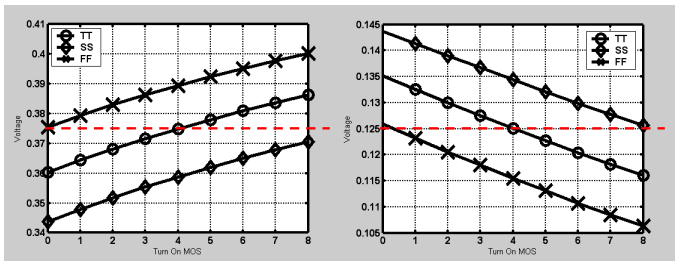

Figure 7. The output voltage of the TT, SS and FF cases

IV. MESUREMENT RESULTS

The chip was implemented through National Chip Implement Center (CIC) in 0.18um CMOS 1P6M technology. The chip photograph is shown in Figure 8.

A. *Measurements*

The measurement results are shown in Figure 9. The results include the eye diagrams for 625Mbps, 1.25Gbps, 2.5Gbps, and 3Gbps, which are popular for high speed I/Os. The measured jitters are 52ps, 55ps, 102ps, 128ps respectively. Note that the height of the eye diagram is about $\pm 250mV$, which conforms the SATA specification.

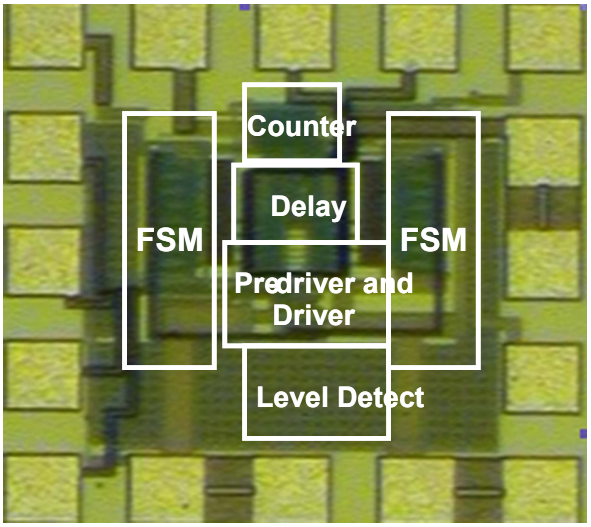

Figure 8. Die photo

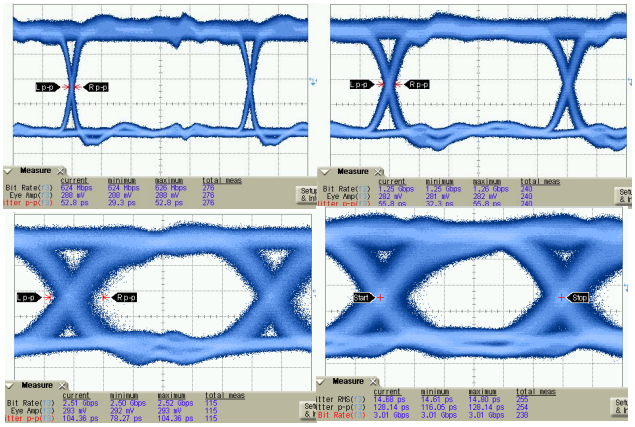

Figure 9. Output eye-diagram (625Mbps, 1.25Gbps, 2.5Gbps, 3Gbps)

B. *Calibration Function Testing*

In order to check the function of the auto calibration, we test the chip in a special way. First, we restrict the four reference voltage to very low level. We expect the chip will calibrate the output to the lowest. Second, we change the reference voltage to the highest so the calibration procedure will force the output "rising". By the recordable function of oscilloscope, we keep track of the output during calibration. In Figure 10, we show the verification of the auto calibration function results. The calibration range is about 100mV according to two blocks movements. Figure 11 shows another case of the "falling" calibration.

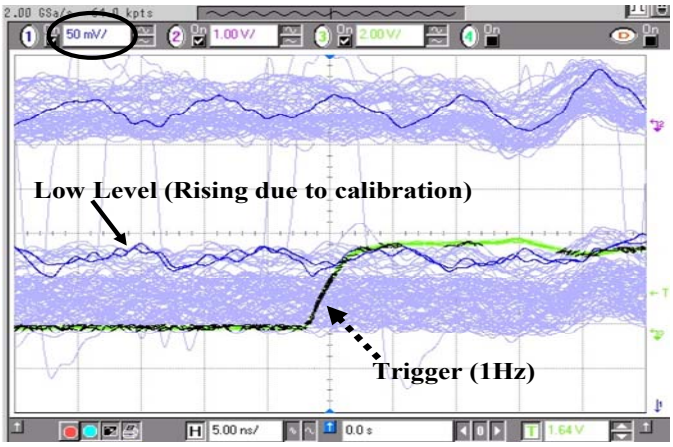

Figure 10. Auto calibration function verification - 1

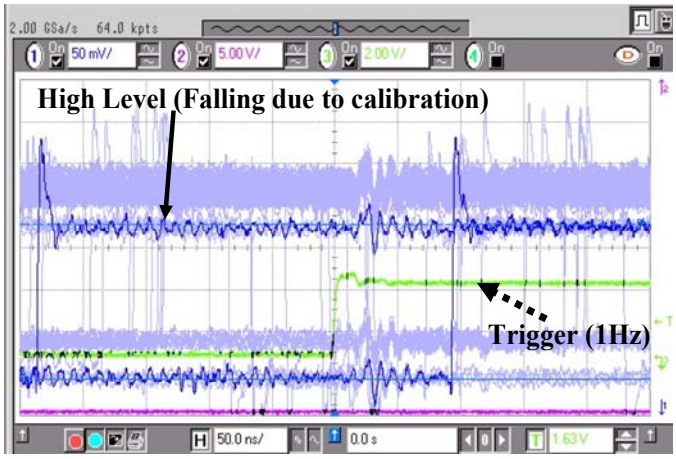

Figure 11. Auto calibration function verification - 2

V. CONCLUSION

In this paper, we have proposed a 3 Gbps SATA II driver with novel scheme for SSN reduction and auto calibration. The proposed orderly turned-on and duty cycle modulation method is effective for SSN reduction. We use the programmable drivers to solve the process variation problem and obtain the desirable offset and swing simultaneously. Further more, by merging the termination 50Ω resistance into the driver, power consumption is reduced by half and reflection is minimized simultaneously. The chip is implemented using TSMC 1P6M CMOS process with a core size of 350 x 350 μm2 . The power consumption is 11mW including calibration and 10mW without calibration. The measurement results show that the offset and swing can be calibrated to the desired value.

TABLE I. CHIP SUMMARY

Function	***3Gbps SATA II Driver***
Technology	0.18um 1P6M CMOS
Supply Voltage	1.8V
Core Size	350x350 μm^2
Transistor/Gate Count	2531/966
Power Comsumption	~11mW
Jitter (pk-pk)	~128ps @ 3Gbps
Output Swing (pk-pk)	$\sim \pm 250mV$

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