Initial-On ESD Protection Design with PMOS-Triggered SCR Device

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***Abstract*—A novel SCR design with "*initial-on*" function is proposed to achieve the lowest trigger voltage and the fastest turn-on speed of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on design is implemented by PMOS-triggered SCR device, which can be realized in general CMOS processes. This initial-on SCR design also presents a high enough holding voltage to avoid latchup issue. The new proposed initial-on ESD protection design with PMOS-triggered SCR device has been successfully verified in a 0.25-μm CMOS process.**

I. INTRODUCTION

Electrostatic discharge (ESD) damage has become the main reliability issue for CMOS IC products fabricated in the nanoscale CMOS processes. The on-chip ESD protection devices must be added into CMOS chips to achieve the required ESD robustness. In the past, the traditional ESD protection devices are initially kept off in CMOS ICs, as illustrated in Fig.1. When the pad is zapped with ESD pulse, the ESD clamp device is triggered on by the overstress ESD voltage to conduct ESD current from the pad to ground. However, when the core circuits are realized with the much thinner gate oxide in the nanoscale CMOS technology, the traditional ESD protection design could not be able to effectively protect the core circuits with thinner gate oxide. To effectively protect the core circuits with much thinner gate oxide in the nanoscale CMOS technology, the new on-chip ESD protection concept with the already-on ESD protection device is shown in Fig. 2. The ESD clamp device is kept off, when the IC is in the normal circuit operation conditions. But, the ESD clamp device is normally on, when the IC is floating without any power bias. When the IC is zapped by ESD, the ESD clamp device standing in the already-on condition can quickly discharge ESD current from the pad to ground. Therefore, this new ESD protection concept can effectively protect the core circuits in the nanoscale CMOS technology.

In IC products, the on-chip ESD protection devices are required to provide higher ESD robustness with smaller layout area to save the chip area. Silicon controlled rectifiers (SCRs) have been used as on-chip ESD protection devices, because of their superior area-efficient ESD robustness. However, SCR has some drawbacks, such as higher trigger voltage (Vt1), slow turn-on speed, and even latchup danger. Therefore, the low-voltage-triggered SCR (LVTSCR) was invented to reduce the trigger voltage of SCR device [1]. Moreover, some advanced circuit techniques (the gate-coupled [2], substrate-triggered [3], and GGNMOS-triggered [4] techniques) were also reported to enhance the turn-on speed of SCR devices. However, those modified SCR designs [1]-[4] still function as the initial-off ESD devices. Recently, in order to further enhance the turn-on speed, the native-NMOS-triggered SCR (NANSCR) has been reported to achieve more efficient ESD protection for CMOS ICs in the nanoscale CMOS technology [5]. In this NANSCR, it uses the special native device to achieve the "initial-on" function. Besides, to keep such NANSCR in off state when the IC is in normal operation, it needs the on-chip negative-bias generator [6]. Such extra efforts to realize the NANSCR with negative gate bias for on-chip ESD protection design would cause some limitation in practical applications of general CMOS ICs.

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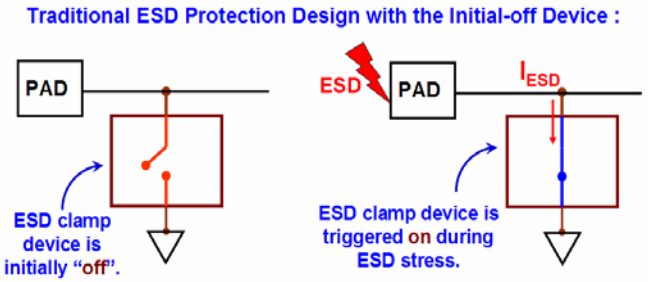


Fig. 1 The traditional ESD protection design with the initial-off ESD protection device.

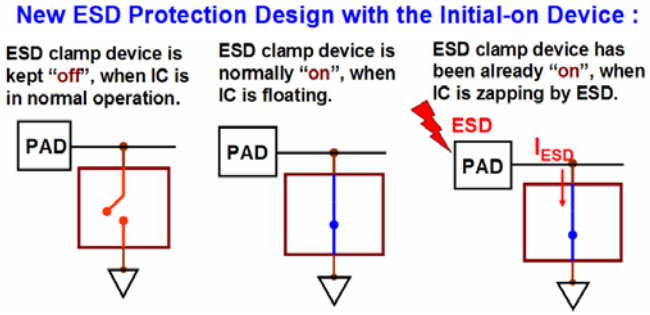


Fig. 2 The new ESD protection concept with the initial-on ESD protection device.

In this work, a novel initial-on SCR design is proposed to achieve the lowest trigger voltage and the fastest turn-on speed of SCR device for effective on-chip ESD protection. Without using the special native device or any process modification, this initial-on SCR design is realized by circuit skill with PMOS in general CMOS process. This initial-on SCR design also presents a high enough holding voltage to avoid latchup issue.

II. Realization of the Initial-On Design

A. Implementation of the Initial-On ESD Protection Circuit

The new proposed initial-on ESD protection design, which consists of the SCR device with PMOS-triggered technique and the RC-base ESD transient detection circuit, is shown in Fig. 3. A PMOS transistor is directly embedded into the SCR structure to achieve the initial-on function for ESD protection. The source and drain terminals of the PMOS transistor are connected to the additional n+ diffusion and p+ diffusion of the SCR structure, respectively, as illustrated in Fig. 3. These additional p+ diffusion and n+ diffusion are the p-triggered and n-triggered nodes in p-substrate and n-well of this SCR structure, respectively, to enhance the turn-on speed of SCR during ESD stress. The gate terminal of the embedded PMOS is connected to the RC-based ESD transient detection circuit, which is used to distinguish the ESD-stress conditions from the normal circuit operation conditions.

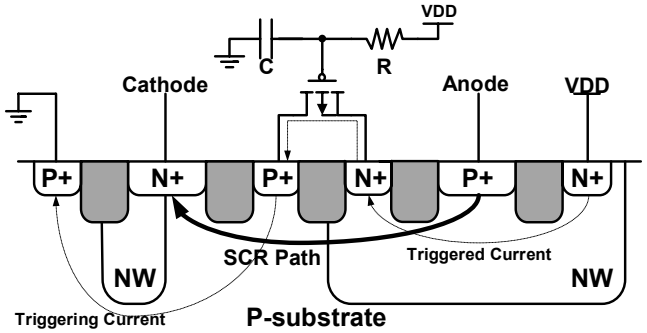


Fig. 3 The *initial-on* SCR design with PMOS-triggered technique. The embedded PMOS transistor generates the triggering current to initiate the turn-on of SCR during ESD stress.

B. Operation Principles

Under ESD-stress condition, the gate voltage of embedded PMOS is initially kept at zero. With an initial gate voltage of 0V, the PMOS is initially on to conduct the ESD current from the anode (P+) of SCR into its n-well, and then inject into the p-substrate of the SCR device. With the both triggering currents in the n-well and p-substrate, the SCR can be fired on quickly. Finally, the ESD current is mainly discharged from the anode to the cathode of SCR device. During normal circuit operation condition with the normal VDD and VSS power supplies, the gate of embedded PMOS is biased at VDD to keep itself off. Therefore, the PMOS-triggered SCR device is always kept off during the normal circuit operation condition. To distinguish the ESD-stress condition from the normal circuit operation condition, the RC time constant of the ESD detection circuit in Fig. 3 is designed around 1 μs.

C. Arrangements for On-Chip Applications

The on-chip ESD protection designs for input, output, and power-rail ESD clamp circuits with PMOS-triggered SCR devices and the corresponding ESD-transient detection circuits are shown in Fig. 4. The initial-on SCR design with the lowest Vt1 and the fastest turn-on speed, as compared to the LVTSCR, can effectively protect the internal circuits against ESD damage. The initial-on SCR design, with the gate bias of VDD on the embedded PMOS, have a high enough holding voltage to prevent the latchup issue under the normal circuit operation condition. In addition, the RC-based ESD detection circuits among the I/O cells can co-share the R and C to save chip area, as those shown in Fig. 4.

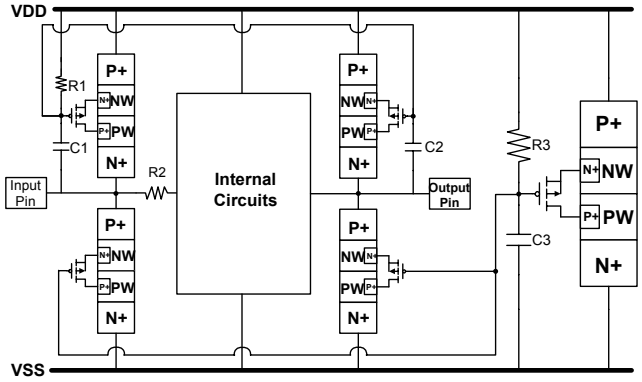


Fig. 4 The on-chip ESD protection design for input, output, and power-rail ESD clamp circuits with the initial-on SCR design.

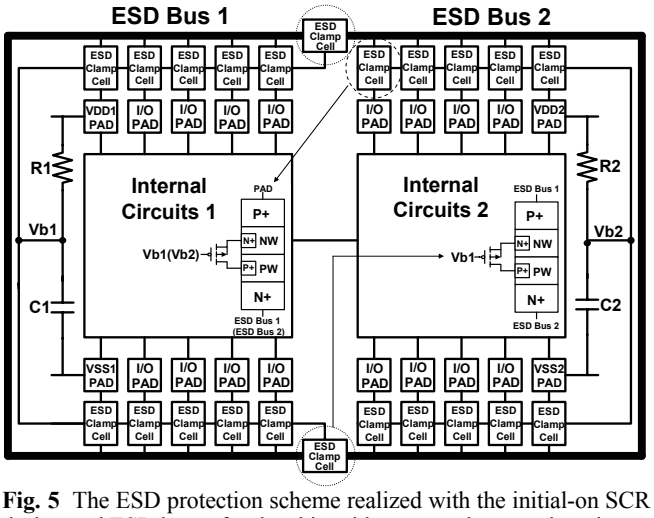


Fig. 5 The ESD protection scheme realized with the initial-on SCR design and ESD buses for the chip with separated power domains.

The interface circuits in the CMOS ICs with separated power domains are often damaged by ESD stress, especially during the I/O pin to I/O pin ESD stress. For the chip with separated power domains, the whole-chip ESD protection scheme realized with the proposed initial-on SCR design and ESD buses is shown in Fig. 5. In the same power domain, the

anodes of the PMOS-triggered SCR devices are connected to the pads (including I/O, VDD, and VSS pads), and their cathodes are connected to the common ESD bus. The ESD bus can be realized by the wide metal line in the chip to efficiently conduct ESD current of several amperes during ESD stresses. To further save layout area, such ESD bus can be co-designed with the seal ring of the chip. Between the ESD buses, the initial-on SCR design is also used to connect the separated ESD buses to avoid the ESD damage on the interface circuits between the separated power domains. During ESD stresses, the PMOS-triggered SCR devices with the *initial-on* function in the whole-chip ESD protection scheme can be quickly triggered on to efficiently protect the internal circuits. The proposed initial-on SCR design can achieve the same turn-on efficiency of the already-on (native) device for ESD protection, but neither the extra on-chip negative voltage generator nor the native device is used in this new realization of initial-on ESD protection concept with the PMOS-triggered SCR device.

D. Layout Structure for Initial-On SCR Device

To investigate the turn-on phenomena and circuit characteristics, two types of layout implementations (structure-1 and structure-2) for the proposed initial-on SCR design are verified in this work, as shown in Figs. 6(a) and 6(b). The embedded PMOS devices of structure-1 and structure-2 are different in the layout of the n-triggered node and the anode-to-cathode spacing. Because the n-triggered node has been merged into the PMOS source terminal, the anode-to-cathode spacing of structure-2 is reduced to 7.7 μm, whereas the anode-to-cathode spacing of structure-1 is 9.5 μm. The holding voltage and ESD robustness of the PMOS-triggered SCR device can be adjusted by its anode-to-cathode spacing.

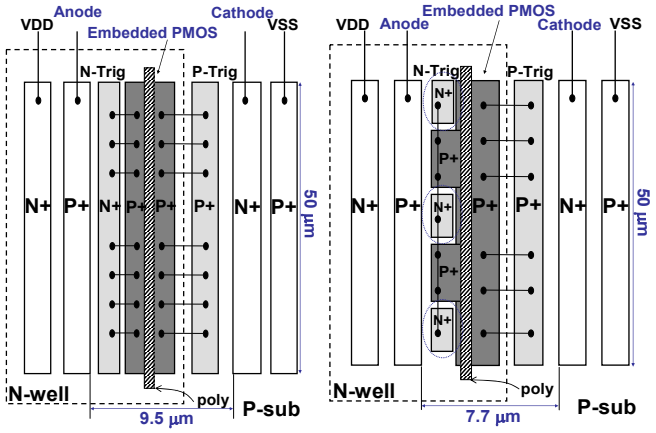


Fig. 6 The top views of initial-on SCR design with (a) structure-1 and (b) structure-2 layout styles.

III. EXPERIMENTAL RESULTS

A. DC Analysis for the Initial-On ESD Protection Circuit

The initial-on SCR designs, in Figs. 6(a) and 6(b), have been fabricated in a 0.25-μm salicided CMOS process without using the silicide-blocking mask. The active width of the SCR devices is drawn as 50 μm in the chip. The measured DC I-V curves of the initial-on SCR designs with structure-1 and structure-2 layout styles are shown in Figs. 7(a) and 7(b), respectively, which are measured with different gate-biased voltages (V_G) on the embedded PMOS transistor of the SCR device. The Vt1 of the PMOS-triggered SCR devices is reduced with the decrease of the gate-biased voltage.

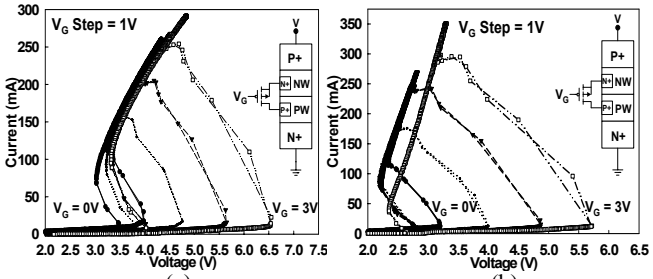


Fig. 7 The measured DC I-V curves of the initial-on SCR designs with the layout styles of (a) structure-1, and (b) structure-2, under different gate-biased voltages.

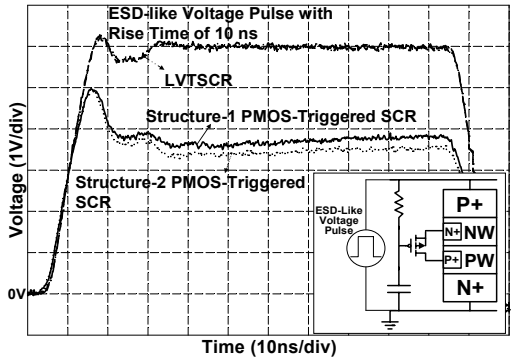
When the gate voltage of the embedded PMOS is increased from 0 to 3 V, the Vt1 of the PMOS-triggered SCR device is increased from ~4 V to ~6.6 V and ~3.3 V to ~5.75 V in structure-1 and stricture-2, respectively. These results have proven that the Vt1 of the SCR device can be significantly reduced by the proposed PMOS-triggered technique. The holding voltage of the PMOS-triggered SCR device is increased when the gate voltage of embedded PMOS is increased, as shown in Figs. 7(a) and 7(b). During ESD stress, the gate voltage of the embedded PMOS is kept at 0V by the RC-based ESD detection circuit. With an initial gate voltage of 0V, the SCR device has the lowest holding voltage to effectively clamp the over-stress ESD pulse.

In addition, another issue of using the SCR devices as the ESD protection device is the latchup concern under normal circuit operation condition. To avoid latchup issue, the holding voltage of the SCR devices must be designed greater than the maximum voltage of VDD. The holding voltage of the PMOS-triggered SCR device with the gate bias of 2.5 V under structure-1 layout style is about ~3.1 V, which is higher than the 2.5-V VDD voltage. The holding voltage of PMOS-triggered SCR device under structure-2 layout style has a holding voltage of ~2.3 V when the gate bias is 2.5 V. A diode can be added in series with the PMOS-triggered SCR device to further increase the total holding voltage for latchup-free applications.

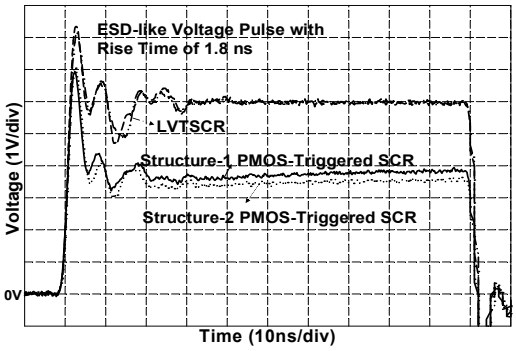
B. Turn-on Speed

To observe the turn-on speed of the initial-on SCR design, ESD like voltage pulse with different rise times were applied on the anodes of the PMOS-triggered SCR with structure-1, structure-2, and the traditional LVTSCR for comparison. The measured waveforms of clamped voltage are shown in Figs. 8(a) and 8(b). The measurement setup for investigating the turn-on speed of the initial-on SCR design is also illustrated in the inset figure of Fig. 8(a). In Fig. 8(a) with a rise time of

10ns, the PMOS-triggered SCR devices clamp the overstress voltage pulse to a lower voltage level. In Fig. 8(b) with a rise time of as short as 1.8ns, the PMOS-triggered SCR devices performed a faster turn-on speed than LVTSCR did. The rising edges of the voltage waveforms clearly prove the faster turn-on speed of the new proposed initial-on SCR design under both structure-1 and structure-2 layout styles. With faster turn-on speed, the PMOS-triggered SCR can rapidly clamp the overshooting ESD voltage pulse to a lower voltage level. Thus, the core circuits with thinner gate oxide can be well protected by the new proposed initial-on SCR design.



(a)

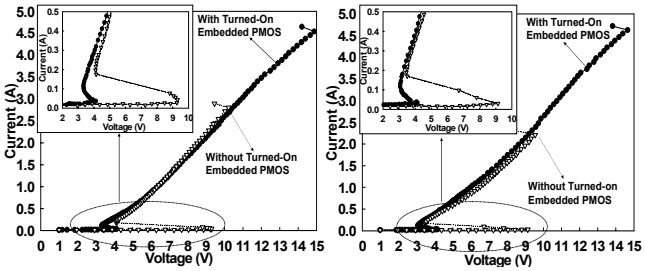


(b)

Fig. 8 The measured voltage waveforms clamped by the LVTSCR and the PMOS-triggered SCR in structure-1 and structure-2. The ESD-like voltage pulses were applied to the anodes of SCR devices with the rise time of (a) 10 ns and (b) 1.8 ns.

C. TLP Characteristics

The TLP-measured I-V characteristics of the new proposed initial-on SCR design with the structure-1 and structure-2 layout styles are shown in Figs. 9(a) and 9(b), respectively. The Vt1 of the PMOS-triggered SCR devices in structure-1 and structure-2 can be significantly reduced to 4.3 V and 4.2 V, respectively, when the gate of embedded PMOS is kept at 0V (to keep the PMOS on). If the gate of embedded PMOS is connected to the anode of SCR (to keep the PMOS off), the SCR has a Vt1 of ~ 9.5V. The second breakdown current (It2) of the PMOS-triggered SCR devices is also obviously improved, when the gate of embedded PMOS is kept at 0V. The It2 of the PMOS-triggered SCR is about 4.5 A (4.6 A) with the layout style of structure-1 (structure-2).



(a) (b)

Fig. 9 The TLP-measured I-V curves of the PMOS-triggered SCR devices with (a) structure-1, and (b) structure-2, layout styles.

D. ESD Robustness

The HBM ESD robustness of the initial-on SCR design was measured by the *ZapMaster* ESD simulator. The failure criterion is defined as 30% I-V curve shifting from its original I-V curves at 1-μA bias. With a device width of 50 μm in a 0.25-μm fully salicided CMOS process, the HBM ESD levels of the initial-on SCR design in structure-1 and structure-2 layout styles are 5.5 kV and 6.0 kV, respectively. With a lower holding voltage in the structure-2 layout style, the ESD robustness of PMOS-triggered SCR in structure-2 is higher than that in structure-1.

IV. CONCLUSION

The novel "*initial-on*" ESD protection concept by using the PMOS-triggered SCR device with RC-based ESD detection circuit has been successfully designed and verified in a 0.25-μm salicided CMOS process. Compared to the LVTSCR, the lowest trigger voltage and the fastest turn-on speed of SCR device can be achieved by the proposed PMOS-triggered technique for effective on-chip ESD protection. Such PMOS-triggered SCR also presents a high enough holding voltage to overcome the latchup issue under the normal circuit operation condition. The ESD robustness of the PMOS-triggered SCR can be higher than 5.5 kV with a device width of as small as 50 μm.

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