A New Method for Extracting the Channel-Length Reduction and the Gate-Voltage-Dependent Series Resistance of Counter-Implanted p-MOSFET's

Chien-Min Wu, *Student Member, IEEE*, and Ching-Yuan Wu, *Member, IEEE*

***Abstract*— Based on the channel-resistance measurement, a new method for extracting the channel-length reduction $(\Delta L_{\rm jj})$ and the gate-voltage-dependent source/drain resistance $(R_{\rm SD})$ of counter-implanted p-MOSFET's is proposed, in which the necessity of the applying substrate bias is demonstrated and an empirical relationship between poly-Si gate length (L_M) and device structure parameters for $\Delta L_{\rm jj}$ extraction is provided. This is the first attempt to extract the basic parameters of counter-implanted p-MOSFET's with the LDD structure. Numerical analysis using two-dimensional (2-D) device simulator has been used to verify the proposed extraction method. Furthermore, an improved approach to extract $R_{\rm SD}$ is also presented. Both numerical analysis and experimental results show good accuracy of our proposed method.**

I. Introduction

THE accurate determination of the channel-length reduction $(\Delta L_{\rm jj})$ and the parasitic source/drain resistance $(R_{\rm SD})$ in MOSFET's becomes increasingly important for device miniaturization and optimization. Many methods [1]–[10] have been presented to extract the effective channel length based on the resistance method because of its simplicity. However, the previous investigations were almost dedicated to n-MOSFET's and had their apparent shortcomings for the LDD structure. Recently, these shortcomings have been carefully studied by two-dimensional (2-D) device numerical analysis and the algorithm for accurately extracting the metallurgical channel length of conventional and LDD n-MOSFET's has been proposed [11]. The accuracy of the proposed method in [11] has been verified by a novel technique based on the charge-pumping method [12].

For existing p-MOSFET's using the n^+-poly Si technology, counter implantation is usually applied to the channel region for lowering the threshold-voltage in modern CMOS/VLSI fabrication. Compared with existing n-MOSFET's, the major differences are that there is no metallurgical p-n junction formed along the channel surface and the conduction carriers are widely spread into the counter-implanted layer. Basically, the conduction current between source and drain diffusion islands of counter-implanted p-MOSFET's consists of two components: One is due to gate-voltage induced carriers and the other is due to the buried channel carriers. The current contributed by the gate-controlled carriers can be fundamentally modeled by the conventional $I-V$ equation, however, the equation is not suitable for describing the current contributed by the buried layer due to the different gate-bias dependence and scattering mobility. As a result, the extraction technique for the channel-length reduction of counter-implanted p-MOSFET's is different from that of n-MOSFET's. Besides, we will focus on the extraction technique for the gate-voltage-dependent $R_{\rm SD}$ because it is a by-product of $\Delta L_{\rm jj}$ extraction based on the resistance method.

In this paper, a new technique based on the resistance method for extracting $\Delta L_{\rm jj}$ of counter-implanted p-MOSFET's with either conventional or LDD structure is proposed, in which the substrate bias $(V_{\rm BS})$ is applied for accurate extraction and the threshold-voltage is determined by the iterative method. The proper selection of poly-Si gate length with applying $V_{\rm BS}$ that obtained from the numerical simulation is presented for $\Delta L_{\rm jj}$ extraction and an improved method to alleviate the discrepancy between the extracted $R_{\rm SD}$ and the actual one is proposed. In addition, the accuracy of the proposed method has been verified by 2-D device numerical analysis and the proposed method is applied to fabricated p-channel MOSFET devices with either conventional or LDD structure.

II. Extraction Method

A. $\Delta L_{\rm jj}$ *Extraction*

Fig. 1 shows the schematic cross section of a LDD p-MOSFET with counter implantation, where $L_{\rm jj}$ is the intrinsic channel length and is defined as the distance between source and drain junctions in the channel surface; $\Delta L_{\rm jj}$ $(\equiv L_M - L_{\rm jj})$ is the channel-length reduction due to lateral diffusion; L_M is the poly-Si gate length. Due to counter-implanted layer, the carrier distribution in p-MOSFET's is spread wider than that in n-MOSFET's. Therefore, the conventional $I-V$ model for effective channel length extraction will be challenged, as demonstrated by 2-D device simulation. Fig. 2 shows the simulated hole concentration along the vertical direction under various substrate biases. Evidently, the holes can be squeezed toward the SiO_2/Si interface with increasing $V_{\rm BS}$. It can be demonstrated that, as the conduction carriers are

Manuscript received November 21, 1996; revised April 3, 1997. The review of this paper was arranged by Editor M. Fukuma. This work was supported by the National Science Council, Taiwan, R.O.C. under Contract NSC-86-2215-E009-034.

The authors are with Advanced Semiconductor Device Research Laboratory and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

Publisher Item Identifier S 0018-9383(97)08298-1.

0018–9383/97$10.00 © 1997 IEEE

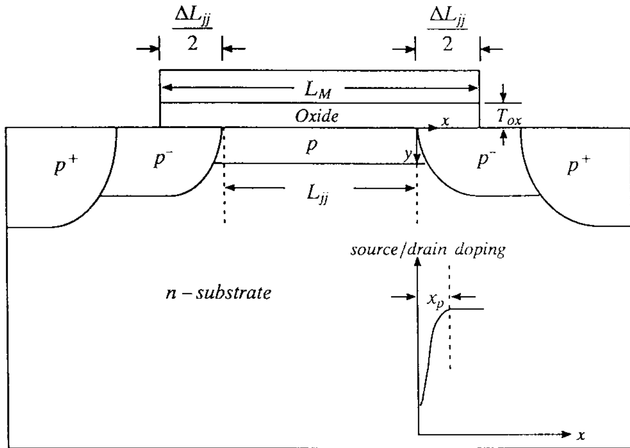


Fig. 1. The cross section view of aLDD p-MOSFET and its definitions.

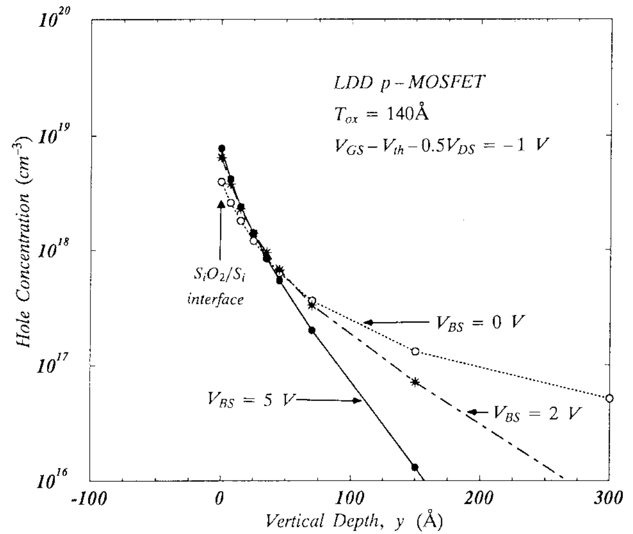


Fig. 2. The hole concentration as afunction of the vertical depth for different substrate biases and $V_{\mathrm{GS}} - V_{\mathrm{th}} - 0.5V_{\mathrm{DS}} = -1$ V.

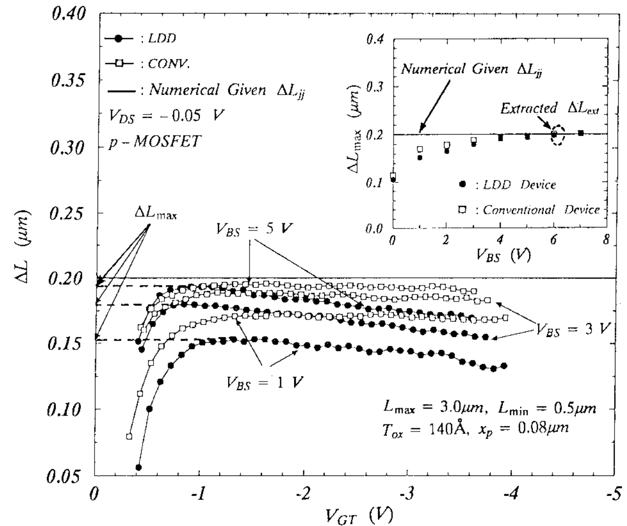


Fig. 3. The extracted ΔL versus V_{GT} at different V_{BS}'s. The insert shows the variation of local maximum $\Delta L_{\max}$ with V_{BS}. The peak value in the insert is found to be the extracted ΔL_{ext}.

integrated from the surface ($y = 0$) to $y = 40$ Å, the ratio of inversion carrier over $C_{\mathrm{ox}}V_{\mathrm{GT}}$ can be improved about 21% for $V_{\mathrm{BS}} = 5$ V when compared with $V_{\mathrm{BS}} = 0$ V. Since the high ratio corresponds to approaching to surface conduction, the application of V_{BS} is justified in order to use the conventional linear-region equation based on the charge-sheet approximation. Under higher V_{BS}, the total drain-to-source resistance for the extrinsic device operated in the linear region can be expressed as

$$R_{\mathrm{TOT}}(V_{\mathrm{GT}}) = A \times L_M + B \quad (1)$$

where $B = -A \times \Delta L + R_{\mathrm{SD}}$ and $A = (W\mu_{\mathrm{eff}}C_{\mathrm{ox}}V_{\mathrm{GT}})^{-1}$; R_{SD} is the source/drain parasitic resistance; $V_{\mathrm{GT}}(\equiv V_{\mathrm{GS}} - V_{\mathrm{th}} - \frac{1}{2}V_{\mathrm{DS}})$ is the gate-drive voltage. ΔL is the effective channel-length reduction and the others have their usual meanings. As discussed before, (1) holds only for surface-conduction devices. Due to the channel broadening effect, the intrinsic channel-resistance (R_{CH}) of counter-implanted p-MOSFET's becomes smaller. Since the bias-dependent R_{SD} can interfere ΔL_{jj} extraction [4], R_{CH} must keep much higher than R_{SD}. In this paper, the application of higher V_{BS} can ensure counter-implanted p-MOSFET to be operated in surface conduction mode and can increase the value of R_{CH}, and hence (1) is more valid for ΔL_{jj} extraction and higher accuracy is expected at larger V_{BS}.

To demonstrate the V_{BS} effect on channel length extraction, a 2-D device simulator—**SUMMOS** [13] is used to generate the I–V data. From Fig. 1, the lateral source/drain profile near the source/drain junction is approximated by Gaussian-tail function and the length of x_p is defined to be the distance between the intrinsic channel edge and the beginning diffusion-point of p^- lateral profile for LDD structure. This definition is still applicable for the conventional structure by replacing the lightly-doped region with the heavily-doped p^+ region. LDD and conventional counter-implanted p-MOSFET's with various poly-Si gate lengths (0.4 μm∼10 μm), a gate width of $W = 25$ μm, $T_{\mathrm{ox}} = 140$ Å and $x_p = 0.08$ μm are used as inputs to **SUMMOS**. It should be noted that accurate determination of the threshold voltage (V_{th}) is very important for (1) especially for small-dimension devices. The conventional linear extrapolation method is sensitive to R_{SD} and is inappropriate for threshold-voltage determination. Here, V_{th} is obtained iteratively by the normalized current method [11]. For a given V_{BS}, the family of $R_{\mathrm{TOT}} - L_M$ with various gate drives obtained by the linear regression technique can be used to establish a set of (A_i, B_i) values. According to the closely-separated-V_{GS} method [6], the extracted ΔL is gate-bias dependent. Similar extractions can be practiced by changing V_{BS}, as shown in Fig. 3. Because ΔL is V_{GT}-and V_{BS}-dependent, the determination of ΔL_{jj} from Fig. 3 is the major concern in this paper.

Fig. 3 illustrates the effects of V_{BS} and V_{GT} on the extracted ΔL for counter-implanted p-MOSFET's. The LDD device shows the stronger V_{GT}-dependence due to the carrier density modulation by the gate field in the lightly doped source/drain region. Because ΔL_{jj} is a parameter to be extracted, the electrical channel length must be prevented from V_{GT} modulation. For a given V_{BS}, ΔL is far away from the exact ΔL_{jj} as $|V_{\mathrm{GT}}|$

increases due to the extension of effective channel region, and $\Delta L_{\rm jj}$ can be approached at low $|V_{\rm GT}|$. As $V_{\rm GT}$ approaches zero, a deviation from the monotonically increasing behavior with decreasing $V_{\rm GT}$ projects the invalidity of the linear-region $I-V$ equation near the subthreshold-region operation. This physical feature is the same as those shown in [3], [4], [11]. However, the degree of this deviation is further enhanced for p-MOSFET's because the drain current is dominated by the conduction in the buried layer. The local maximum of ΔL at low $V_{\rm GT}(\Delta L_{\rm max})$ as shown in Fig. 3 can be reasonably taken as the temporarily extracted value for each $V_{\rm BS}$. Since ΔL under changing $V_{\rm BS}$ has different $\Delta L_{\rm max}$, the relationship between $\Delta L_{\rm max}$ and $V_{\rm BS}$ can be obtained, as illustrated in the insert of Fig. 3. It is clearly evident that the conventional method, which confines the channel-length reduction extracted at $V_{\rm BS} = 0$ V, is very inaccurate and the error in $\Delta L_{\rm jj}$ extraction is over 40%. As seen in the insert of Fig. 3, due to the spill-over effect of the carriers [10], $\Delta L_{\rm max}$ increases initially with $V_{\rm BS}$ and is gradually approaching the exact $\Delta L_{\rm jj}$ (i.e., 0.2 μm). As expected, this result is self-consistent with the previous analysis and demonstrates that the applying $V_{\rm BS}$ is indispensable for p-MOSFET's. This distinctive feature is very different from that of n-MOSFET's. The saturation behavior for $V_{\rm BS} \geq 5\ V$ may be regarded as the necessary condition for accurate extraction. Here, we choose the peak value (see the insert of Fig. 3) as the extracted channel-length reduction $\Delta L_{\rm ext}$.

In addition to the $V_{\rm BS}$ effect, we also find that the choice of L_M combination can slightly influence the extracted values, as pointed out in [8], [9]. Fig. 4(a) shows the different extracted results. Note that $L_{\rm max}$ and $L_{\rm min}$ denote the maximum and minimum poly-Si gate lengths used for extraction, respectively. The deviations from the given value are considered to be caused by the small-dimension effect and the fluctuations in linear regression process [9], and the error should be corrected. As shown in Fig. 4(a), the intersecting point for the extracted $\Delta L_{\rm ext}$ equal to $\Delta L_{\rm jj}$ with each curve determines the gate length (i.e., $L'_{\rm max}$) needed for correct extraction. Careful examination of $L'_{\rm max} \times L_{\rm min}$ versus $L_{\rm min}$, we find that the product of $L'_{\rm max} \times L_{\rm min}$ is nearly independent of the selected $L_{\rm min}$. This makes the L_M combination choice more flexible with only keeping the value of $L'_{\rm max} \times L_{\rm min}$. To complete the numerical analysis, different oxide thickness ($T_{\rm ox} = 100\sim250$ Å) and source/drain lateral diffusion profiles ($x_p = 0.04\sim0.16$ μm) are used to construct $L'_{\rm max} \times L_{\rm min}$ by directly comparing with the exact given $\Delta L_{\rm jj}$. The data points shown in Fig. 4(b) are determined under the applying $V_{\rm BS}$ and each point coincides with the given value. It's interesting that the data points with different stucture parameters locate on their universal curves. An empirical equation is used to fit the data points, which reads

$$L'_{\rm max} \times L_{\rm min} = \begin{cases} b_1 \times x_p + b_0 & \text{for CONV. devices} \\ b'_1 \times \frac{x_p}{T_{\rm ox}} + b'_0 & \text{for LDD devices} \end{cases} \quad (2)$$

where x_p and $T_{\rm ox}$ are in μm. The lines in Fig. 4(b) are generated by (2) with $b_1 = 4.28$ μm, $b_0 = 0.25$ μm^2 and $b'_1 = 0.28$ μm^2, $b'_0 = 0.06$ μm^2. It is shown that different source/drain doping gradient can affect the extraction result. In [3], Sun *et al.* had proposed that the extraction error in $\Delta L_{\rm jj}$ can be minimized whenever the modulated $R_{\rm SD}$ is much less than the change in $R_{\rm CH}$. Since the gradual junction profile (larger x_p) has the increasingly gate-modulated $R_{\rm SD}$, choosing the longer L_M as the reference device is needed to suppress the extraction error. For this reason, the gate voltage can easily modulate the lightly doped source/drain, $L'_{\rm max} \times L_{\rm min}$ exhibits much stronger structure-dependences on $T_{\rm ox}$ and x_p for LDD devices. Moreover, compared to conventional device, LDD device has the larger value of $R_{\rm SD}$ and this reflects that longer L_M combination for $\Delta L_{\rm jj}$ extraction is essential in order to reduce the interference of $R_{\rm SD}$. Hence, $L'_{\rm max} \times L_{\rm min}$ has the larger value as shown in Fig. 4(b). On the other hand, for the conventional structure with heavy doping, the $R_{\rm SD}$ value mainly depends on the source/drain doping gradient but is hardly influenced by gate field, and hence, $T_{\rm ox}$ plays only a minor role in $\Delta L_{\rm jj}$ extraction. So, $L'_{\rm max} \times L_{\rm min}$ becomes $T_{\rm ox}$-independent and is related to x_p only. As can be seen in Fig. 4(b), when $L'_{\rm max} \times L_{\rm min} = 2.4$ μm^2 is used, $\Delta L_{\rm ext}$ with $T_{\rm ox} = 100$ Å and $x_p = 0.08$ μm can be accurately determined to be 0.201 μm ($\Delta L_{\rm jj} = 0.2$ μm) for LDD devices. However, for the case of $T_{\rm ox} = 140$ Å and $x_p = 0.08$ μm, the extracted $\Delta L_{\rm ext}$ is 0.231 μm if $L'_{\rm max} \times L_{\rm min} = 2.4$ μm^2 is still used for extraction, and the extraction error is about 16%, as shown in Fig. 4(a). This suggests that, to extract $\Delta L_{\rm jj}$ accurately, $L'_{\rm max} \times L_{\rm min}$ must be properly chosen for devices with different technologies, especially for LDD devices. The extracted channel-length reduction $\Delta L_{\rm ext}$ according to (2) can be assigned to be $\Delta L_{\rm jj}$.

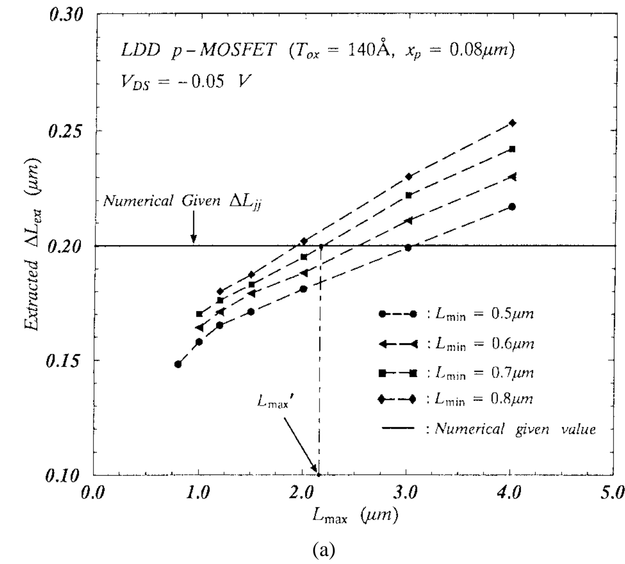
To further verify the validity of the proposed extraction method, the numerical devices with different channel profile, lateral diffusion ratio of source/drain island, contact resistance, or $\Delta L_{\rm jj}$ are also examined. The proposed method is implemented to extract the channel-length reduction and the extracted value is directly compared with the given value. The extraction results have demonstrated that the extraction errors in channel-length reduction are within 3% and good accuracy can be obtained. This indicates that the proposed extraction method is valid for the counter-implanted p-MOS device.

B. $R_{\rm SD}$ *Extraction*

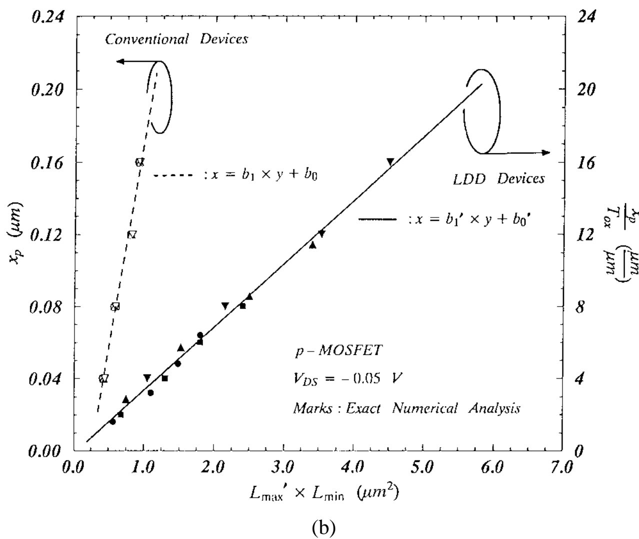
In this study, $R_{\rm SD}$ is defined as the parasitic resistance outside $L_{\rm jj}$ and, therefore, the gate-voltage-dependence of $R_{\rm SD}$ can be theoretically obtained by drawing a vertical line at $L_M = \Delta L_{\rm jj}$ in the $R_{\rm TOT} - L_M$ plot and the intercepts with these straight lines give $R_{\rm SD}(V_{\rm GT})$. It means that $R_{\rm SD}(V_{\rm GT})$ can be determined by

$$R_{\rm SD}(V_{\rm GT}) = A_i \times \Delta L_{\rm jj} + B_i. \quad (3)$$

Fig. 5 shows comparisons between numerical analysis and extracted $R_{\rm SD}$. It is clearly seen that the extracted results are underestimated and the deviation is enhanced for low $V_{\rm GT}$. The insert in Fig. 5 can explain this phenomenon. Obviously, the calculated A_i across the intrinsic channel region is assumed to be constant for the extraction method and its magnitude is nearly equal to the exact numerical value at the middle point of the channel. However, the channel resistance near



(a)



(b)

Fig. 4. (a) $\Delta L_{\rm ext}$ versus $L_{\max}$ for different $L'_{\min}s$. $L'_{\max}$ means the mask length needed for correct extraction; (b) $x_p(x_p/T_{\rm ox})$ versus $L'_{\max} \times L_{\min}$ for conventional (LDD) devices. The data points are extracted from the numerical simulation and the lines are computed from (2).

the source/drain junction in real situation is less modulated. This is partially attributed to the fact that some normal electric fields under the gate are terminated by the source/drain island; the other is that there exists the ambiguous junction between the channel surface and the source/drain island due to the counter-implanted channel. Therefore, the source/drain diffusion tail can extend into the counter-implanted channel and the excess holes near the source/drain junction will be increased. These excess holes behave as if they are a part of the source/drain diffusion region. As a consequence, these two effects overestimate the extracted $R_{\rm CH}$ and lead to the underestimation of the extracted $R_{\rm SD}$. Fig. 5 also shows that, even for higher $V_{\rm GT}$, the deviation of $R_{\rm SD}$ between them can be still observed. This can be explained by the carrier spill-over effect near the source/drain. Based on this understanding, we cannot accurately determine both $\Delta L_{\rm jj}$ and $R_{\rm SD}$ simultaneously, but an effective length can be defined by integrating the exact numerical curve and dividing by A_i, as shown in the insert of Fig. 5. Therefore, the length reduction, which satisfies the exact $R_{\rm SD}$, can be evaluated by

$$\Delta L'(V_{\rm GT}) = L_M - \frac{R_{\rm CH,num}(V_{\rm GT})}{A_i(V_{\rm GT})} \tag{4}$$

where $R_{\rm CH,num}(V_{\rm GT})$ is calculated by $\int_0^{L_{\rm jj}} \frac{dR}{dx}\, dx$, and the increased amount in $\Delta L_{\rm jj}$ is

$$\delta \equiv \Delta L' - \Delta L_{\rm jj}. \tag{5}$$

Fig. 6 shows the calculated results for p-MOSFET's with various device parameters, in which different given $\Delta L_{\rm jj}$'s are also examined. The average δ for all $V_{\rm GT}$'s ($\Delta \equiv {\rm Ave}(\delta)$) is plotted in the insert of Fig. 6. As pointed out before, the underestimation of $R_{\rm SD}$ is due to the lateral electric field emanating from the source/drain island and the carrier spill-over effect. However, the change of $V_{\rm GT}$ ($|V_{\rm GT}| > 1$ V) and $T_{\rm ox}$ can only affect the normal field. For this reason, $\Delta L'$ is nearly independent of the variations of $V_{\rm GT}$ and $T_{\rm ox}$. As shown in the insert of Fig. 6, the variation ranges of Δ for the LDD and conventional structures are strictly confined to about 0.031 μm ($\equiv \Delta_1$) and 0.021 μm ($\equiv \Delta_2$), respectively. It should be noted that the doping level in the LDD structure (10^{18} cm^{-3}) is much less than that in the conventional structure (10^{20} cm^{-3}), leading to the reduction of the lateral field and the stronger control capability of the normal gate-field near the channel edge. As a result, the larger $\Delta L'$ can be expected due to the reduced dR/dx, and hence the correction term of LDD devices (Δ_1) has the larger value. Although a steep source/drain junction profile can slightly increase the lateral field, it is the second-order effect. Based on this observation, Δ represents the average length over which the source/drain junctions are blurred and its amount is much dependent on the source/drain doping level. For simplicity, $R_{\rm SD}(V_{\rm GT})$ of p-MOSFET's can be newly extracted as

$$R_{\rm SD}(V_{\rm GT}) = A_i \times (\Delta L_{\rm jj} + \Delta) + B_i. \tag{6}$$

As discussed previously, Δ looks as if the extension of the source/drain for counter-implanted p-MOSFET's. Although Δ may depend on different technologies, its physical reason for its nonvanishing value has been clearly stated. Fig. 7 shows comparisons of $R_{\rm SD}$ between numerical analysis and improved extraction method for LDD devices. Note that the universal property can be observed from the numerical data of $R_{\rm SD} - V_{\rm GT}$ for various $V_{\rm BS}$. For $|V_{\rm GT}| > 1$ V the devices are operated in turn-on linear-region, the extracted $R_{\rm SD}$ is very accurate and is consistent with $\Delta L_{\rm jj}$. It also shows that some deviations can be still observed for lower $V_{\rm GT}$ because the drain current is dominated by subthreshold conduction in the buried-layer. In this region, due to the linear-region $I{-}V$ equation used, the drain current will be overestimated and $R_{\rm CH}$ will be underestimated, and therefore, it leads to the slightly overestimation of $R_{\rm SD}$. Nevertheless, the agreements are quite good for wide-range $V_{\rm GT}$ and various device sructure parameters. As compared to counter-implanted p-MOSFET's, the actual dR/dx near the source/drain junction is nearly equal to the extracted value at the middle point of the channel for n-MOSFET's because the lateral field of abrupt p-n junction is

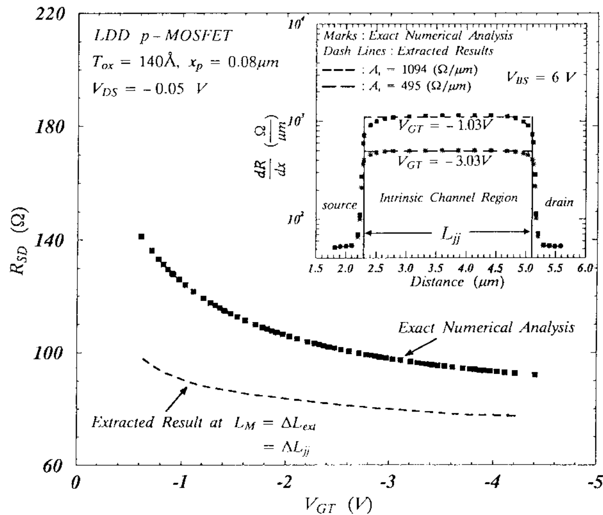


Fig. 5. Comparisons between numerical analysis and extracted $R_{\rm SD}$ at $L_M = \Delta L_{\rm ext} (= \Delta L_{\rm jj})$ for LDD device. The insert shows comparisons of dR/dx between numerical analysis and extraction results for various $V'_{\rm GT}s$.

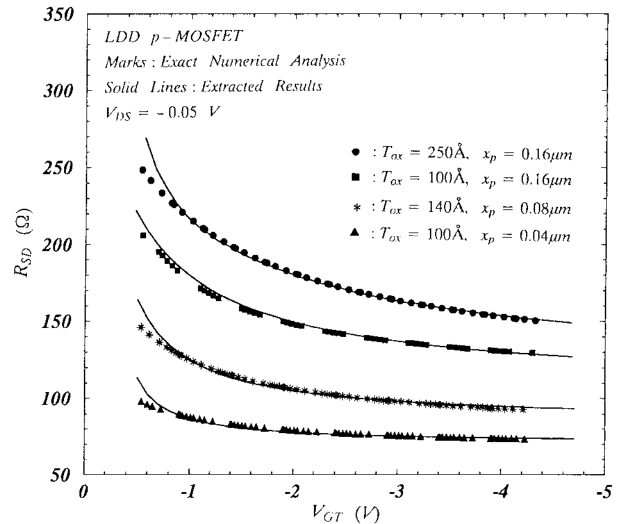


Fig. 7. Comparisons between numerical analysis and extracted $R_{\rm SD}$ at $L_M = \Delta L_{\rm jj} + \Delta$ [see (6)] for LDD devices with different device structure parameters.

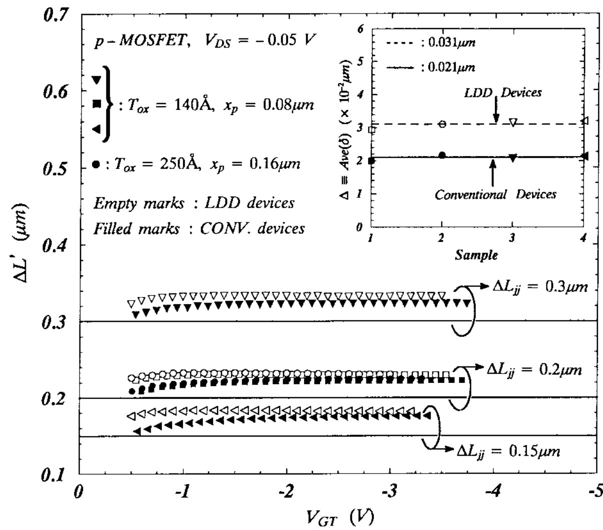


Fig. 6. $\Delta L'$ versus $V_{\rm GT}$ for conventional and LDD p-MOSFET's with various $T_{\rm ox}, x_p$, and $\Delta L_{\rm jj}$. The insert shows the variations of Δ for these devices.

much higher and the carrier spill-over effect doesn't occur, and hence Δ can be neglected, as shown in [11]. This distinctive feature is different from that of p-MOSFET's.

III. Application to Fabricated Devices

Several sets of experimental counter-implanted p-MOSFET's are tested here. The first set was fabricated by the 0.5 μm n-well CMOS technology with $T_{\rm ox} = 110$ Å for both conventional and LDD structures. The second and third sets used consist of a series of p-channel LDD MOSFET's fabricated using the 0.7-μm technology with $T_{\rm ox} = 140$ Å and the 1.0-μm technology with $T_{\rm ox} = 198$ Å, respectively. All devices have the same poly-Si gate width ($W = 25$ μm), and the $I-V$ data are measured at $V_{\rm DS} = -0.05$ V by HP4145B. For practical application, we assume that the lateral doping in the p$^-$ region along the surface begins to diffuse at the poly-Si gate edge (i.e., $x_p = \Delta L_{\rm jj}/2$), and this can be reasonably regarded as the general/central case for the actual devices. We first take a fixed $L_{\rm min}$ and choose different $L_{\rm max}$ to extract the corresponding $\Delta L_{\rm ext}$. Similar calculations can be performed by changing $L_{\rm min}$ and x_p is evaluated by $\Delta L_{\rm ext}/2$. The extracted results are shown in the insert of Fig. 8 and (2) for LDD devices is also plotted for extraction. It is observed that the intersecting points for various curves with (2) are nearly confined at a common point when $L_{\rm min}$ is varying from 0.65 μm to 0.9 μm. This feature clearly demonstrates that our extraction method is very reliable. Then, the channel-length reduction can be determined by

$$\Delta L_{\rm jj} = 2 \times x_{p0} \tag{7}$$

where x_{p0} is y-value at the intersecting point times $T_{\rm ox}$. Similar procedure can be performed for conventional devices. Applying our extraction method and the conventional method to the experimental devices, comprehensive extraction results are listed in Table I. TK57097-2 and TK57097-10 are the conventional devices but have different implanted doses in n-well and counter-implanted layer. It is clearly seen that the values of extracted $\Delta L_{\rm jj}$ (0.198 and 0.194 μm) are very close for our extraction method. This fact supports that, for conventional structures with heavily doped source/drain, the channel-length reduction is less sensitive to the change of implantation dosages because the lateral profile near the source/drain junction has a steep gradient. TK57097-11 and TK57097-15 have the same LDD structure parameters except for $V_{\rm th}$ adjustment, and BF_2^+ implant was added in the channel region with an energy of 50 KeV. The former is implanted with a dose of $2.4 \times 10^{12}/{\rm cm}^2$ and the latter with a dose of $2.9 \times 10^{12}/{\rm cm}^2$. As a result, the spill-over length of carrier concentration for TK57097-15 is longer than that of TK57097-11 due to higher dosage. This behavior looks like the extension of the source/drain region, hence the extracted $\Delta L_{\rm jj}$ for TK57097-15 is larger than that of TK57097-11.

TABLE I
THE EXTRACTED RESULTS FROM EXPERIMENTAL DEVICES USING THE CONVENTIONAL METHOD AND OUR EXTRACTION METHOD

Set No.	*Wafer No.*	T_{ox}(Å)	ΔL_{jj} (μm) (*Conventional method*)	ΔL_{jj} (μm) (*Our method*)
1	*TK*57097 – 2 (*CONV.*)	110	0.163	0.198
	*TK*57097 – 10 (*CONV.*)	110	0.152	0.194
	*TK*57097 – 11 (*LDD*)	110	0.137	0.233
	*TK*57097 – 15 (*LDD*)	110	0.192	0.260
2	*TK*55001 (*LDD*) 3431 – 04	140	0.084	0.148
3	*TC*5701*C* (*LDD*) 3214 – 19	198	0.215	0.291

† *CONV.* : *Conventional structure*

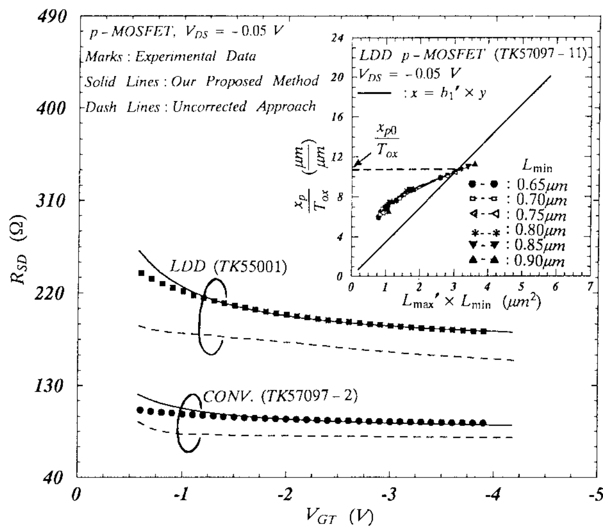


Fig. 8. Comparisons between experimental data and extracted $R_{\rm SD}$. The extracted results of the improved method and the original one [see (3)] are also compared. The insert shows the application of (2) to the extraction of the channel-length reduction for experimental devices.

Obviously, a larger wide-range variation of $\Delta L_{\rm jj}$ can also be observed. Due to the ambiguous junction for the LDD structures, the channel-length reduction is much influenced by the lateral doping gradient. This implies that careful monitor of the fabrication process is absolutely needed to precisely control its value. More evidence of our extracted $\Delta L_{\rm jj}$ has been examined by comparing the DIBL and punchthrough effects of experimental short-channel p-MOSFET devices using a 2-D numerical simulator. Simulation results using our extraction value show good agreements with the measured subthreshold characteristics (DIBL & punchthrough) for short-channel devices. However, the conventional method always gives the lower value of $\Delta L_{\rm jj}$, leading to the underestimation of the simulated subthreshold $I-V$.

To demonstrate the validity of the extraction method for $R_{\rm SD}$, both of conventional (TK57097-2) and LDD (TK55001) devices are tested. In general, $R_{\rm SD}$ is composed of the contact resistance, the sheet resistance, the spreading resistance, and the accumulation layer resistance. For purely experimental measurements, it is very difficult to obtain the reliable $R_{\rm SD}$ due to the limited resolution of the equipment. Over the past years, the use of a 2-D device simulator has proven to be particularly useful to obtain realistic $R_{\rm SD}$. In this paper, the simulation output data from **SUMMOS** are analyzed by a post-processor program, and then the exact $R_{\rm SD}$ can be evaluated through the simulated values of the hole quasi-Fermi potentials in the device structure and the total drain current [8]. Therefore, the basic device parameters are calibrated first by 2-D device simulator. This method employed in determining experimental $R_{\rm SD}$ as a function of $V_{\rm GT}$ is very reliable. Fig. 8 shows experimental data and extracted $R_{\rm SD}$, and the extracted results of the proposed method and the uncorrected approach are also compared. The values of $\Delta L_{\rm jj} + \Delta$ for TK57097-2 and TK55001 used in the offset method are 0.219 μm and 0.179 μm, respectively. The reason for the deviation between experimental data and our proposed method at very low $V_{\rm GT}$ has been explained in the previous section. Although this small deviation occurs, good agreements for wide-range $V_{\rm GT}$ can be obtained by the proposed method, while (3) shows poor accuracy. Therefore, the extraction method has its physical meanings.

IV. CONCLUSION

A new method based on channel-resistance measurement to extract both the channel-length reduction ($\Delta L_{\rm jj}$) and the gate-voltage-dependent source/drain resistance ($R_{\rm SD}$) for counter-implanted p-MOSFET's has been proposed. The iterative threshold-voltage determination has been implemented into the extraction method. Moreover, we particularly emphasizes on the application of the substrate bias to extract $\Delta L_{\rm jj}$ and its validity has been justified. Since conventional and LDD p-MOSFET's have different source/drain structures, LDD devices show the stronger gate-dependence of ΔL and $R_{\rm SD}$. With applying $V_{\rm BS}$, the empirical equation of $L'_{\rm max} \times L_{\rm min}$ has been established by our numerical simulation and the relationship is reflected from the different degree of gate modulation in the source/drain region. It can provide a guide for the choice of poly-Si gate length combination for $\Delta L_{\rm jj}$ extraction and can be well appilcable to our experimental devices. Simulations on the subthreshold $I-V$ using our extracted $\Delta L_{\rm jj}$ show good agreements with the measured data. This paper also demonstrates that the extracted $R_{\rm SD}$ will be underestimated if the extracted channel-length reduction is exactly equal to $\Delta L_{\rm jj}$, and this can be attributed to the ambiguous junction and the shielding effect of lateral electric field near the source/drain edge. The offset length Δ is introduced to account for these effects. Substituting $\Delta L_{\rm jj} + \Delta$ for $\Delta L_{\rm jj}$, satisfactory agreements can be obtained. Both numerical analysis and experimental results show good accuracy and reliability of the proposed extraction method.

REFERENCES

[1] K. Terada and H. Muta, "A new method to determine effective MOSFET channel length," *Jpn. J. Appl. Phys.*, vol. 18, p. 953, 1979.
[2] J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "A new method to determine MOSFET channel length," in *IEEE Electron Device Lett.*, vol. EDL-1, p. 170, 1980.

[3] J. Y. C. Sun, M. R. Wordeman, and S. E. Laux, "On the accuracy of channel length characterization of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, p. 1556, 1986.
[4] G. J. Hu, C. Chang, and Y. T. Chia, "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-34, p. 2469, 1987.
[5] D. J. Mountain, "Application of electrical effective channel length and external resistance measurement techniques to a submicrometer CMOS process," *IEEE Trans. Electron Devices*, vol. ED-36, p. 2499, 1989.
[6] J. Ida, S. Ishii, and F. Ichikawa, "Accurate characterization of gate-n^- overlapped LDD with the new $L_{\rm eff}$ extraction method," in *IEDM Tech. Dig.*, 1990, p. 219.
[7] K. K. Ng and J. R. Brews, "Measuring the effective channel length of MOSFET's," *IEEE Circuits and Devices Mag.*, vol. 6, p. 33, 1990.
[8] S. E. Laux, "Accuracy of effective channel length/external resistance extraction algorithm for MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-31, p. 1245, 1984.
[9] K. Terada, "Suppression of measurement errors in effective-MOSFET-channel-length extraction," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, 1992, p. 208.
[10] S. Hong and K. Lee, "Extraction of metallurgical effective channel length in LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, p. 1461, 1995.
[11] Y. S. Jean and C. Y. Wu, "A new extraction algorithm for the metallurgical channel length of conventional and LDD MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-43, p. 946, 1996.
[12] H. H. Li and C. Y. Wu, "A novel extraction technique for the effective channel length of MOSFET devices," *IEEE Trans. Electron Devices*, vol. ED-42, p. 856, 1995.
[13] R. K. Perng, P. S. Lin, and C. Y. Wu, "A new methodology for developing a fast two-dimensional MOSFET device simulator," *Solid-State Electron.*, vol. 34, p. 635, 1991.

Chien-Min Wu (S'92) was born in Tainan, Taiwan, R.O.C., on July 14, 1967. He received the B.S. degree in electrical engineering from National Central University, Taiwan, in 1990. Since 1991, he has been pursuing the Ph.D. degree at the Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan. His current research interests focus on characterization and modeling for counter-implanted p-MOSFET's.

Ching-Yuan Wu (M'72) was born in Taiwan, R.O.C., on March 18, 1946. He received the B.S. degree from the Department of Electrical Engineering, National Taiwan University, Taipei, in 1968, and the M.S. and Ph.D. degrees from the State University of New York (SUNY) at Stony Brook, in 1970 and 1972, respectively.

During the 1972–1973 academic year, he was appointed as a Lecturer at the Department of Electrical Sciences, SUNY, Stony Brook. During the 1973–1975 academic year, he was a Visiting Associate Professor at National Chiao-Tung University (NCTU), Hsinchu, Taiwan. In 1976, he became a Full Professor in the Department of Electronics and the Institute of Electronics, NCTU. At NCTU, he was the Director of Engineering Laboratories and Semiconductor Research Center from 1974 to 1980; the Director of the Institute of Electronics from 1978 to 1984; and the Dean, College of Engineering, from 1984 to 1990. He was a principal investigator of the National Electronics Mass Plan-Semiconductor Devices and Integrated-Circuit Technologies from 1976 to 1979, and a Coordinator of the National Microelectronics Researches and High-Level Man-Power Education Committee, National Science Council, R.O.C., from 1982 to 1988. He has been the Research Consultant of the Electronics Research and Service Organization (ERSO), ITRI; a member of the Academic Review Committee, the Ministry of Education; and the Chairman of the Technical Review Committee on Information and Microelectronics Technologies, the Ministry of Economic Affairs. His research activities have been in semiconductor device physics and modelings, Integrated-circuit designs and Technologies. His present research areas focus on the developments of efficient 2-D and 3-D simulators for deep-submicrometer semiconductor devices, design rules and optimization techniques for deep-submicrometer CMOS devices, and key technologies for deep-submicrometer CMOS devices. He has published over 180 papers in the semiconductor field and has served as a reviewer for international journals such as IEEE ELECTRON DEVICE LETTERS, IEEE TRANSACTIONS ON ELECTRON DEVICES, and *Solid-State Electronics*.

Dr. Wu is a member of the Honorary Editorial Advisory Board of Solid-State Electronics. He received the Academic Research Award in Engineering from the Ministry of Education (MOE), in 1979 and the outstanding Scholar Award from the Chinese Educational and Curtural Foundation in 1985. He has received the Outstanding Research Professor Fellowship from the Ministry of Education and the National Science Council (NSC), R.O.C. He received the Distinguished Engineering Professor Medal Award from the Chinese Engineering Society in 1992.