# A New Method for Extracting the Counter-Implanted Channel Profile of Enhancement-Mode p-MOSFET's

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*Abstract*— A new methodology is proposed to extract the nonuniform channel doping profile of enhancement mode p-MOSFET's with counter implantation, based on the relationship between device threshold voltage and substrate bias. A self-consistent mathematical analysis is developed to calculate the threshold voltage and the surface potential of counter-implanted long-channel p-MOSFET at the onset of heavy inversion. Comparisons between analytic calculation and two-dimensional (2-D) numerical analysis have been made and the accuracy of the developed analytic model has been verified. Based on the developed analytic model, an automated extraction technique has been successfully implemented to extract the channel doping profile. With the aid of a 2-D numerical simulator, the subthreshold current can be obtained by the extracted channel doping profile. Good agreements have been found with measured subthreshold characteristics for both long- and short-channel devices. This new extraction methodology can be used for precise process monitoring and device optimization purposes.

## NOMENCLATURE

| | |
|---|---|
| $E(y_d)(E(y_{d\max}))$ | Built-in electric field at the depletion (maximum depletion) edge. |
| $L(W)$ | Mask channel length (width). |
| $N_D(y)(N_A(y))$ | Non-uniform donor (acceptor) doping profile in the substrate. |
| $p(y)(n(y))$ | The hole (Electron) concentration distribution. |
| $Q_{\text{sc}}(Q_I)$ | Space-charge (Inversion-charge) density per unit area. |
| $V_{\text{GS}i}$ | Extrapolated gate voltage at $I_{\text{DS}} = 0$. |
| $V_{\text{GS}x}$ | Gate voltage for the maximum transconductance. |
| $y_d(y_{d\max})$ | Depletion (Maximum depletion) width under the gate. |
| $\Psi_{\sin v}$ | Surface potential at threshold. |
| $\phi_F$ | The Fermi potential in the bulk. |
| $\phi_s$ | Surface potential without considering the drain bias effect. |
| $\phi_t$ | Thermal voltage. |
| $\phi(y_d)(\phi(y_{d\max}))$ | Built-in potential at the depletion (maximum depletion) edge. |
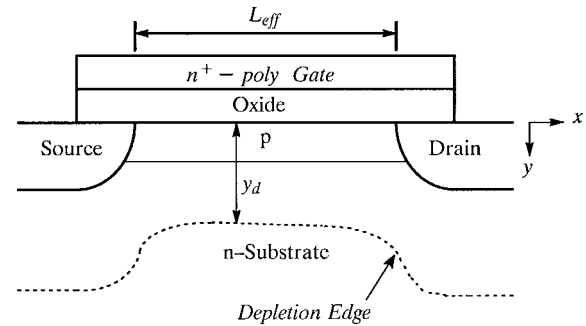
Fig. 1. The cross section view of a conventional p-MOSFET with counter implantation.

## I. INTRODUCTION

CMOS technology has become a major trend in existing VLSI circuits due to its low power dissipation, however, the modeling efforts spent on p-MOSFET's are quite limited. To achieve comparable threshold voltage for both n- and p-channel devices in CMOS circuits, counter implantation is usually applied to the channel region of p-MOSFET's in the well-established $n^+$-poly silicon technology. Moreover, the deep phosphorus implant for punchthrough suppression, which can reduce the DIBL effect [1], [2], is commonly used in modern VLSI technology. Fig. 1 shows the cross-sectional view of a typical p-MOSFET with counter implantation, in which a p-n junction is formed near the channel surface and the operation mode of this device depends on the device structure parameters [3], [9].

Many methods [4]–[8] have been proposed to profile the channel implant in MOSFET. Secondary ion mass spectrometry (SIMS) [4] and spreading resistance profile (SRP) [5] are often used but these methods suffer from the destruction of semiconductor wafer. The capacitance measurement had been proposed [6], however, it subjects to the Debye limit and is not suitable for deep submicron MOSFET's. Another technique to extract the channel profile is based on the current–voltage method. The $V_{\text{BS}}$-$V_{\text{GS}}$ technique [7] is based on constant drain current corresponding to constant inversion charge, which requires a correction in the analysis because the effective MOSFET mobility varies with $V_{\text{GS}}$. Recently, the threshold voltage method [8] has been modified and used for the device with nonuniformly doped channel profile. However, the detailed profile near the surface within 0.1 $\mu$m is still unknown. This disadvantage will lead to the error of the simulated subthreshold current. Moreover, $Q_I$ above threshold cannot be predicted accurately.

TABLE I
STRUCTURE PARAMETERS OF THE DEVICE
USED FOR EXACT NUMERICAL SIMULATION

| Parameter | value |
|---|---|
| $T_{ox}(\text{Å})$ | 140 |
| $W/L(\mu m/\mu m)$ | 25/25 |
| $D_{I1}(10^{12}cm^{-2})$ | -0.8 |
| $\Delta R_{P1}(10^{-5}cm)$ | 0.4 |
| $R_{P1}(10^{-5}cm)$ | 0.3 |
| $D_{I2}(10^{12}cm^{-2})$ | 4.0 |
| $\Delta R_{P2}(10^{-4}cm)$ | 0.45 |
| $R_{P2}(10^{-4}cm)$ | 0.25 |
| $N_B(10^{14}cm^{-3})$ | 3.0 |

In this paper, a new extraction methodology to extract the channel doping profile of enhancement-mode p-MOSFET's with counter implantation is proposed. With the aid of the *threshold-voltage fitting* method and two-dimensional (2-D) numerical simulator, the proposed method becomes very efficient and accurate. The merit of this method is to measure the current–voltage ($I-V$) characteristics directly, and no special large test structure is required. Since the *threshold-voltage fitting* method is used for profile extraction, the accurate $V_{\text{th}}$ model is needed. Due to nonuniformly doped substrate, a self-consistent analysis is developed to calculate the threshold voltage and the onset of heavy inversion in Section II. The accuracy of the new analysis has been verified by exact 2-D numerical analysis. In Section III, the *threshold-voltage fitting* method is described. Applications and discussions of the new methodology to extract actual doping profile are given in Section IV. Conclusions are summarized in the final section.

## II. ONE-DIMENSIONAL THRESHOLD-VOLTAGE MODEL

Due to channel implantation in MOS devices, Booth *et al.* [9] had shown that the surface potential at the threshold condition for all the extraction methods is not equal to the conventional $2\phi_F$ for the nonuniformly doped substrate. In general, the threshold voltage is usually determined experimentally from $I-V$ characteristics by linear extrapolation method, and the discrepancy and inconsistency between the definitions of $\Psi_{\sin v}$ and $V_{\text{th}}$ can be expected. Antoniadis [11] had first proposed an algorithm to directly calculate $V_{\text{th}}$ from the extrapolation $Q_I-V_{\text{GS}}$ curve, and the problem of defining $\Psi_{\sin v}$ was still overlooked. Moreover, there is a questionable assumption that the linear part of $Q_I$ versus $V_{\text{GS}}$ occurs at the vicinity of $Q_{I0} = 3 \times 10^{-8}$ coul/cm$^2$. In practice, the theoretical analysis and simulation show that $Q_{I0}$ is not exactly equal to this magic number but depends on the device structure parameters. In this section, we will introduce a new mathematical analysis to calculate the $V_{\text{th}}$ and $\Psi_{\sin v}$ self-consistently.

For the implanted profile, the excess profile $N_{\text{CH}}(y)$ ($\equiv N_D(y) - N_A(y)$) can be approximated by the superposition of Gaussian distributions

$$N_{\text{CH}}(y) = \sum_i \frac{D_{\text{I}i}}{\sqrt{2\pi}\Delta R_{\text{P}i}} \cdot \exp\left[-\left(\frac{y+T_{\text{ox}}-R_{\text{P}i}}{\sqrt{2}\Delta R_{\text{P}i}}\right)^2\right] \tag{1}$$
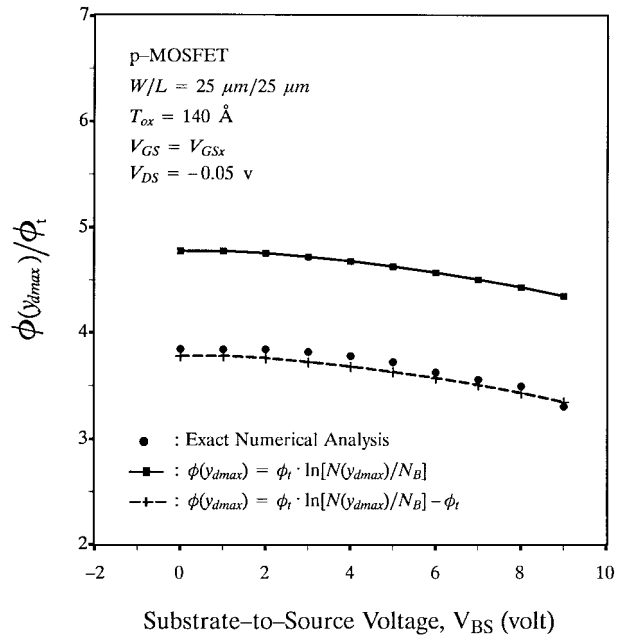


Fig. 2. Comparisons between approximation (c), conventional $\phi(y_{d\max})$, and the numerically generated built-in voltage at the depletion edge.

where $D_{\text{I}i}$, $R_{\text{P}i}$, and $\Delta R_{\text{P}i}$ are the dose, range, and straggling of the $i$-th implantation, respectively. Note that $D_{\text{I}i}$ is not the total dose implanted into the substrate as the dosage loss in $y < 0$ is also included in $D_{\text{I}i}$.

To compute $V_{\text{th}}$, we use the following assumptions [10]:

(a) The depletion width reaches its maximum value ($y_d = y_{d\max}$) when the gate voltage is equal to the threshold voltage.

(b) No electron distribution within the depletion region for $p$-channel devices.

(c) $\phi(y_{d\max}) \approx \phi_t \ln\left[\frac{N(y_{d\max})}{N_B}\right] - \phi_t$, where $N_B$ is the base concentration in the substrate and $N(y_{d\max})$ ($= N_{\text{CH}}(y_{d\max}) + N_B$) is the net doping at the maximum depletion edge.

(d) $E(y_{d\max}) \approx -\frac{\phi_t}{N(y)} \cdot \frac{dN(y)}{dy}\big|_{y=y_{d\max}}$

To examine the validity of assumptions, a 2-D device simulator—**SUMMOS** (**SU**b **M**icron **MOS**FET) [17] is used and Table I lists the structure parameters used. According to the definition of depletion width [10], the built-in electric field at the defined depletion edge is not equal to zero but is negligibly small. Approximation (d) is derived by assuming the thermal equilibrium and, in general, it can hardly affect the $V_{\text{th}}$ calculation for its small value. Due to the charge exchange of electrons, the charge neutrality is not valid at the depletion-layer edge, and this effect has been considered in approximation (c) by using conventional value minus $\phi_t$. Fig. 2 is presented to demonstrate good agreement between approximation (c) and simulated $\phi(y_{d\max})$ for various substrate biases.

Using these assumptions, we can easily obtain [10]

$$Q_{\text{sc}}(y_{d\max}) = q \int_0^{y_{d\max}} N(y)\,dy - \epsilon_{\text{si}} \cdot E(y_{d\max}) \tag{2}$$

$$Q_I(y_{d\max}) = q \int_0^{y_{d\max}} p(y)\, dy \tag{3}$$

and

$$\phi_s = V_{BS} + \phi(y_{d\max}) + y_{d\max} \cdot E(y_{d\max})$$
$$- \frac{q}{\epsilon_{si}} \int_0^{y_{d\max}} y N(y)\, dy - \frac{q}{\epsilon_{si}} \int_0^{y_{d\max}} y \cdot p(y)\, dy. \tag{4}$$

It is noted that $y_{d\max}$ must first be determined. In this paper, we concentrate our attention on the surface channel conduction devices, therefore the heavy-inversion definition can be used [10]

$$\left. \frac{dQ_I}{d\phi_s} \right|_{\phi_{sc}} = \left. \frac{dQ_{sc}}{d\phi_s} \right|_{\phi_{sc}}. \tag{5}$$

This leads to the critical surface potential as

$$\phi_{sc} = -\phi_t \ln \frac{Q_{sc}(y_{d\max}) \cdot N_B}{q \cdot y_{d\max} \cdot n_i^2}. \tag{6}$$

Note that (5) is valid only when $Q_I$ is negligibly small as compared to $Q_{sc}$. (4) is eventually written as

$$\phi_{sc} = V_{BS} + \phi(y_{d\max}) + y_{d\max} \cdot E(y_{d\max})$$
$$- \frac{q}{\epsilon_{si}} \int_0^{y_{d\max}} y N(y)\, dy. \tag{7}$$

Combining (6) and (7), $y_{d\max}$ can be determined. Moreover, (3) will collapse for the buried channel conduction. The reason is that direct integration cannot be made by using the integral variable transform since $d\phi/dy = 0$ at the potential minimum point and most contribution of holes comes from this position below the surface. In this case, (6) no longer holds due to negative $Q_{sc}$. This limitation is consistent with our application which is limited to the case of surface conduction p-channel devices.

From the numerical analysis, it is found that $p(y)$ for surface conduction is nearly a Gaussian function along the vertical direction and can be approximated by

$$p(y) \approx p_s \cdot \exp\left( -\frac{y^2}{\lambda^2} \right) \quad \text{for } y \geq 0 \tag{8}$$

where $p_s$ and $\lambda$ can simply expressed as

$$p_s = \frac{n_i^2}{N_B} \cdot \exp\left( \frac{-\phi_s}{\phi_t} \right) \tag{9}$$

and

$$\lambda \approx \frac{2 \cdot Q_I}{\sqrt{\pi} \cdot q \cdot p_s}. \tag{10}$$

$p_s$ is the hole concentration at the surface and $\lambda$ is the characteristic length for hole distribution. Under the charge-sheet approximation, the potential balance equation is

$$V_{GS} = V_{FB} + \phi_s - \frac{Q_{sc}(\phi_s) + Q_I(\phi_s)}{C_{ox}} \tag{11}$$

and then $\phi_s$ at $V_{GS} = V_{GSx}$ can be iteratively calculated from (2)–(4) and (8)–(11). The surface potential at the middle point can be expressed by

$$\Psi_s = \phi_s + V_x \tag{12}$$

where $V_x$ is equal to $0.5\,V_{DS}$. Since $I_{DS}$ is proportional to $Q_I$ in the linear part of the $I_{DS}$ versus $V_{GS}$ curve, the threshold voltage can be defined as

$$V_{th} \equiv V_{GSx} - \left. \frac{Q_I}{\frac{\partial Q_I}{\partial V_{GS}}} \right|_{V_{GS}} = V_{GSx} - V_x \tag{13}$$

where the effect of $V_{DS}$ on $Q_I$ has been taken into account. It should be noted that $V_{th}$ is evaluated at $V_{GS} = V_{GSx}$ and $V_{GSx}$ can be obtained by $I{-}V$ measurement. Because the integrals can be integrated or approximated by error function, the computation time can be considerably saved.

According to this strategy, the $V_{th}$ versus $V_{BS}$ relation can be found without difficulty and $V_{GSi}$ is re-substituted into (11) to determine $\Psi_{\sin v}$ by

$$\Psi_{\sin v} = V_{GSi} - V_{FB} + \frac{Q_{sc}(\phi_{\sin v}) + Q_I(\phi_{\sin v})}{C_{ox}} \tag{14}$$

where $\phi_{\sin v}$ is the surface inversion potential at $V_{DS} = 0$ V. Fig. 3 shows $Q_I$ as a function of $V_{GS}$ for various substrate biases. Obviously, the accuracy of the developed analytic model is excellent near and beyond threshold. This result is extremely important because the calculations of $V_{th}$ and $\Psi_{\sin v}$ need accurate $Q_I$ above threshold. By contrast, the traditional definition of $V_{th}$ obtained by setting $\phi_s = \phi_{sc}$ and $Q_I = 0$ in (11) is compared with our approach. $Q_{sc}$ and the surface potential at the threshold condition versus $V_{BS}$ are shown in the insert of Fig. 4, in which the results of analytical model are compared with exact numerical analysis. Good agreements for our model can be observed and underestimation of surface potential shows the deficiency of the traditional method. Note that $\Psi_{\sin v}$ increases with $V_{BS}$, while it tends to saturate as $V_{BS}$ is high. This behavior is attributed to the squeezed effect of inversion-charge. Fig. 4 also shows comparisons among our $V_{th}$ model (solid curve), traditional approach (dash curve), and numerical data, and the agreements are quite good for our model. Furthermore, considerable discrepancy between numerical analysis and traditional approach due to inconsistent $V_{th}$ definition can be observed. With the high accuracy of $V_{th}$ calculation, the *threshold-voltage fitting* method can be used to extract the nonuniformly doped channel profile.

## III. THE THRESHOLD-VOLTAGE FITTING METHOD

The $I{-}V$ characteristics of a long-channel device are not affected by the short-channel effects. The subthreshold current is nearly independent of carrier mobility, therefore the subthreshold behavior mainly depends on the channel doping profile. Based on this concept, the *threshold-voltage fitting* method using the $V_{th}$–$V_{BS}$ relation is presented to extract the channel profile. This technique can be understood by the following description. The substrate bias forces the depletion region under the gate to extend into the substrate, therefore different surface potentials and space-charge densities correspond to different $V_{BS}$. In other words, the substrate sensitivity of the threshold voltage can monitor the nonuniform channel profile. Because the $V_{th}$, $\Psi_{\sin v}$, $Q_I$, and $Q_{sc}$ calculated in Section II agree well with those extracted by numerical analysis,
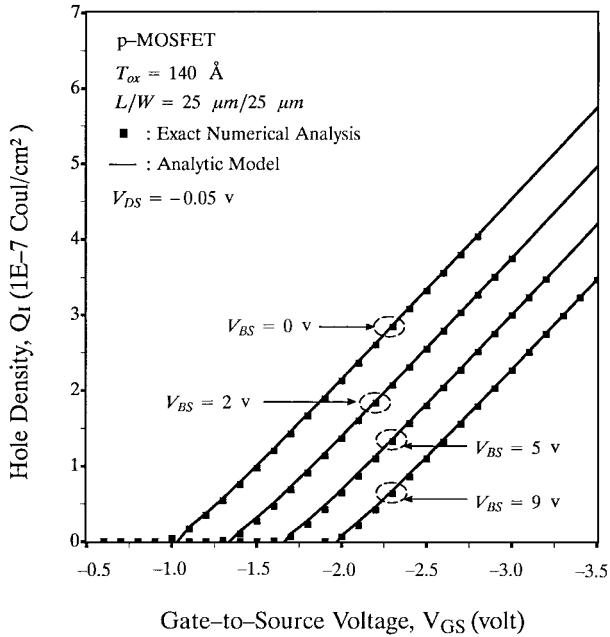
Fig. 3. Comparisons of the hole density between 2-D numerical analysis andanalytic model for different substrate biases.
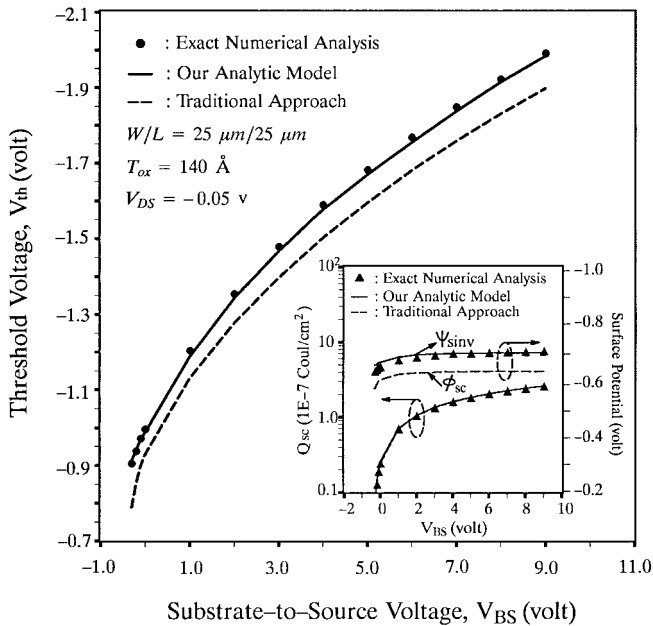


Fig. 4. Application of the developed new strategy to the calculation of thethreshold voltage for $V_{DS} = -0.05$ V. The insertshows comparisons between the numerical data $(Q_{sc}, \phi_s)$ and our analytical calculations. Thecalculation results of the traditional approach are also compared.

consequently the *threshold-voltage fitting* method can be used for profile extraction.

In this work, the approach to extract the threshold voltage from the experimental device is directly based on $I-V$ measurements, the drain current of the enhancement mode MOSFET's operated in the linear region can be expressed by [12]

$$I_{DS} = \frac{k_0}{[1 + \theta(V_{GS} - V_{th})]} \left( V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \quad (15)$$

TABLE II
VARIOUS INITIAL GUESSES AND EXTRACTED PROFILE
PARAMETERS FOR EXACT NUMERICAL ANALYSIS

| Parameter | Initial Guess 1 | Extraction 1 | Initial Guess 2 | Extraction 2 |
|---|---|---|---|---|
| $D_{I1}(10^{12} cm^{-2})$ | -1.8 | -0.976 | -1.5 | - 0.844 |
| $\Delta R_{P1}(10^{-5} cm)$ | 0.6 | 0.58 | 0.25 | 0.397 |
| $R_{P1}(10^{-5} cm)$ | 0.5 | 0.271 | 0.3 § | 0.3 |
| $D_{I2}(10^{12} cm^{-2})$ | 6.5 | 7.403 | 4.0 § | 4.0 |
| $\Delta R_{P2}(10^{-4} cm)$ | 0.7 | 0.715 | 0.3 | 0.439 |
| $R_{P2}(10^{-4} cm)$ | 0.65 | 0.595 | 0.25 § | 0.25 |

§ : the value of parameter is the same as that of Table I and is fixed in optimization.

where $k_0 = \mu_0 C_{ox} W_{eff}/L_{eff}$. $\theta$ is the mobility degradation coefficient and $\mu_0$ is the low field mobility. $L_{eff}$ $(W_{eff})$ is the effective channel length (width). In general, (15) is accurate enough for the long-channel devices. For p-channel devices in modern MOS technology, the concentration of deep phosphorus implant is high enough and the depth of counter-implanted layer is shallow. Due to the built-in voltage of the formed p-n junction, the counter-implanted layer is normally depleted. This leads to enhancement-mode operation and (15) can be applied.

According to (15), we first measure the drain current at a low drain voltage (e.g., $V_{DS} = -0.05$ V), and then the linear extrapolation of drain current at the point where the maximum transconductance occurs gives the extrapolated (or intercept) gate voltage $V_{GSi}$. Therefore, the experimental threshold-voltage can be written as

$$V_{th} = V_{GSi} - \left. \frac{V_{DS}}{2} \right|_{I_{DS}=0}. \quad (16)$$

By using the nonlinear optimization algorithm in [18] and the $V_{th}$ model, we can search several variables in the $V_{th}$ model and minimize the error between the threshold function and experimental data.

## IV. RESULTS AND DISCUSSION

### A. Comparisons With Numerical Data

The structure parameters of the test device are listed in Table I and are used as inputs to SUMMOS. The high accuracy of $V_{th}$ calculation must be claimed because the error of $V_{th}$-$V_{BS}$ between numerical analysis and analytically calculated results will contribute to the extraction of surface concentration. Table II shows two sets of initial and extracted parameters.

Extraction 1 and Extraction 2 are the extracted profiles for initial guess 1 and initial guess 2, respectively. Putting the extracted parameters into 2-D numerical simulator, we can obtain the corresponding subthreshold characteristics for different profiles. It demonstrates that excellent agreements between comparisons can be obtained for long-channel device (not shown in this paper). The insert of Fig. 5 shows the actual and extracted doping profiles, and some discrepancy among them can be observed. This can be attributed to the nonlinear property of the channel profile parameters ($D_{Ii}$, $\Delta R_{Pi}$, and $R_{Pi}$) correlated to the threshold voltage. For this reason, the extracted profile only guarantees to have the same $V_{th}$–$V_{BS}$ relation as that of the actual device. This implies that the channel
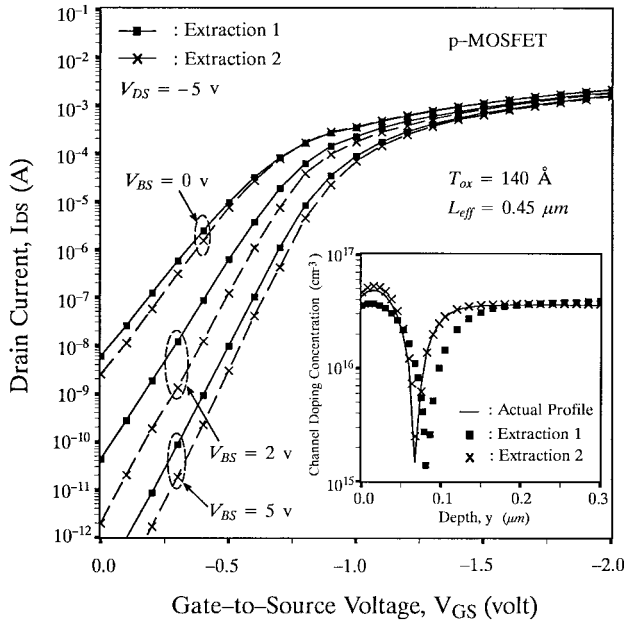
Fig. 5. Comparisons of the simulated subthreshold $I-V$ characteristics between Extraction 1 and Extraction 2 for 2-D numerical device with $L_{\text{eff}} = 0.45$ $\mu$m operated at $V_{\text{DS}} = -5$ V. The insert shows comparisons of the channel doping profiles among the actual profile (solid curve), Extraction 1, and Extraction 2.



Fig. 6. The flowchart of our extraction methodology for determining the channel doping profile.

profile determined by the *threshold-voltage fitting* method is the equivalent profile viewed from the Si/SiO$_2$ interface. There are some equivalent profiles satisfying the measured $V_{\text{th}}$–$V_{\text{BS}}$, the actual profile is one of the extracted equivalent profiles. In order to obtain the actual profile, the doping distribution along the lateral direction must be carefully examined by the DIBL effect [13] and punchthrough phenomenon [14]–[16] of short-channel devices, because the 2-D effects on the subthreshold $I-V$ characteristics are very sensitive to the detailed profile distribution. A 2-D numerical simulator is a powerful tool to investigate these phenomena. Fig. 5 shows comparisons of the simulated subthreshold $I-V$ characteristics between Extraction 1 and Extraction 2 for device with $L_{\text{eff}} = 0.45$ $\mu$m at $V_{\text{DS}} = -5$ V. Obviously, the behaviors of punchthrough characteristics are very different. It is the fact that current path strongly depends on the implanted range and the peak concentration of implantation. Small difference in profiles will lead to large deviations of subthreshold $I-V$ curves. The insert of Fig. 5 also shows that the profile extracted from initial guess 2 can approach the actual one. Based on this observation, it is recommended that the number of unknown/searched parameters must be reduced for profile extraction. The procedure can be easily extended to the experimental extraction if some fabrication parameters of the test devices are known previously.

According to the above discussions, a new feedback technique can be practiced. Under suitable initial guess, the choices of channel profile can be further reduced by the *threshold-voltage fitting* method. For short-channel devices, as the donor dose ($D_{I2}$) is increased or $\Delta R_{P2}$ is decreased, the effective doping level of anti-punchthrough implant increases, causing the drain field penetration to decrease, thus the DIBL is
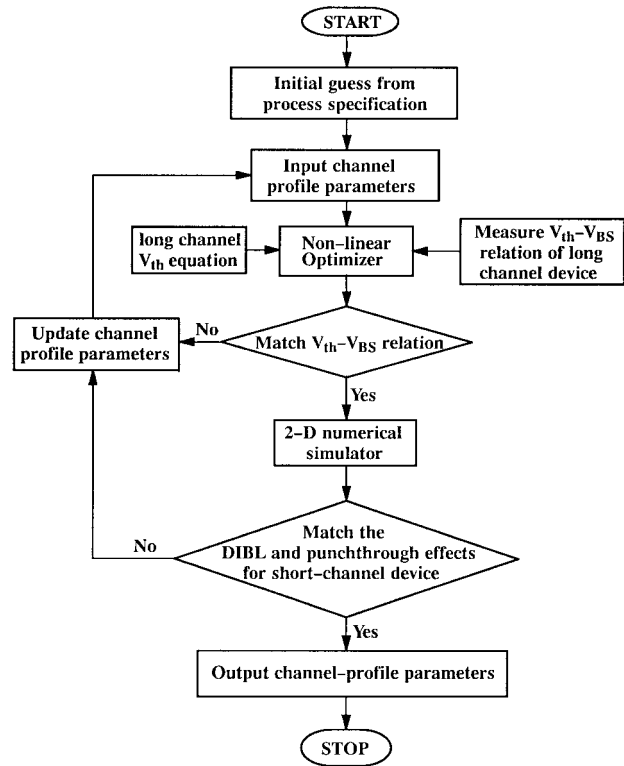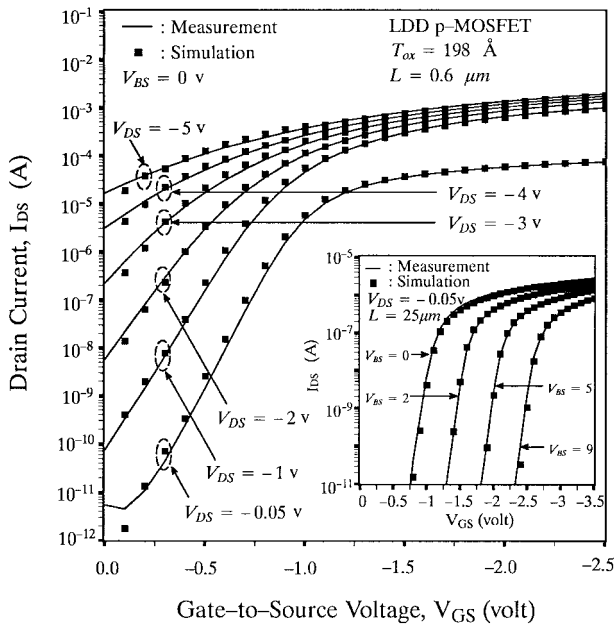
reduced. With the dose level of counter-implanted layer ($D_{I1}$) increases or $R_{P1}$ increases, p-MOSFET's are more prone to the DIBL. For a small-geometry device with the deeper source/drain junction or the steeper junction profile, the DIBL effect is further enhanced. A 2-D numerical simulator is used to evaluate the lateral profile by comparing the DIBL and punchthrough effects of short-channel devices. If good agreements are obtained, the extraction is finished; otherwise the feedback procedure is continued. The full extraction methodology is illustrated in Fig. 6.
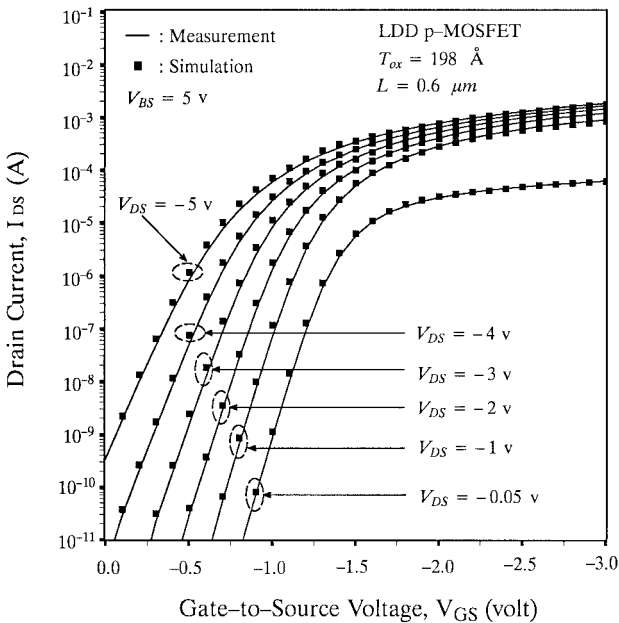
### B. Comparisons with Experimental Data

The test devices studied are fabricated by the 1.0-$\mu$m n-well CMOS technology. The LDD structure is embedded and the gate oxide thickness is 198 Å. Due to buried channel, the induced carriers in the linear region are not tightly confined near the surface, but is widely spread in the counter-implanted layer. With channel broadening, the channel resistance ($R_{\text{ch}}$) becomes smaller and might be comparable with the parasitic resistance ($R_{\text{SD}}$). Small gate drive ($V_{\text{GS}} - V_{\text{th}} - 0.5V_{\text{DS}}$) under suitable substrate bias meets the requirement of $\partial R_{\text{ch}}/\partial V_{\text{GS}} \gg \partial R_{\text{SD}}/\partial V_{\text{GS}}$ and higher accuracy of channel-length reduction ($\Delta L$) can be expected. The method used for extracting $\Delta L$ of counter-implanted p-MOSFET's [21] is slightly different from that of n-MOSFET's [19], which has been verified by a novel technique based on the charge-pumping method [20]. $\Delta L = 0.33$ $\mu$m is obtained for the test devices.

From process specification, we obtain some structure parameters of implantation. For example, $BF^+$ implantation with

(a)



(b)

Fig. 7. Comparisons between the measured and extracted subthreshold $I-V$ characteristics for the test device with $L = 0.6$ $\mu$m operated at (a) $V_{\rm BS} = 0$ V and (b) $V_{\rm BS} = 5$ V.

Si and SiO$_2$ and use the superposed Gaussian function to approximate the implanted profile. Comparisons between our extraction and the measured subthreshold $I-V$ for $L = 25$ $\mu$m are plotted in the insert of Fig. 7(a). The agreements are quite excellent. To check the DIBL and punchthrough characteristics of short-channel devices, the p$^-$ source/drain profile of LDD structure only needs slightly adjusted. In Fig. 7, the measured subthreshold $I-V$ are compared with those obtained from 2-D numerical simulations for $L = 0.6$ $\mu$m operated at different substrate biases. It is clearly seen that the DIBL and punchthrough effects are very prominent at $V_{\rm BS} = 0$ V, as shown in Fig. 7(a). Good agreements in a wide range of drain biases and substrate biases are obtained. It means that the extracted parameters are accurate. Therefore, the proposed method is successfully verified and has high efficiency/accuracy.

## V. CONCLUSION

The formulation and verification of a new self-consistent strategy for the $V_{\rm th}$ calculation and the surface potential at threshold are provided. The definition and the resultant criterion of the onset heavy-inversion in MOSFET with nonuniformly doped substrate have been used to compute $Q_{\rm sc}$. Comparisons between analytic model and exact numerical analysis have been made and high accuracy can be obtained. Based on the calculated $V_{\rm th}$, the *threshold-voltage fitting* method has been implemented in a nonlinear optimizer to automatically adjust the profile parameters of p-MOSFET's with counter implantation. With the aid of a 2-D numerical simulator and by comparing the DIBL and punchthrough effects of short-channel devices, the extracted channel profile can approach the actual one by our extraction methodology. Good agreements have been found with the measured subthreshold characteristics for both long-and short-channel devices. The extracted channel profile can be used for the evaluation of the p-MOSFET's characteristics and precise process monitoring.

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energy of 25 Kev and dose of $1.1 \times 10^{12}$/cm$^2$ is used for the threshold adjustment and the implantation range $R_{P1}$ can be estimated to be around 0.095 $\mu$m. For n-well, phosphorus ions are implanted with energy of 150 Kev and dose of $5.5 \times 10^{12}$/cm$^2$, and therefore, $R_{P2}$ is about 0.23 $\mu$m. Though high-temperature processing steps can alter the channel profile by redistribution and segregation of dopants, we assume the deviations of $D_{Ii}$ and $R_{Pi}$ between initial and actual values are not large. Therefore, the initial guess for implantation can be confined within a small interval during optimization. Here we neglect the difference in stopping power between

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**Chien-Min Wu** (S'92), for a photograph and biography, see this issue, p. 2199.

**Yuan Wu** (M'72), for a photograph and biography, see this issue, p. 2199.