3D GOI CMOSFETs with Novel IrO_2(Hf) Dual Gates and High-κ Dielectric on 1P6M-0.18μm-CMOS

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Abstract

For the first time, we demonstrate 3D integration of self-aligned IrO_2(Hf)/$LaAlO_3$/GOI CMOSFETs above 0.18 μm Si CMOSFETs. At EOT=1.4nm, the novel IrO_2(Hf) dual gates (4.4 and 5.1 eV workfunction) on control 2D $LaAlO_3$/Si devices have high electron and hole mobilities of 203 and 67 cm^2/Vs. On the 3D structure the $LaAlO_3$/GOI shows even higher 389 and 234 cm^2/Vs mobilities, and process compatibility with current Si VLSI. The higher drive current, larger integration density, shorter interconnects distance, and simple process of 3D approach can help solve the AC power issue and 2D scaling limitation.

Introduction

As down-scaling continues beyond the implementation of high-κ gate dielectrics for VLSI ICs, the AC power consumption from the interconnect capacitance ($Cv^2f/2$) becomes a major barrier [IEDM 2003 panel session]. This arises from increasing interconnect density and operational frequencies (f). Although wireless or optical interconnects are useful [1]-[2], they currently only apply to inter-chip connections. Another difficult challenge is that the scaling limits of CMOS (<10nm), from source-drain quantum-mechanical tunneling, are being approached [3]-[4]. In this paper, we propose and demonstrate a solution for the AC power consumption and also address the scaling limitation, by using a simple 3D integration. The 3D IC structure is similar to the logic and memory functions in the brain, which may provide an effective low cost solution to rapidly increasing cost of IC fabs as scaling down. However there are technological challenges to realize such 3D ICs within a low thermal budget and small impact on the lower-layer devices. Previously we have shown that GOI MOSFETs [5]-[6] meet the required low thermal budget of a 500°C RTA, show dislocation free for high yield and display high mobility. To achieve full 3D integration and a VLSI-compatible process, we fabricated self-aligned IrO_2(Hf) dual-gate high-κ [7]-[9] $LaAlO_3$/GOI CMOSFET on 1-Poly -6-Metal (1P6M) 0.18μm Si devices. No degradation of bottom 0.18μm devices was measured due to low RTA. The IrO_2 gate has high 5.1 eV workfunction and 4 orders of magnitude lower J_g than SiO_2 at 1.4 nm EOT, which can largely reduce the DC power consumption. The control 2D IrO_2(Hf)/$LaAlO_3$ CMOS on Si have high electron and 80% universal hole mobility comparable with the best metal-gate/HfO_2 CMOS [10]. The 3D GOI CMOS had even higher electron and hole mobilities than similar devices on 2D Si. The high max operation voltage ($|V_{max}|$) of 1.2 V for a 10 year lifetime at 85°C is comparable with or better than HfAlO [11] and HfSiON [12] devices. The higher 3D integration density and 2.2-2.4X better drive current in the GOI transistors are equivalent to device scaling. Thus, the 3D metal-gate/high- κ/GOI/Si integration not only reduces the AC and DC power consumptions, but also equivalently extends CMOS scaling beyond 2D quantum-mechanical limit. The low cost process and equivalent scaling in 3D GOI IC may be one of the potential solutions to the rapidly increasing fab cost as continuously scaling down.

Experimental Procedure

The self-aligned 3D GOI CMOS was formed by PECVD SiO_2 deposition on both H^+-implanted Ge and 1P6M 0.18μm MOSFETs, O_2 plasma enhanced bonding, a smart-cut at 300°C, followed by 400°C annealing and slight polishing [3]-[4]. The high-κ $LaAlO_3$ was deposited from a κ=25.1 $LaAlO_3$ source. Then 150nm-IrO_2 or 150nm-IrO_2/15nm-Hf gate was formed on $LaAlO_3$ followed by self-aligned P^+ or B^+ source-drain implant for n- or p-MOSFET, respectively. The activation was done by 500°C or 950°C RTA for respective 3D GOI or 2D Si CMOSFETs.

Results and Discussion

(A) 3D integration:

Figs. 1-4 show the 3D structure, S-parameters, measured S_{21} loss, and power loss of 3D interconnects. The total AC power consumed by 3D interconnect is the sum of each $Cv^2f/2$, $Li^2f/2$ and $i^2Rf/2$, which can be calculated from S-parameters rather than from complicated CLR distributed circuit. The integrating 1 or 2 layers of GOI CMOS on Si ICs can reduce the interconnect distance, S_{21} signal coupling loss and AC power consumption very effectively.

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Fig. 5 is the picture of 3D GOI selectively formed on 1P6M Si device. This is due to the thicker surface profile of ~2μm M6 in Fig. 6, and Figs. 7-8 are the X-TEM views of bottom 0.18μm MOSFET and top GOI. The I_d-V_d and I_d-V_g data for the lower Si MOSFETs (Figs. 9-10) show minor degradation even after a 500°C RTA for top GOI CMOS.

(B) IrO_2(Hf)/$LaAlO_3$ on 3D GOI and control 2D Si CMOS:

Fig. 11 is the V_{fb} and EOT plot for IrO_2(Hf)/$LaAlO_3$ /Si devices after 550-950°C RTA. The IrO_2 gate has a high workfunction of 5.1 eV, close to Ir (5.2 eV), which is reduced to 4.4 eV by adding low workfunction 15nm-Hf on $LaAlO_3$. The small $|V_{fb}|$ decrease with increasing RTA to 950°C suggests little Fermi-level pinning. Figs. 12-13 show the J_g-V_g of IrO_2(Hf)/$LaAlO_3$ CMOS on Si or GOI. The J_g is ~10X lower using IrO_2 than Ir that is most probably due to lower metal diffusion in more thermal-dynamic stable IrO_2 compared with pure metallic Ir. Figs. 14-15 are the C-V and identical C_{inv} and C_{acc} using IrO_2 or IrO_2/Hf indicating no gate depletion in CMOS with EOT=1.4nm and ~4 orders lower J_g than SiO_2. Figs. 16-19 show the I_d-V_d and I_d-V_g of IrO_2(Hf)/$LaAlO_3$ CMOS on Si or GOI. The I_d is a lot higher using GOI, and further increases for PMOS on (110) GOI. Small V_t of -0.25V is measured in the PMOS devices, reflecting high workfunction and little Fermi-level pinning. Figs. 20-21 show the mobility data. Good electron and hole mobility of 203 and 67cm^2/Vs are measured in IrO_2(Hf)/$LaAlO_3$/Si CMOS, comparable with the best metal-gate/HfO_2/Si data [10]. The hole mobility, up to ~0.8X universal mobility, may be due to the perfect match of both oxide gate and oxide high-κ, and excellent metal and O_2 diffusion barrier of IrO_2. The electron and hole mobility improved, for IrO_2(Hf)/$LaAlO_3$ on GOI over Si, by 1.8X and 3.5X - to 357 and 234 cm^2/Vs. This values are close to universal electron mobility and 2.5X higher than universal hole mobility at 1 MV/cm E_{eff}. Further improving mobility beyond GOI is possible by integrating low temperature processed III-Vs on 3D IC [13]-[14]. Figs. 22-24 are the NBTI and PBTI, which are comparable with or better than the metal-gate on HfAlO [11] or HfSiON [12] devices. This may be due to the strong AlO in high-κ $LaAlO_3$ but much reduced κ in HfAlO or HfSiON for better BTI improvement than HfO_2 [12]. High 1.9 or 1.2 V $|V_{max}|$ at RT or 85°C is obtained from extrapolated NBTI (50mV change) for 10 years lifetime. The good 3D CMOS may also provide equivalent scaling extension after 2D CMOS approaches the quantum mechanics limit, in addition to the advantage of low AC power consumption.

Conclusions

We have shown for the first time 3D integrated metal-gate/high-κ/GOI CMOSFETs on 1P6M 0.18μm Si devices. The larger I_d, higher 3D density, shorter interconnects and 4 orders lower J_g in 3D provide low cost solutions to AC and DC power consumptions and scaling limitation.

Acknowledgments

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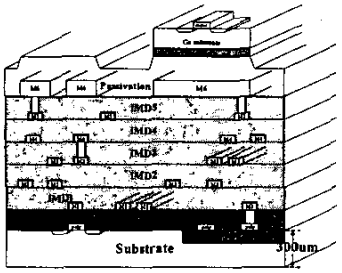

Fig. 1. Schematic of the 3D VLSI with multi-level parallel interconnect lines and GOI CMOS. The AC power consumes $Cv^2f/2$ $Li^2f/2$ and $i^2Rf/2$ in parasitic C, L R circuits.

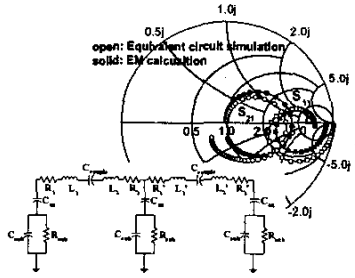

Fig. 2. The equivalent circuit simulated and 3D EM calculated S_{21} and S_{11} for 1mm long 0.5μm spacing parallel lines. The consumed AC powers can be calculated by solving CLR circuit or simply from S by $1-|S_{11}|^2-|S_{21}|^2$.

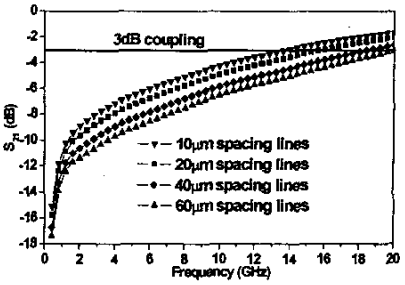

Fig. 3. Measured S_{21} coupling of 1-mm long two parallel lines with various spacing from 10 to 60μm using M6. The 3dB coupling is the limit since 50% signal loss to 2nd line.

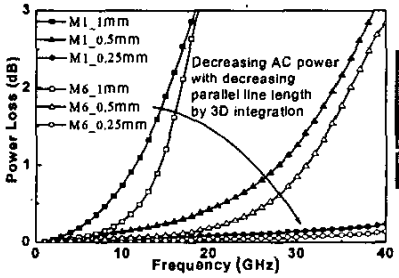

Fig. 4. Calculated power loss of 1-mm long 0.5μm spaced parallel lines. The 3D integration can reduce line length to 0.5-mm (1 GOI) or 0.25-mm (2 GOI layers on Si IC).

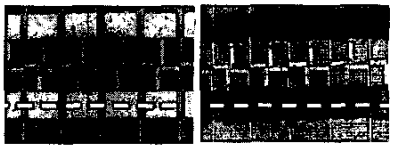

Fig. 5. Pictures of 0.18μm MOSFETs with probing pads (M6 and 2μm thickness). The "dark" area on the pad after bonding is due to the selectively bonded Ge by "smart cut".

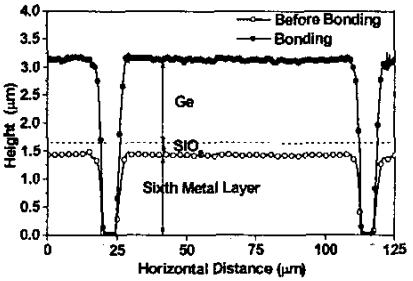

Fig. 6. Surface profile (dashed line in Fig. 5) before and after Ge bonding and "smart cut". A Ge thickness of 1.6μm is obtained.

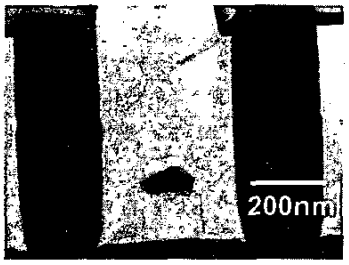

Fig. 7. The cross-sectional TEM of lower 0.18μm MOSFET.

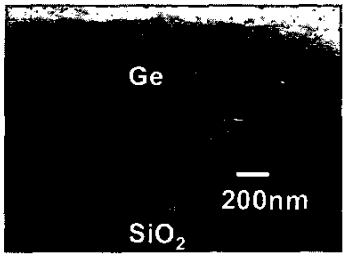

Fig. 8. The cross-sectional TEM of selectively bonded and smart cut Ge-on-Insulator on pad. Dislocation free and smooth Ge/SiO_2 interface are observed.

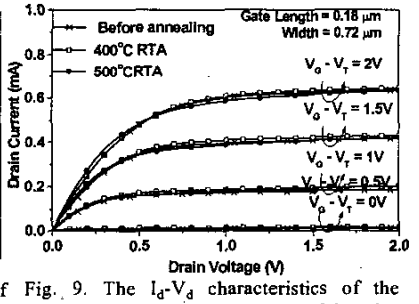

Fig. 9. The I_d-V_d characteristics of the 0.18μm MOSFETs beneath 3D GOI after bonding. No drain current degradation occurs after processing thermal cycle.

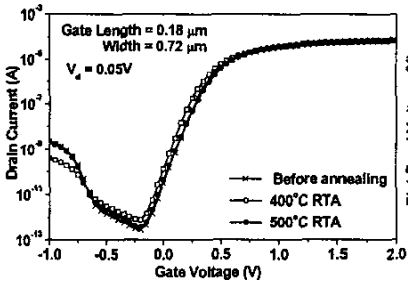

Fig. 10. The I_d-V_g characteristics of the 0.18μm MOSFETs beneath 3D GOI after bonding. Near identical I_{ds} is measured after processing thermal cycle.

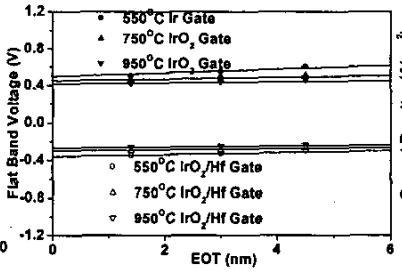

Fig. 11. The V_{fb} and EOT plot for IrO_2 and IrO_2/Hf gate on $LaAlO_3$/Si after different RTA condition from 550 to 950°C.

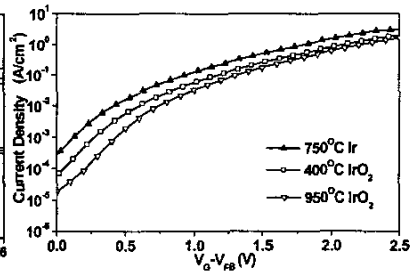

Fig. 12. J_g-V_g of 150nm-IrO_2/$LaAlO_3$/Si MOSFETs. The J_g is much lower using IrO_2 than Ir gate.

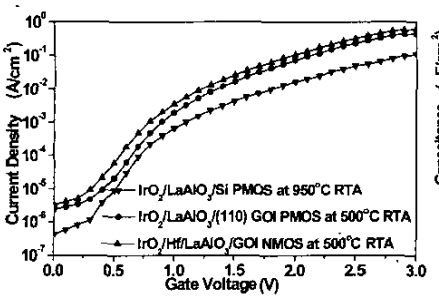

Fig. 13. The J_g-V_g curves of IrO_2/20nm-Hf or IrO_2 on $LaAlO_3$ MOSFETs on Si or GOI at 1.4nm EOT. The J_g is ~10^4X lower than SiO_2 at 1.4nm EOT.

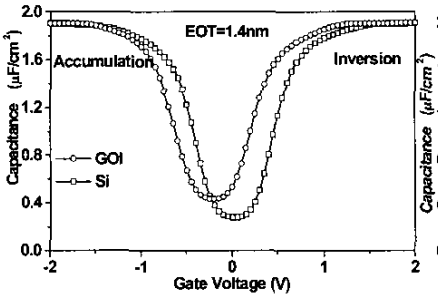

Fig. 14. The C-V characteristics of IrO_2/ 20nm-Hf on $LaAlO_3$ gate dielectric n-MOSFETs on Si and GOI.

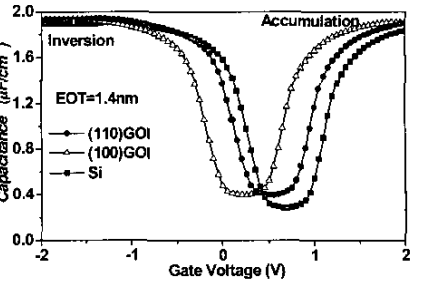

Fig. 15. The C-V characteristics of IrO_2 on $LaAlO_3$ gate dielectric p-MOSFETs on Si and GOI.

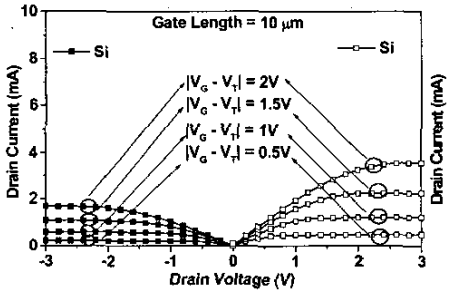

Fig. 16. The I_d-V_d characteristics of IrO_2/ 20nm-Hf or IrO_2 on $LaAlO_3$ gate dielectric n- and p-MOSFETs on Si.

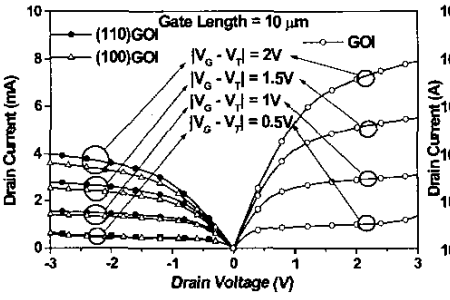

Fig. 17. The I_d-V_d characteristics of IrO_2/ 20nm-Hf or IrO_2 on $LaAlO_3$ gate dielectric n- and p-MOSFETs on GOI. Higher I_d is observed than on Si in Fig. 16.

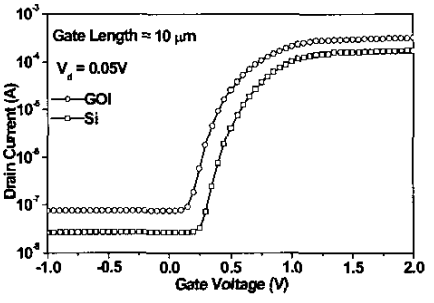

Fig. 18. The I_d-V_g characteristics of IrO_2/ 20nm-Hf on $LaAlO_3$ gate dielectric n-MOSFETs on Si or GOI.

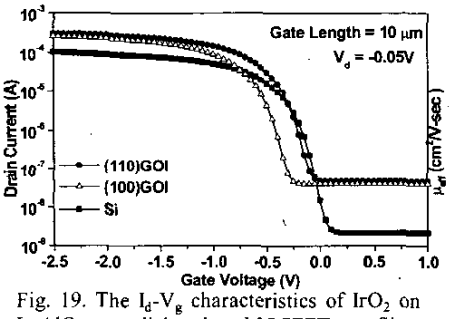

Fig. 19. The I_d-V_g characteristics of IrO_2 on $LaAlO_3$ gate dielectric p-MOSFETs on Si or GOI. Low V_t of -0.25V is measured in Si and (110)Ge.

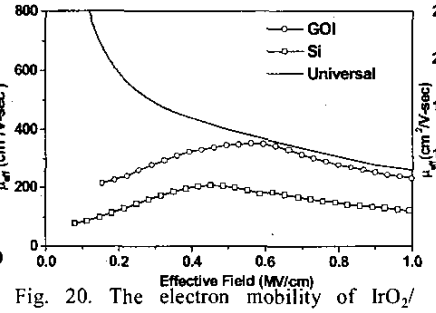

Fig. 20. The electron mobility of IrO_2/ 20nm-Hf on $LaAlO_3$ n-MOSFETs on Si or GOI. The GOI has 1.8X higher peak electron mobility improvement.

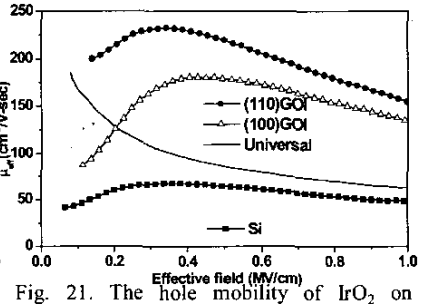

Fig. 21. The hole mobility of IrO_2 on $LaAlO_3$ p-MOSFETs on Si or GOI. The PMOS on Si and GOI have 0.8X and 2.5X universal hole mobility at 1 MV/cm E_{eff}.S

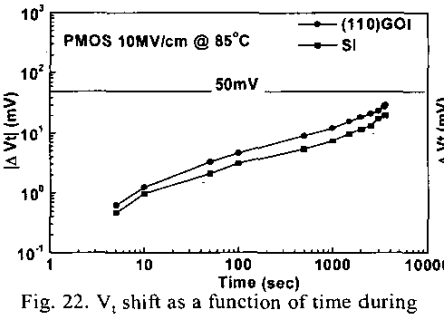

Fig. 22. V_t shift as a function of time during NBTI measurement of IrO_2/$LaAlO_3$ on 3D GOI or 2D Si PMOS at 85°C and 10MV/cm.

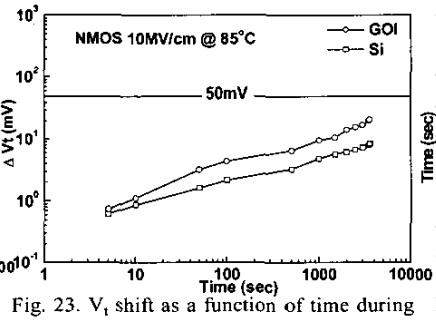

Fig. 23. V_t shift as a function of time during PBTI measurement of IrO_2/Hf/$LaAlO_3$ on 3D GOI or 2D Si NMOS at 85°C and 10MV/cm.

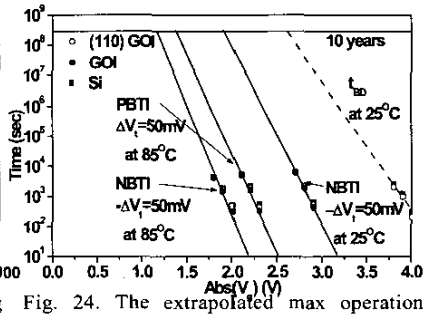

Fig. 24. The extrapolated max operation voltage $|V_{max}|$ from BTI and t_{BD} for 10 years lifetime. The $|V_{max}|$ is limited by NBTI that is reduced from 1.9 V at RT to 1.2 V at 85°C.