A Novel Methodology for Extracting Effective Density-of-States in Poly-Si Thin-Film Transistors

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Abstract

A novel methodology that greatly simplifies the procedure of extracting the effective density-of-states (DOS) in polycrystalline-Si thin-film transistors (poly-Si TFTs) is proposed and demonstrated. The characterization is performed on a Schottky barrier (SB) TFT with electrical source/drain extensions induced by a field-plate. Only one single device and two simple subthreshold I-V measurements at room temperature are needed for full band-gap DOS extraction. Impacts of different process treatments are clearly resolved using this methodology.

Introduction

Poly-Si TFTs have been investigated extensively due to their applications in large-area electronics like flat-panel displays. The operation of poly-Si TFTs is more complicated compared with their single-crystal counterpart due to the existence of grain boundaries in the channel, since the defects at and inside the grain boundaries may increase the off-state leakage, retard the device turn-on, and impede the carrier transport (1). Accurate modeling of poly-Si TFT behavior is thus indispensable for simulation and design of poly-Si TFT circuits. This requires precise determination of the effective density-of-states (DOS) distribution within the poly-Si band gap. Previously, field-effect conductance (FEC) method (2~4) which characterizes the subthreshold conductance of devices has been employed to extract DOS. Fig. 1 shows the flow chart of FEC analysis. Detailed theoretical background of FEC could be found in (2) and (3). Briefly, three major steps are involved: (a) determination of flat-band voltage, V_{FB}, (b) determination of relationship between V_G and surface potential, ψ_s, and (c) calculation of DOS as a function of $E-E_F$ within the gap. In step (a), V_{FB} can be determined as the V_G when the term $T \bullet [d(\log G)/dV_G]$ is independent of temperature. (T is temperature, G is I_D/V_D) (5). In step (b), either the "***incremental method***" or the "***temperature method***" can be adopted (3). To obtain full band-gap DOS, at least one n-channel device and one p-channel device are needed for characterization. Besides, I-V measurements need to be performed at various temperatures, making the procedure very tedious and time-consuming. In this work, we present a novel methodology to address this issue. In this scheme, all we need for full band-gap DOS extraction are only one device and two I-V measurements performed at room temperature. The whole process is thus greatly simplified and shortened.

Structure of the Test Device

The characterization is performed on a Schottky barrier (SB) TFT which features metallic (CoSi) source/drain and a sub-gate lying over the passivation oxide (6~7), as shown in Fig. 2. During operation, electrical source/drain extensions are induced in the channel offset regions underneath the gate sidewall spacers by applying a high voltage on the sub-gate (or the field-plate). Depending on the polarity of sub-gate bias, the device could be set for either n- or p-channel operation. The formation of electrical junctions could also dramatically reduce the off-state leakage (7), which is essential for the analysis. To reduce the impact of series resistance on the analysis, self-aligned sidewall spacers were used to define the channel offset regions. By exploiting the ambipolar characteristics of Schottky-barrier (SB) TFTs, full band-gap DOS can be obtained on a single device. Detailed device fabrication and operation could be found in our previous reports (6~7).

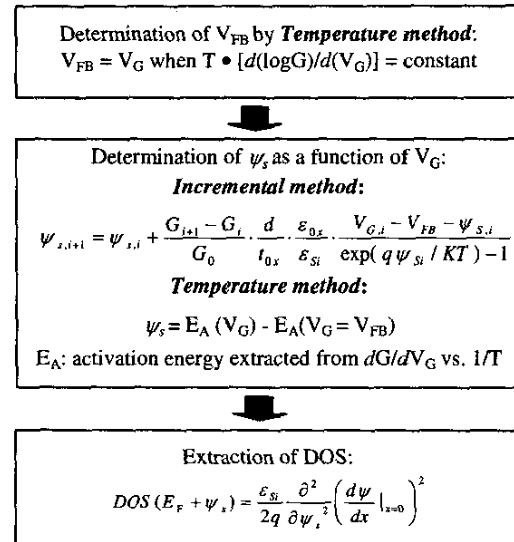

Fig. 1 Flow chart for extracting DOS in TFT using conventional FEC method.

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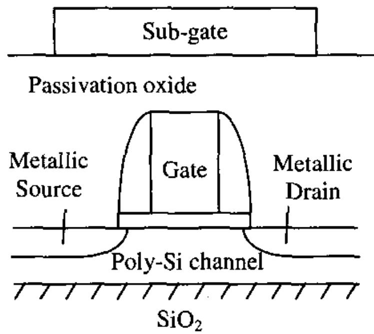

Fig. 2 Structure of poly-Si SB-TFT featuring silicide source/drain and a sub-gate lying over the passivation oxide.

Experimental Results

A. Determination of V_{FB} by temperature method

Multiple I_D-V_G measurements were performed at various temperatures to determine V_{FB}. In this work we found that the V_{FB} extracted from n-channel operation coincides well with that of p-channel operation with the same device. An example is shown in Fig.3 in which $T[d(\log G)/dV_G]$ is expressed as a function of 1000/T. In the figures, the results for both p- and n-channel operations indicate that V_{FB} is around –2.1 V at which $T[d(\log G)/dV_G]$ is almost independent of temperature. This consistency between the two operation modes is expected and confirms the validity of this method.

B. DOS extraction

Next, we used both the "incremental method" and the "temperature method" to extract DOS. Ambipolar subthreshold I-V characteristics measured at various temperatures are show in Fig. 4. For the "temperature method", Arrehenius plots of dG/dV_G and the corresponding E_A as a function of V_G are shown in Fig. 5 and Fig. 6, respectively. Good agreement in the extracted DOS between the two methods is obtained, as shown in Fig. 7. We have also performed the "incremental method" at room temperature and 55 °C to check if ambient temperature will cause any disparity on the results. As can be seen in Fig. 8, no significant difference is observed between the two characterizations.

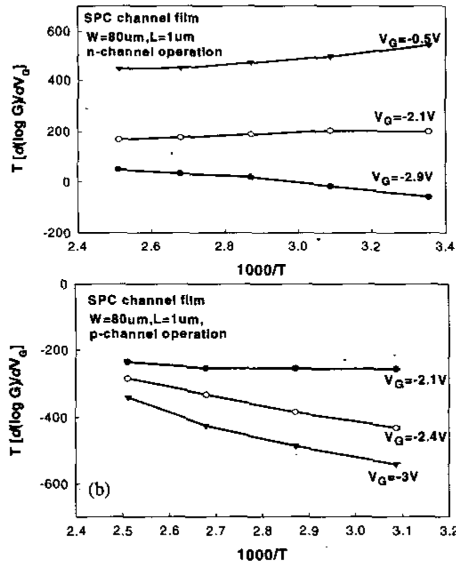

Fig. 3 $T[d(\log G)/dV_G]$ vs. 1000/T for (a) n- and (b) p-channel operations of a SB poly-Si TFT. In both cases, V_{FB} is determined to be around -2.1 V.

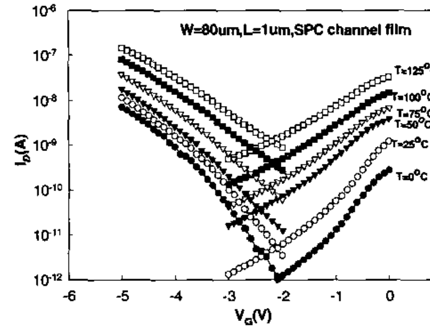

Fig.4 Ambipolar subthreshold I-V characteristics of a SB poly-Si TFT measured at various temperatures.

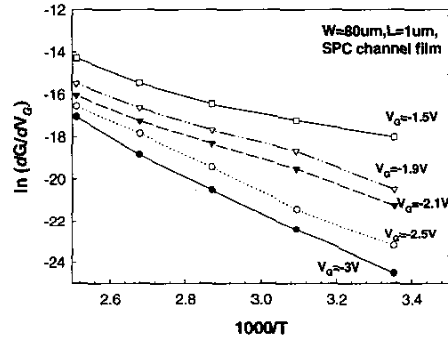

Fig. 5 Arrhenius plots of ln (dG/dV_G) extracted from Fig. 4.

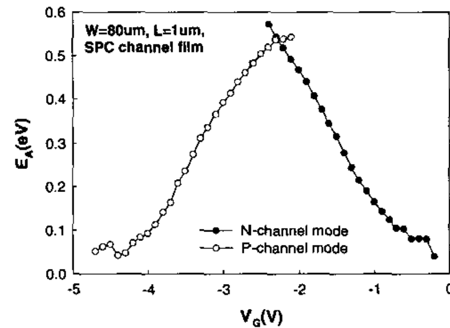

Fig. 6 Activation energy extracted from Figs. 4 and. 5.

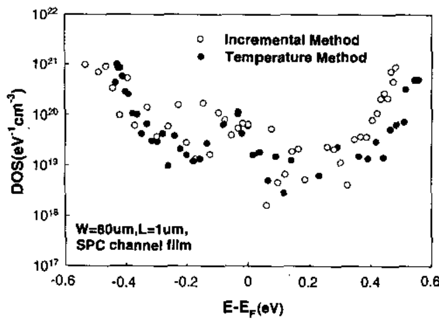

Fig. 7 DOS results obtained by using incremental method and temperature method.

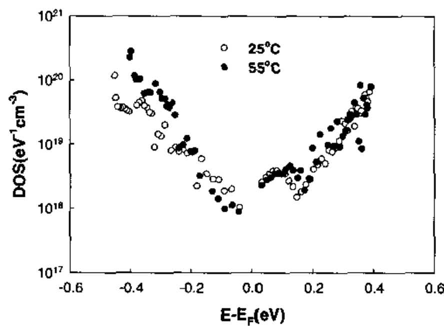

Fig. 8 DOS results obtained by using incremental method performed on ambipolar subthreshold I-V characteristics measured at 25 and 55 °C

C. *Effects of process treatments*

It's well known that the DOS of poly-Si TFT is closely related to the channel preparation methods and the process conditions. In this work the new DOS characterization scheme was also employed to study the impact of different process treatments on the device characteristics. Fig. 9 illustrates the effect of plasma hydrogenation performed in an NH_3 plasma at 300 °C for one hour. As can be seen in the figure that such plasma treatment is useful in reducing the DOS, especially for those located near the mid-gap level.

Fig.10 compares the DOS characteristics of devices with channel prepared by three different schemes, namely, as-deposited poly-Si, solid-phase crystallization (SPC), and excimer laser annealing (ELA). Among those splits the ELA sample shows lowest DOS value. Figs. 11 (a) and (b) show the TEM pictures for SPC and ELA samples, respectively. The larger grain size observed in the ELA sample explains the results shown in Fig.10. The above results indicate that the proposed methodology is useful in resolving the effects of different process treatments on the material and device characteristics.

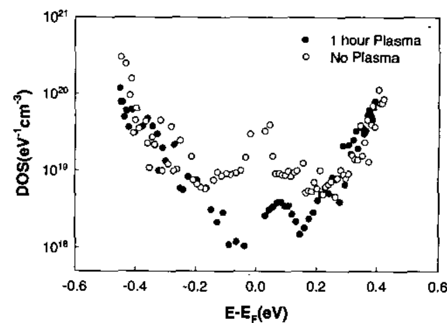

Fig. 9 Effects of plasma treatment on the DOS of devices. The results indicate that 1-hour NH_3 treatment is effective in reducing the mid-gap defect density.

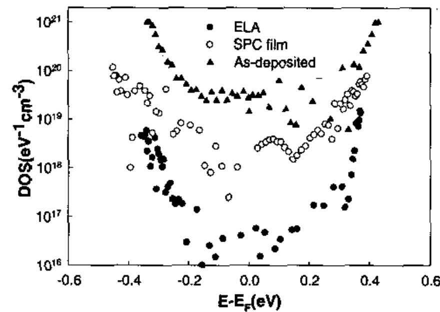

Fig. 10 Effects of different recrystallization treatments on the DOS of devices.

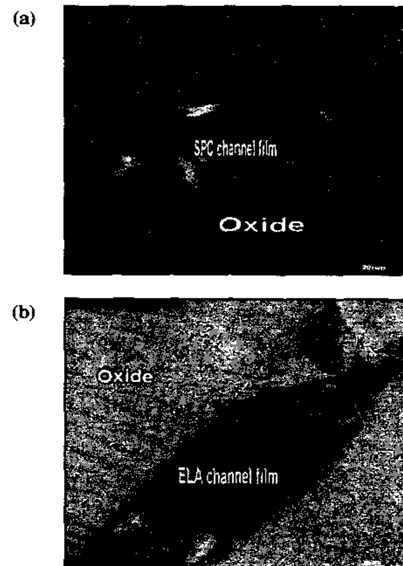

Fig. 11 TEM pictures of characterized samples that received (a) solid-phase crystallization (SPC), and (b) excimer laser annealing (ELA) treatments. The larger grain size in ELA sample well explains its low extracted DOS shown in Fig. 10.

D. A new way for determining V_{FB}

Finally, an important finding is discovered during the course of this study. Specifically, we observed that the extracted V_{FB} using the tedious conventional temperature scheme coincides well with the V_G value at the intersection point of the bi-channel I-V curves measured at room temperature. An example can be found by comparing Fig. 3 and Fig. 4. To further validate the universality of this observation, different groups of samples were characterized and the results are summarized in Fig. 12. It can be seen that good agreements are obtained in all cases. This important finding thus provides a new and much simpler methodology for the determination of V_{FB}.

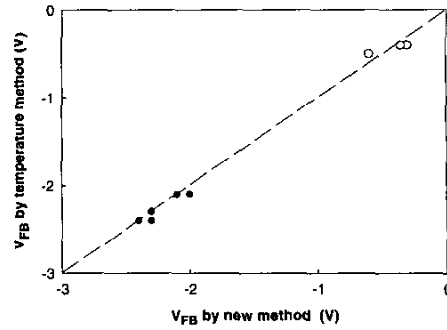

Fig. 12 Comparison of V_{FB} values determined using the conventional ***temperature method*** and the new methodology performed on two groups of devices with various parameters.

Discussion and Conclusion

Using the new methodology, the overall DOS extraction procedure for TFT can be greatly simplified compared to the conventional scheme (TABLE I). In short, only a single device and two simple subthreshold I-V measurements at room temperature are all that needed for full band-gap DOS extraction. In addition, the new methodology lends itself handily to automatic measurement system. It is very simple and useful for TFT technology development as well as practical manufacturing, since the device structure (Fig. 2) and layout are compatible with modern TFT technology. In particular, the sub-gate can be formed simultaneously with the metal pad, so no extra mask is needed. And the formation of the metallic source/drain could be cleverly incorporated into the baseline by skipping the source/drain implant in the DOS test structure.

In this work, only the defect states contained in the channel are considered, though more precise DOS extraction is possible if the oxide interface states are also taken into account (8). This will be the main subject of our future work.

Acknowledgement

The authors would like to thank the National Nano Device Laboratories (NDL) for assistance in device fabrication. This work was supported by the NSC 93-2215-E-492-003.

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TABLE I Comparison between conventional and the new methodologies.

	Conventional FEC methodology	The new methodology
Test device	One p-device for extracting DOS between Ev and Ei in the gap. One n-device for extracting DOS between Ec and Ei in the gap.	One SB device for full band-gap DOS extraction.
V_{FB} determination	***Temperature method*** Multiple I-V measurements conducted at various temperatures are necessary.	$V_{FB} \approx V_G$ @ the intersection point of ambipolar subthreshold I-V curves. Only needs to perform two I-V measurements at room temperature.
Determination of ψ_s as a function of V_G	***Temperature method*** or ***Incremental method.***	***Incremental method.***